(From the register file's two write ports)

WDest0
WDest1

Br Logic

Resolve or Kill

UOP Code | BrMask | Ctrl... | Val | RDst | RS1 | p1 | RS2 | p2

issue slot is valid

ready

ready

request

issue

Control Signals

Physical Destination Register

Physical Source Registers

Issue Select Logic

Issued to the *Register Read* stage