Solution & Marking scheme

Ryerson University

Department of Electrical and Computer Engineering

ELE404 (Electronic Circuits I)

Final Examination (P2013)

July 2013

Duration: 180 minutes

Examiner: Prof. A. Yazdani

Name:..

[Print Last Name] [Print First Name]

Student No:........................... Section:....

NOTES

1. This is a closed-book examination. No aids other than basic scientific calculators are permitted.

2. The last two pages include some useful formulae and circuit configurations. **You may only detach the two information pages**.

3. The examination paper is comprised of **EIGHT QUESTIONS**, *each* question worth as indicated in the following Table. The entire examination is worth *200* marks.

Question #	Maximum Mark	Mark Earned
1	**25**	
2	**20**	
3	**20**	
4	**25**	
5	**30**	
6	**20**	
7	**30**	
8	**30**	
Total	**200**	

4. Answer all questions in the booklet, within the blank spaces provided under each question in this booklet. Use the reverse if needed.

5. ***No Questions to be asked during the examination***. *If in doubt about any question, clearly state your assumptions in answering the question.*

6. Part marks for an answer will only be given if the *correct methodology* is clearly shown.

Q1: **Fig. 1** shows a current-steering circuit in which all of the transistors are of the same parameters, except $Q4$ whose emitter-base junction area is four times that of the other transistors. Further, $V_{CC} = 5.0\ V$, $-V_{EE} = -3.3\ V$, $R = 6.9\ k\Omega$, and $|V_{BE(on)}| = 0.7\ V$. Assuming that all transistors are in the active mode and β is very large, calculate the labeled currents. Summarize your results in **Table 1**. Show all the work.

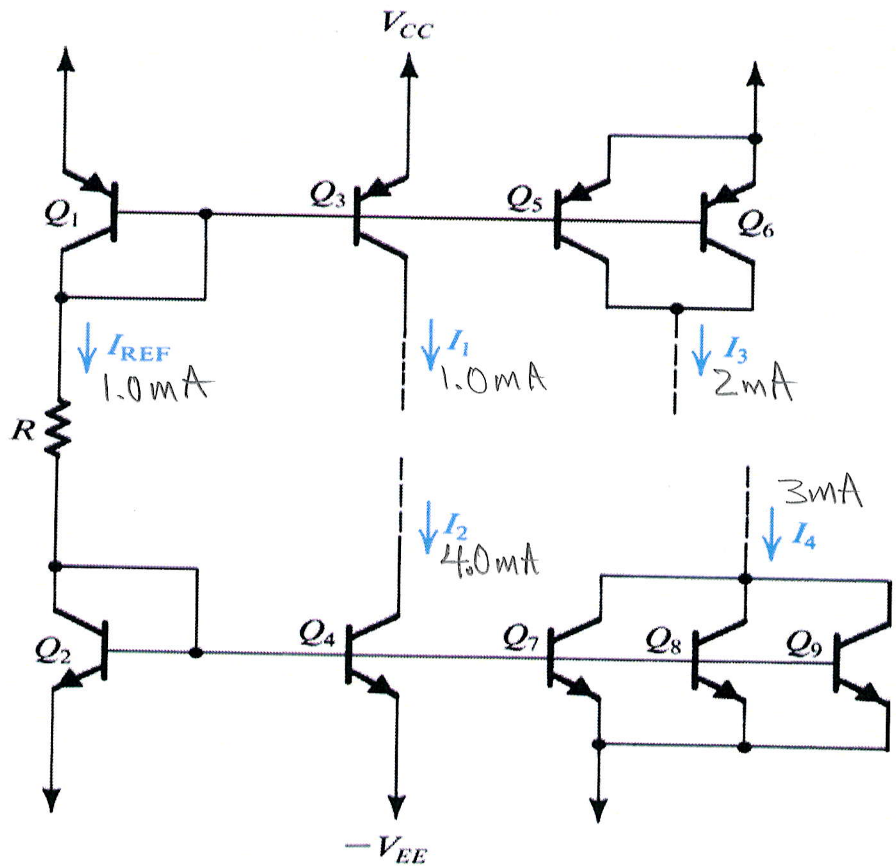

Fig. 1: Current-steering circuit of Q1.

Table 1. Currents in the circuit of **Fig. 1 [each 5 marks]**.

$I_{REF}[mA]$	$I_1[mA]$	$I_2[mA]$	$I_3[mA]$	$I_4[mA]$
1.0	1.0	4.0	2.0	3.0

$$I_{REF} = \frac{V_{CC} - V_{BE} - V_{BE} + V_{EE}}{R} = \frac{5.0 - 1.4 + 3.3}{6.9} = 1.0\ mA$$

$I_C = 1.0\ mA$ for all transistors except Q4

$I_{C4} = 4 \times 1.0 = 4.0\ mA$

$\Rightarrow I_1 = I_{C3} = 1.0\ mA$

$I_3 = I_{C5} + I_{C6} = 2.0\ mA$

$I_2 = I_{C4} = 4.0\ mA$

$I_4 = I_{C7} + I_{C8} + I_{C9} = 3.0\ mA$

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Q2: In the differential amplifier of **Fig. 2**, the MOS devices are identical and the parameters are: $k = 5\ mA/V^2$, $V_A = \infty$, $V_t = 0.5\ V$, $I = 1.0\ mA$. Further, $V_{DD} = V_{SS} = 5.0\ V$. Calculate R_D such that the dc (bias) drain voltages are $V_{D1} = V_{D2} = 1.0\ V$. Then, calculate the differential voltage gains $A_{d1} = v_{d1}/v_{id}$, $A_{d2} = v_{d2}/v_{id}$, and $A_d = (v_{d2} - v_{d1})/v_{id}$. Report your results in **Table 2**.

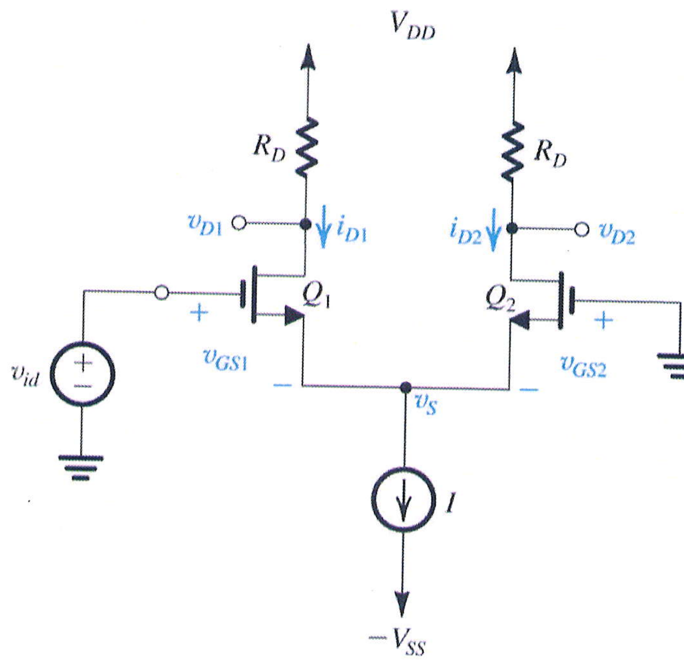


Fig. 2: Differential amplifier of Q2.

Table 2. Results for the amplifier of **Fig. 2 [each 5 marks]**.

R_D [kΩ]	$A_{d1} = \frac{v_{d1}}{v_{id}}$ [V/V]	$A_{d2} = \frac{v_{d2}}{v_{id}}$ [V/V]	$A_d = \frac{v_{d2}-v_{d1}}{v_{id}}$ [V/V]
8.0	−8.94	8.94	17.89

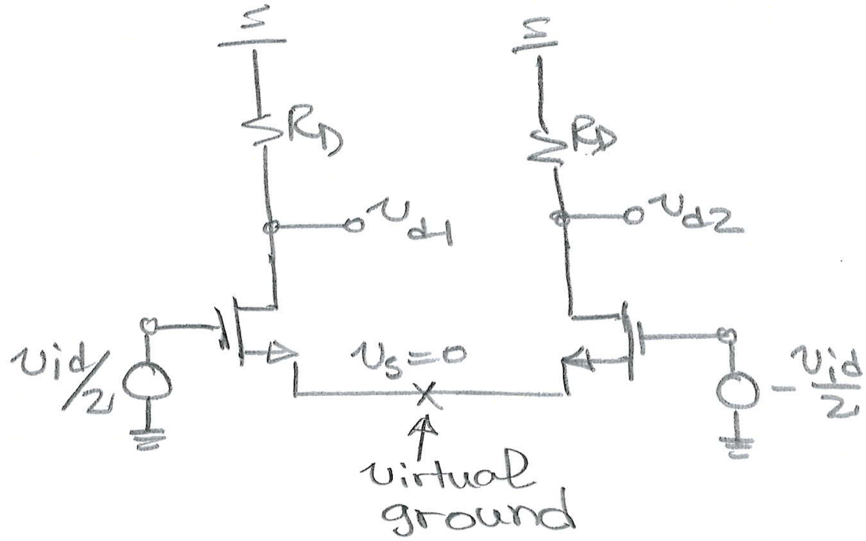
$I_{D1} = I_{D2} = \frac{1}{2} I = 0.5\,mA$

$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5 - 1.0}{0.5} = 8.0\,k\Omega$

$g_{m1} = g_{m2} = g_m = \sqrt{2k I_D} = \sqrt{2 \times 5 \times 0.5} = 2.236\ mS$

For the gains, see next page:

Half-circuit



$$\frac{v_{d1}}{v_{id}/2} = -g_m R_D \Rightarrow A_{d1} = \frac{v_{d1}}{v_{id}} = -\frac{1}{2} g_m R_D$$

$$\Rightarrow A_{d1} = -8.94 \frac{V}{V}$$

$$\frac{v_{d2}}{-v_{id}/2} = -g_m R_D \Rightarrow A_{d2} = \frac{v_{d2}}{v_{id}} = \frac{1}{2} g_m R_D$$

$$\Rightarrow A_{d2} = 8.94 \frac{V}{V}$$

$$A_d = \frac{v_{d2} - v_{d1}}{v_{id}} = A_{d2} - A_{d1} = 2 \times 8.94 = 17.89 \frac{V}{V}$$

Q3: For the cascode current sink of **Fig. 3**, the parameters are: $k = 400\ \mu A/V^2$, $V_A = 10\ V$, and $V_t = 0.7\ V$. Further, $R_1 = 2.2\ k\Omega$, $R_2 = 1.5\ k\Omega$, and $R_3 = 1.0\ k\Omega$; and the power supply voltage is $V_{DD} = 4.7\ V$. Ignoring the Early effect in DC, calculate the output current i_O, the voltage v_1, and the minimum permissible value of the output voltage v_O. Then, accounting for the Early effect, calculate the internal (or output) resistance of the current sink, as well as the small-signal gain i_o/v_o [$\mu A/V$]. Show all the work, but summarize your findings in **Table 3**.

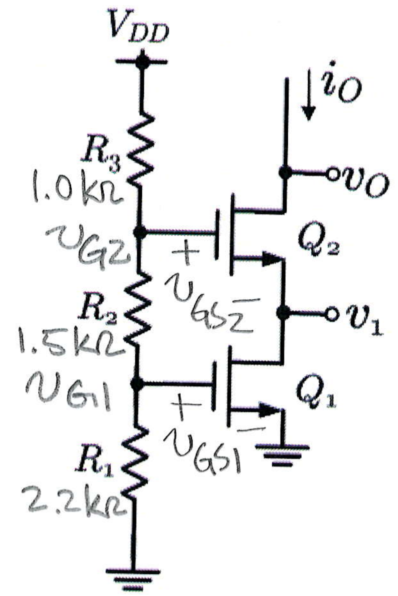


Fig. 3: Cascode current sink of Q3.

Table 3: Results of the circuit of Q3 **[each 5 marks]**.

i_O [mA]	v_1 [V]	v_{O-min} [V]	i_o/v_o [$\mu A/V$]
0.45	1.5	3.0	2.94

$$v_{G1} = \frac{V_{DD}}{R_3+R_2+R_1} R_1 = \frac{4.7}{1.0+1.5+2.2} \times 2.2 = 2.2^V$$

$$v_{G2} = \frac{V_{DD}}{R_3+R_2+R_1}(R_1+R_2) = \frac{4.7}{1.0+1.5+2.2} \times (2.2+1.5) = 3.7^V$$

$$i_{D1} = i_{D2} = \frac{1}{2}k(v_{GS1}-V_t)^2 \quad \text{(ignoring Early effect)}$$

$$\Rightarrow i_O = \frac{1}{2} \times 0.4 \times (2.2-0.7)^2 = \boxed{0.45\ mA}$$

$$v_{GS2} = v_{GS1} \Rightarrow v_{GS2} = 2.2^V \Rightarrow \boxed{v_1 = 3.7^V - 2.2^V = 1.5^V}$$

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Calculation of v_O range

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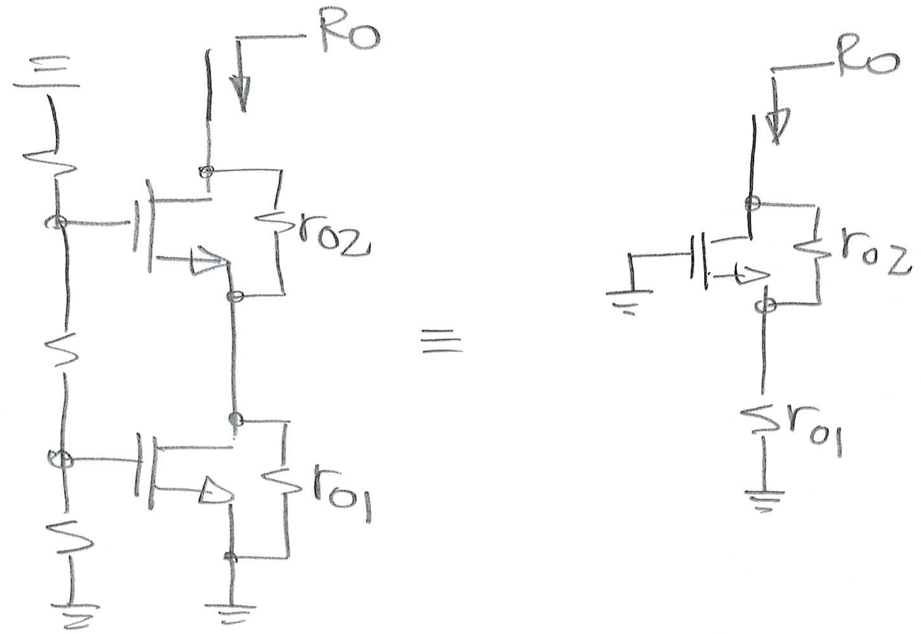
$$v_{DS2} \geq v_{GS2} - V_t$$

$$v_O - v_1 \geq v_{G2} - V_t$$

$$\Rightarrow v_O - 1.5 \geq 2.2 - 0.7$$

$$\Rightarrow \boxed{v_O \geq 3.0^V} \Rightarrow v_{Omin} = 3.0^V$$

Calculation of R_O



$$R_O = r_{o1} + r_{o2} + (g_m r_{o2}) r_{o1}$$

$$r_{o1} = r_{o2} = \frac{V_A}{I_D} = \frac{10}{0.45} = 22.2^{k\Omega}$$

$$g_m = \sqrt{2k_n I_D} = \sqrt{2 \times 0.4 \times 0.45} = 0.6 \text{ mS}$$

$$\Rightarrow R_O = 22.2 + 22.2 + (0.6 \times 22.2) \times 22.2 = 340.1 \text{ k}\Omega$$

$$\Rightarrow \frac{i_O}{v_O} = \frac{1}{R_O} = \frac{1}{340.1} = 0.00294 \text{ mA/V or } \boxed{2.94 \text{ }\mu\text{A/V}}$$

Q4: In the active-loaded Common-Source (CS) amplifier of **Fig. 4**, the MOS devices have the parameters $k = 200\ \mu A/V^2$, $|V_A| = 10\ V$, and $|V_t| = 0.4\ V$. Further, the diodes exhibit an on-state voltages of $0.8\ V$, and the power supply voltage is $V_{DD} = 5.0\ V$. The bias voltage V_{bias} is set in such a way that $V_O = 2.5\ V$.

Calculate the voltage gain v_o/v_i, the output resistance of the amplifier, the minimum and maximum permissible values of the output voltage, and the bias voltage V_{bias}. Summarize your findings in **Table 4**. Show all the work.

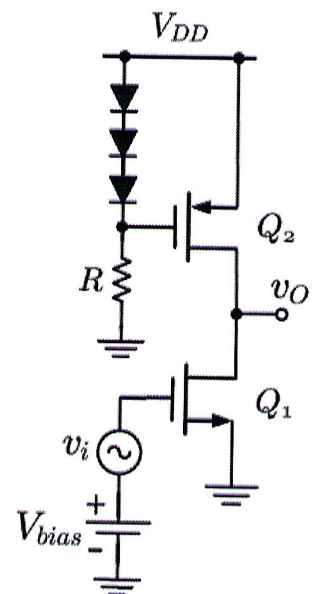


Fig. 4: CS amplifier of Q4.

Table 4: Characteristics of the CS amplifier of **Fig. 4 [each 5 marks]**.

$v_o/v_i\ [V/V]$	$R_{out}\ [k\Omega]$	$v_{O-min}\ [V]$	$v_{O-max}\ [V]$	$V_{bias}\ [V]$
-5.59	12.5	2.0	3.0	2.4

$i_{D1} = i_{D2} \Rightarrow I_{D1} = I_{D2}$. Further, $k_1 = k_2$. Therefore,

$$v_{OV1}^2 \left(1 + \frac{v_{DS1}}{|V_A|}\right) = v_{OV2}^2 \left(1 + \frac{v_{SD2}}{|V_A|}\right)$$

$$\Rightarrow v_{OV1}^2 \times \left(1 + \frac{2.5}{10}\right) = (3 \times 0.8 - 0.4)^2 \left(1 + \frac{5 - 2.5}{10}\right)$$

$$\Rightarrow v_{OV1} = 2.0^V \Rightarrow v_{GS1} - 0.4 = 2.0^V \Rightarrow$$

$$v_{GS1} = 2.4^V \Rightarrow \boxed{V_{bias} = 2.4^V}$$

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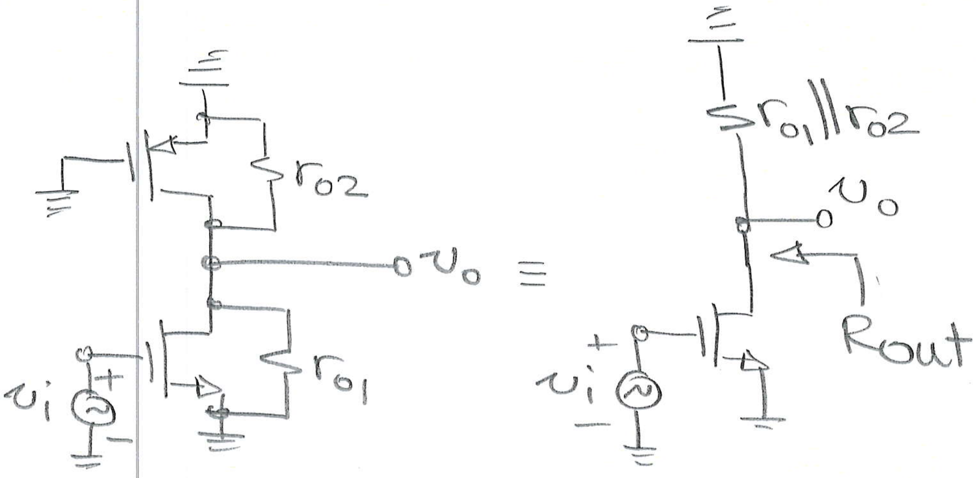
AC equivalent



$$I_{D1} = \frac{1}{2}k(V_{GS1} - V_t)^2\left(1 + \frac{V_{DS1}}{|V_A|}\right)$$

$$= \underbrace{\frac{1}{2} \times 0.2 \times (2.4 - 0.4)^2}_{I_D' = 0.4\,\text{mA}}\left(1 + \frac{2.5}{10}\right) = 0.5\ \text{mA}$$

$$g_{m1} = \sqrt{2k\,I_D} = \sqrt{2 \times 0.2 \times 0.5} = 0.447\ \text{mS}$$

$$r_{o1} = r_{o2} = \frac{|V_A|}{I_D'} = \frac{10}{0.4} = 25\ \text{k}\Omega$$

$$\frac{v_o}{v_i} = -g_{m1}(r_{o1} \| r_{o2}) = -0.447 \times 12.5 = \boxed{-5.59\ \frac{V}{V}}$$

$$R_{out} = r_{o1} \| r_{o2} = \boxed{12.5\ \text{k}\Omega}$$

$$V_{DD} - v_o \geq V_{ov2} \Rightarrow 5 - v_o \geq 2.4 - 0.4 \Rightarrow \boxed{v_o \leq 3.0\,V}$$

$$v_o \geq V_{ov1} \Rightarrow \boxed{v_o \geq 2.4 - 0.4 = 2.0\,V}$$

Q5: Calculate the dc collector currents as well as the open-circuit voltage gain v_0/v_i, input resistance R_{in}, and output resistance R_{out} of the discrete-circuit amplifier of **Fig. 5.** Assume that $\beta = 100$, $V_{BE(on)} = 0.7\ V$, $V_{CEsat} = 0.3\ V$. For dc analysis, you may assume β to be very large. Summarize your results in **Tables 5a and 5b**. Show all the work.

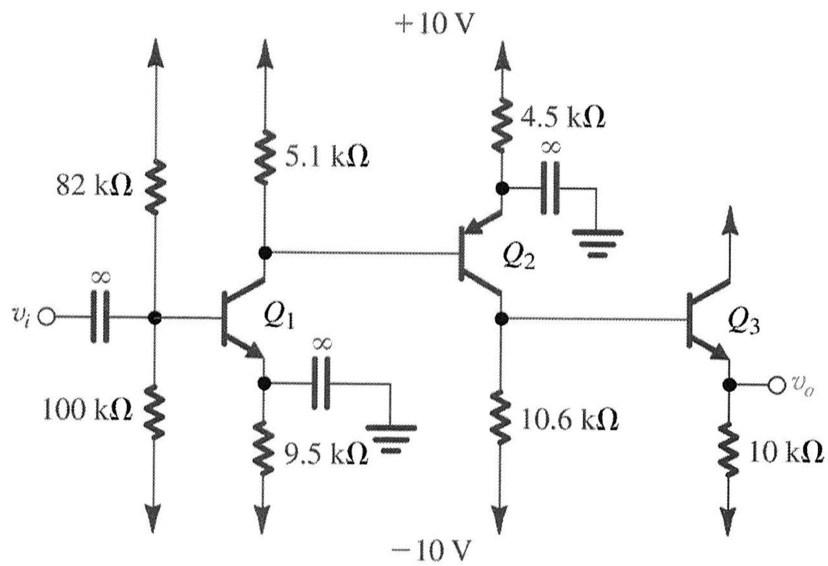


Fig. 5. Discrete-circuit amplifier of Q5.

Table 5a: DC collector currents of the amplifier of **Fig. 5 [each 5 marks]**.

$I_{C1}\ [mA]$	$I_{C2}\ [mA]$	$I_{C2}\ [mA]$
1.08	1.07	1.06

Table 5b: Characteristics of the amplifier of **Fig. 5 [each 5 marks]**.

$v_o/v_i\ [V/V]$	$R_{in}\ [k\Omega]$	$R_{out}\ [k\Omega]$
31053	2.2	0.128

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DC Analysis

$$V_{B1} = \frac{10}{82+100} \times 100 + \frac{-10}{82+100} \times 82 = 0.989^V$$

$$V_{E_1} = 0.989^V - 0.7^V = 0.289^V$$

$$I_{E_1} = \frac{0.289-(-10)}{9.5} = 1.08 \text{ mA} \Rightarrow \boxed{I_{C_1} = 1.08 \text{ mA}}$$

$$V_{C1} = 10^V - 5.1 \times 1.08 = 4.49^V$$

$$V_{E_2} = 4.49^V + 0.7^V = 5.19^V$$

$$I_{E_2} = \frac{10-5.19}{4.5} = 1.07 \text{ mA} \Rightarrow \boxed{I_{C2} = 1.07^{mA}}$$

$$V_{C2} = -10 + 10.6 \times 1.07 = 1.342^V$$

$$V_{E3} = 1.342^V - 0.7^V = 0.642^V$$

$$I_{E3} = \frac{0.642-(-10)}{10} = 1.06 \text{ mA} \Rightarrow \boxed{I_{C3} = 1.06 \text{ mA}}$$

$$\left.\begin{array}{l} V_{CE_1} = 4.49 - 0.289 > 0.3^V \checkmark \\ V_{EC2} = 5.19 - 1.342 > 0.3^V \checkmark \\ V_{CE3} = 10 - 0.642 > 0.3^V \checkmark \end{array}\right\} \text{all transistors in active mode.}$$

The foregoing DC analysis may also be done with β taken into account; the results will then be slightly different (about 10%).

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AC analysis

$g_{m1} = 40 \times 1.08 = 43.2\,mS$

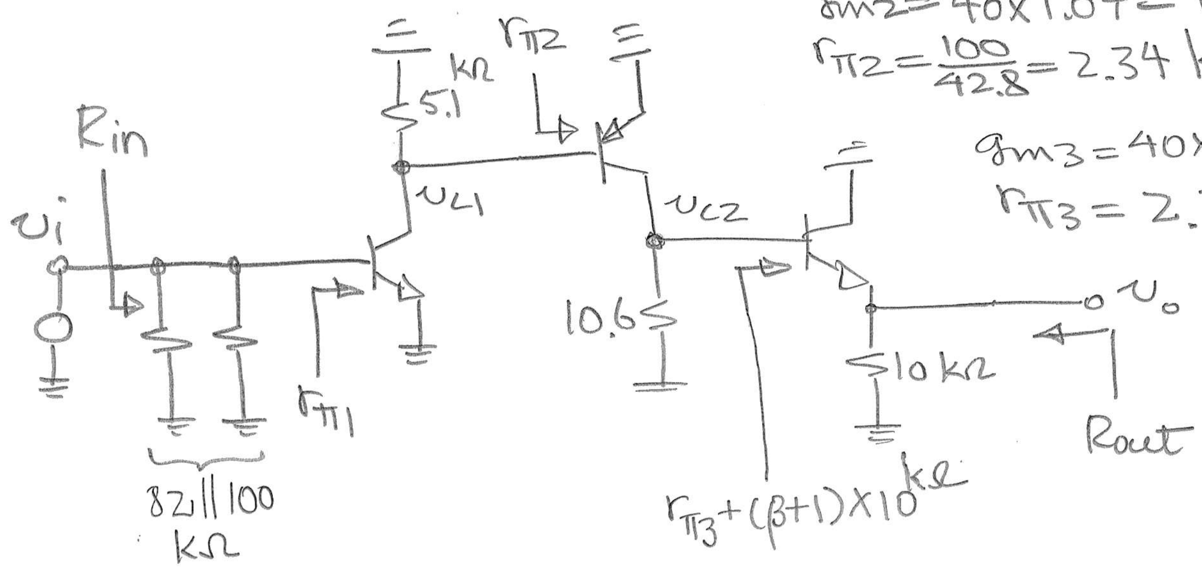
$r_{\pi 1} = \frac{100}{43.2} = 2.31\,k\Omega$

$g_{m2} = 40 \times 1.07 = 42.8\,mS$

$r_{\pi 2} = \frac{100}{42.8} = 2.34\,k\Omega$

$g_{m3} = 40 \times 1.06 = 42.4\,mS$

$r_{\pi 3} = 2.36\,k\Omega$



$$CE: \frac{v_{c1}}{v_i} = -g_{m1}(5.1 \| r_{\pi 2}) = -43.2(5.1\|2.34) = -69.3\ \frac{V}{V}$$

$$CE: \frac{v_{c2}}{v_{c1}} = -g_{m2}\left[10.6 \| (r_{\pi 3} + (\beta+1)\times 10^{k\Omega})\right] = -42.8\times(10.6\|1012.4) = -449\ V/V$$

$$CC: \frac{v_o}{v_{c2}} = \frac{g_{m3}\times 10k\Omega}{1+g_{m3}\times 10k\Omega} = 0.998\ \frac{V}{V}$$

$$\Rightarrow \frac{v_o}{v_i} = -69.3\times -449 \times 0.998 = \boxed{31053\ \frac{V}{V}}$$

$$R_{in} = 82\|100\|r_{\pi 1} = 82\|100\|2.31 = \boxed{2.2\,k\Omega}$$

$$R_{out} = 10 \| \left(\frac{10.6 + r_{\pi 3}}{\beta}\right) = 10\|0.1296 \simeq \boxed{0.128\ k\Omega}$$

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Q6: A source-degenerated CS amplifier with appreciable Early effect, **Fig. 6a,** has been modeled by the two-port circuit of **Fig. 6b**. Assume saturation (active) mode for the MOS transistor and prove that the internal (output) resistance is

$$R_o = r_o + R_s + (g_m r_o)R_s$$

Hint: use the T model, apply a test current, note that the gate current is zero, and formulate the voltage that appears across the test current source.

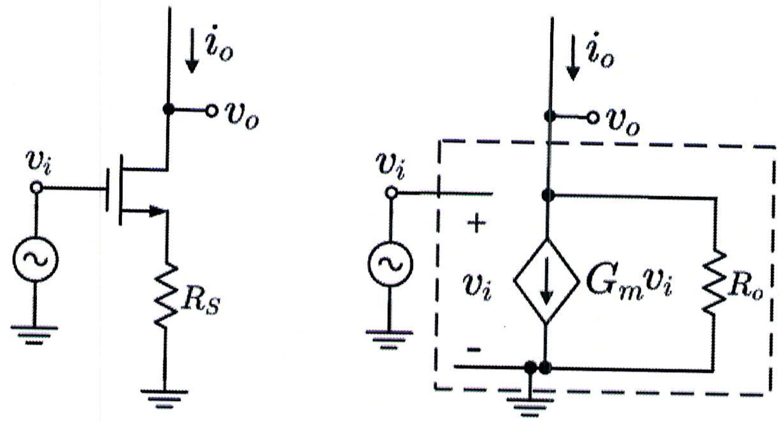

Fig. 6: (a) Common-Source amplifier; (b) its equivalent two-port representation.

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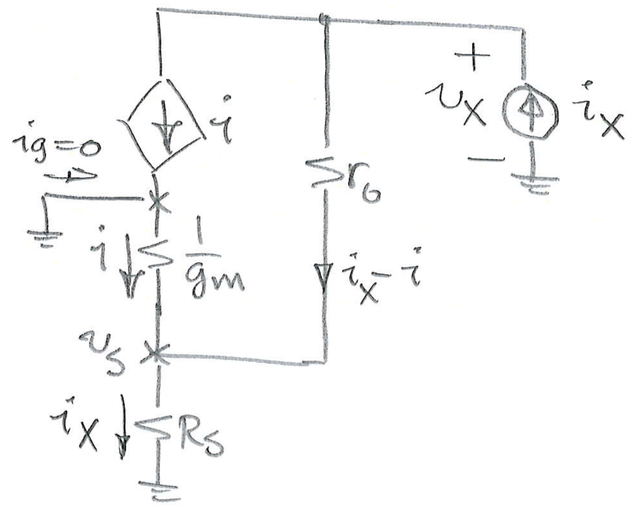


$$v_S = R_S i_X$$

$$i = \frac{0 - v_S}{1/g_m} = -g_m v_S \Rightarrow i = -g_m R_S i_X$$

$$v_X = v_S + r_o(i_X - i) = R_S i_X + r_o i_X - r_o i$$

$$\Rightarrow v_X = (r_o + R_S) i_X + g_m R_S r_o i_X$$

$$\Rightarrow \boxed{R_o = \frac{v_X}{i_X} = r_o + R_S + (g_m r_o) R_S} \checkmark$$

Q7: Assuming ideal diodes, derive and mathematically express the transfer characteristic ($v_I - v_O$ characteristic) of the diode circuit of **Fig. 7a**. Then, plot the transfer characteristic on **Fig. 7b**.

- Each expression 5
- Each line segment 5

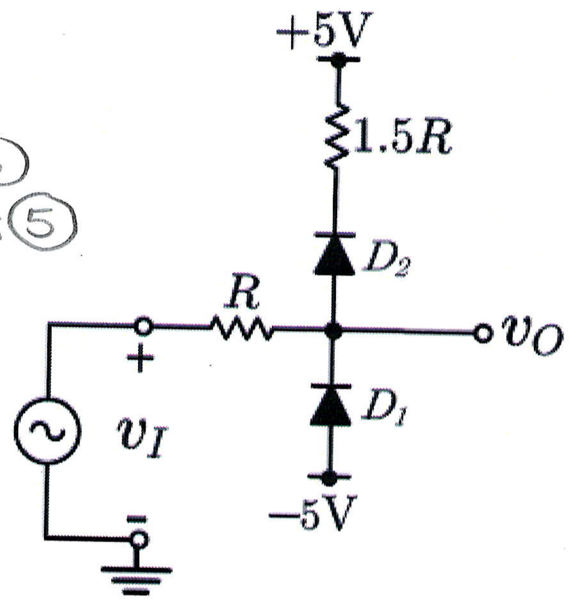


Fig. 7a: Diode circuit of Q7.

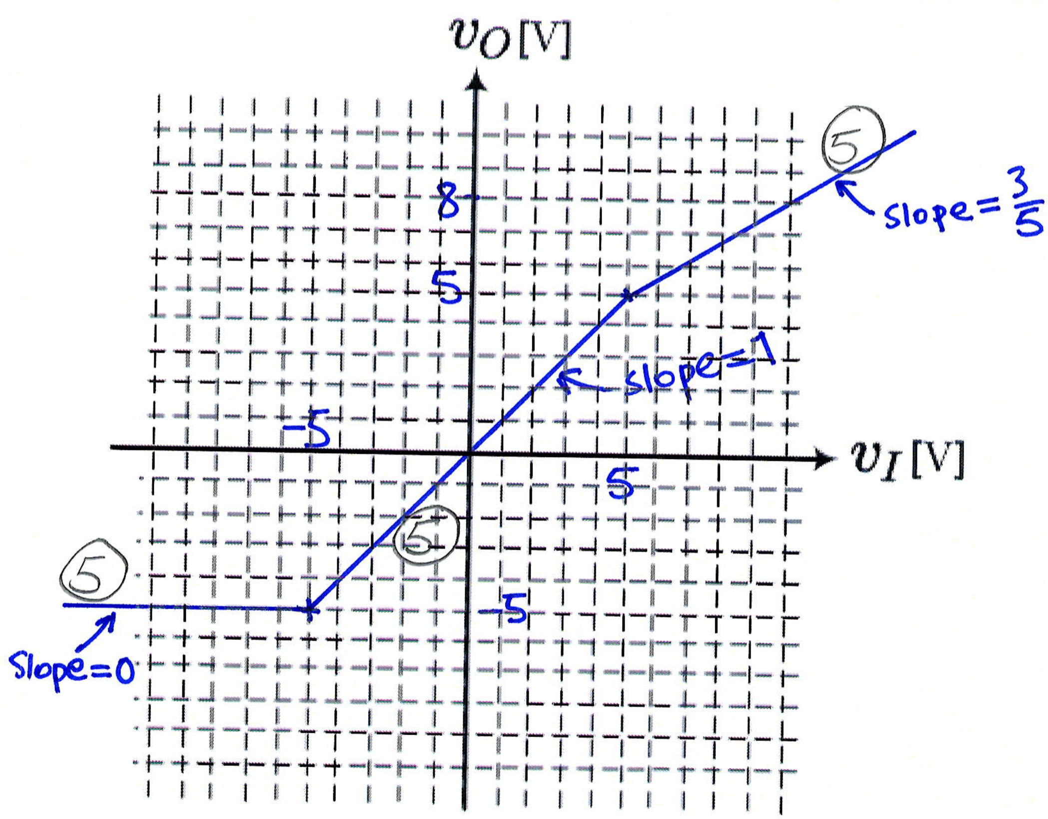
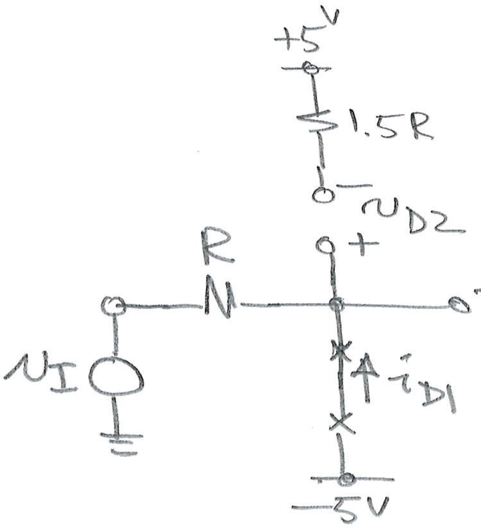


Fig. 7b: Transfer characteristic of the diode circuit of Fig. 7a.

$v_I \to -\infty \Rightarrow D_1: \text{ON}, \ D_2: \text{OFF}$



$$\boxed{v_O = -5^V}$$

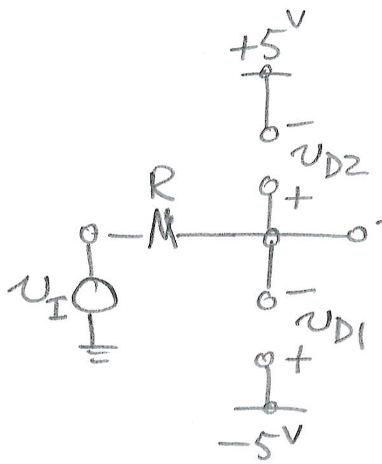
$$i_{D1} = \frac{-5 - v_I}{R} > 0$$

$$\Rightarrow \boxed{v_I < -5^V}$$

$$v_{D2} = v_O - 5 < 0$$

$$\Rightarrow v_O < 5 \ \checkmark$$

$v_I \geq -5^V \Rightarrow D_1: \text{OFF}, \ D_2: \text{OFF}$



$$\boxed{v_O = v_I}$$

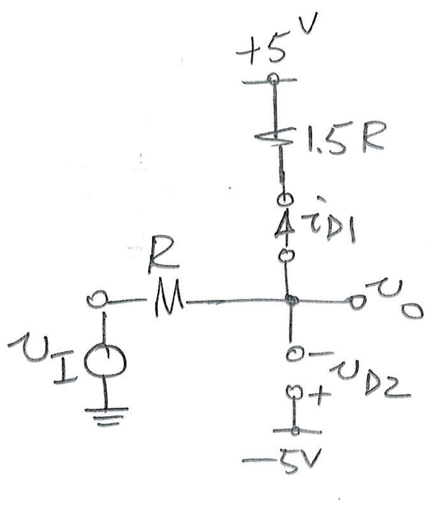
$$v_{D1} = -5 - v_O = -5 - v_I < 0$$

$$\Rightarrow v_I > -5^V \ \checkmark$$

$$v_{D2} = v_O - 5 = v_I - 5 < 0$$

$$\Rightarrow \boxed{v_I < 5^V}$$

$v_I \geq 5^V \Rightarrow D_1: \text{OFF}, \ D_2: \text{ON}$



$$v_O = \frac{v_I}{R + 1.5R} \times 1.5R + \frac{5}{R + 1.5R} \times R$$

$$\Rightarrow \boxed{v_O = \frac{3}{5} v_I + 2}$$

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$$\text{So,} \quad v_O = \begin{cases} -5 & \text{if } v_I \leq -5^V \quad (5) \\ v_I & \text{if } -5^V \leq v_I \leq 5^V \quad (5) \\ \frac{3}{5}v_I + 2 & \text{if } v \geq 5^V \quad (5) \end{cases}$$

The corresponding line segments are plotted on Fig. 7b.

Q8: In the bridge rectifier of **Fig. 8**, the source voltage v_I is a 60-Hz, 12V-Vrms sinusoid. Determine the ***reading of a DC voltmeter*** of the output voltage v_O, under each of the following conditions:

- **(8a)** Only the load R_L is connected (the smoothing capacitor C has been removed);
- **(8b)** Only C is connected (R_L has been removed);
- **(8c)** $R_L = 1.0\ k\Omega$ and $C = 100\ \mu F$;
- **(8d)** $R_L = 1.0\ k\Omega$ and $C = \infty$;
- **(8e)** Same as **(8a)** but with D_3 and D_4 removed; and
- **(8f)** Same as **(8b)** but with D_3 and D_4 removed.

Assume that the diodes are ideal and the meter does not draw any current. Support your answers by calculations and/or explanations. Summarize your results in **Table 8**.

Table 8: results of the circuit of Q8 **[each 5 marks]**.

Answer of (8a)	Answer of (8b)	Answer of (8c)	Answer of (8d)	Answer of (8e)	Answer of (8f)
10.8	17.0	16.3	17.0	5.4	17.0

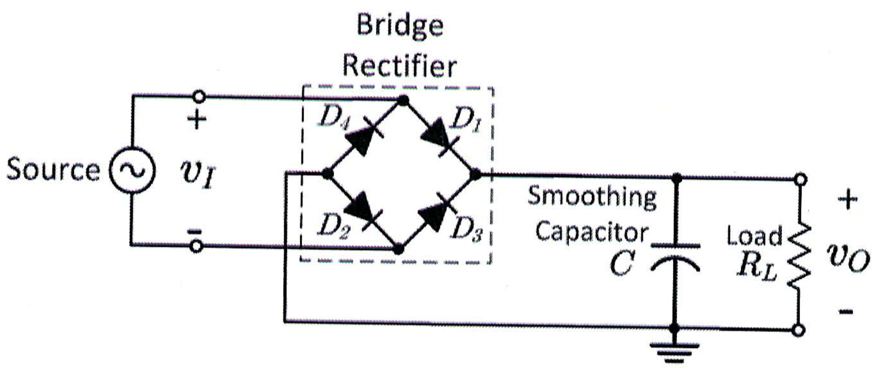

Fig. 8: Bridge rectifier of Q8.

$V_m = 12\sqrt{2} \cong 17^V$

8a) $\overline{v}_O = \frac{2V_m}{\pi} = \frac{2\times 17}{\pi} = 10.8^V$ full-wave rectification

8b) $\overline{v}_O = V_m = 17^V$ (peak detector)

8c) $\overline{v}_O = V_m - \frac{1}{2}V_r$, where

$$V_r = \frac{V_m}{2fRC} = \frac{17}{2\times 60\times 1000\times 100\times 10^{-6}} = 1.42^V$$

$\Rightarrow \overline{v}_O = 17 - \frac{1}{2}\times 1.42 = 16.3^V$

8d) becomes a peak detector similar to 8b $\Rightarrow \overline{v}_O = V_m = 17.0^V$

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8e) $\overline{v}_O = \frac{V_m}{\pi} = \frac{17}{\pi} = 5.4^V$ (half-wave rectifier)

8f) $\overline{v}_O = V_m = 17^V$ (becomes a peak detector)

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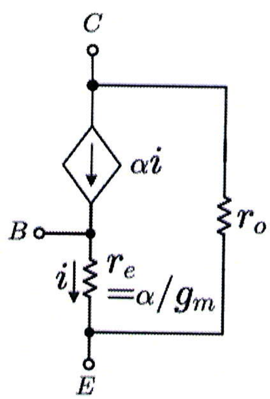
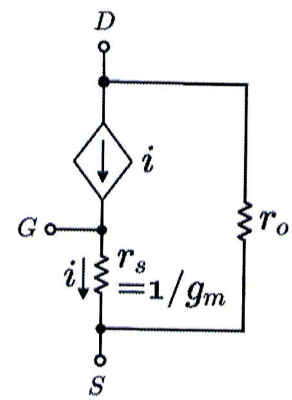
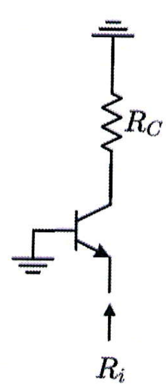
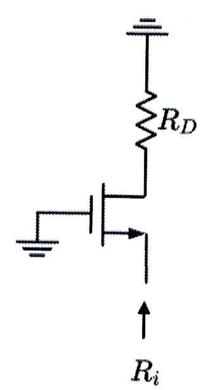
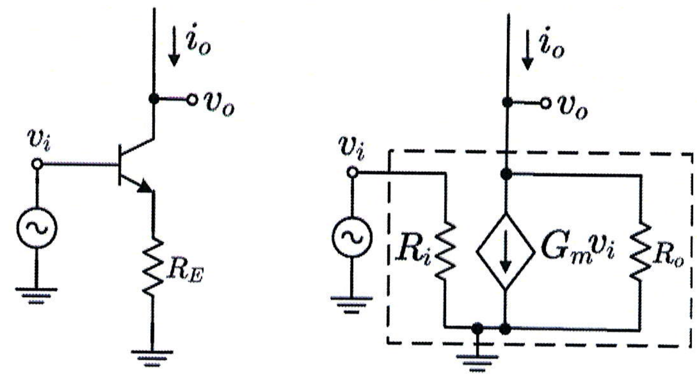
Last updated June 24, 2013—AY

Some Useful Equations and Circuit Configurations (Page 1/2)

BJT	MOS
$i_C = I_s exp\left(\frac{v_{BE}}{V_T}\right)\left(1+\frac{v_{CE}}{V_A}\right); \quad v_{CE} \geq V_{CEsat}$	$i_D = \frac{1}{2} k v_{OV}{}^2 \left(1+\frac{v_{DS}}{V_A}\right); \quad v_{DS} \geq v_{OV}$
$i_C = \beta i_B = \alpha i_E$	$k = k'\left(\frac{W}{L}\right)$
$\alpha = \beta/(\beta+1)$	$k' = \mu C_{ox}$
$g_m = I_C/V_T \approx 40 I_C$	$v_{OV} = (v_{GS} - V_t) \geq 0$
$r_e = \alpha/g_m$	$g_m = 2I_D/V_{OV} = kV_{OV} = \sqrt{2kI_D}$
$r_\pi = (\beta+1)r_e = \beta/g_m$	$r_o = V_A/I_D$
$r_o = V_A/I_C$	

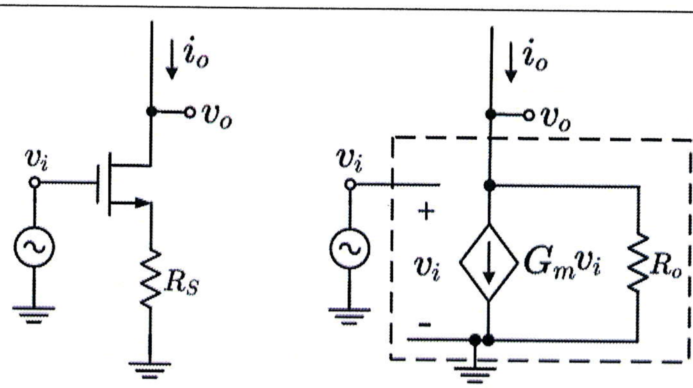
T Model for the BJT	T Model for the MOS
	
	
$R_i = r_e + R_C/(1+g_m r_o)$	$R_i = r_s + R_D/(1+g_m r_o)$

Some Useful Equations and Circuit Configurations (Page 2/2)



(a) (b)

$$R_i = (1 + g_m R_E) r_\pi = r_\pi + \beta R_E$$
$$G_m = g_m / (1 + g_m R_E)$$
$$R_o = [1 + g_m (r_\pi || R_E)] r_o$$



(a) (b)

$$G_m = g_m / (1 + g_m R_S)$$
$$R_o = r_o + R_S + g_m r_o R_S \approx g_m r_o R_S$$