Ryerson University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

ELE 202
Electric Circuit Analysis
LAB COVER PAGE for **Part I** submission.

Lab #:	3	**Lab Title:**	Nodal & Mesh Analysis

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Section #:	11
Submission date and time:	1/3/2023 - 15:00
Due date and time:	1/3/2023 - 15:00

Document submission for Part I:

- A completed and signed "COVER PAGE – **Part I**" has to be included with your submission. The report will not be graded if the signed cover page is not included.
- Your completed handwritten pages of **Section 4.0** should be scanned (via a scanner or phone images), together with the required MultiSIM images. **Note:** *MultiSIM results must be generated using the Department's licensed version of MultiSIM, and the captured screenshots should show your name (at the center-top) and the timestamp (at the bottom-right corner of your screen).*
- Collate and create a ***.pdf*** or ***.docx*** file of the above, and upload it via D2L **any time prior to the start of your scheduled lab**. Upload instructions are provided on D2L.

Zero marks will be assigned for the entire lab if this Part I is not submitted prior to your scheduled lab.

**By signing above, you attest that you have contributed to this submission and confirm that all work you have contributed to this submission is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: www.ryerson.ca/senate/current/pol60.pdf.*

Pre lab 3

Date: _____

a (i) $E = IR$

$$\frac{15}{3.3+2.2+1} = I = 2.31\,mA$$

$V_a = 15\,V$

$V_d = 0\,V$

$V_b = 15 - (1)(2.307)$

$= 12.693\,V$

$V_{cd} = V_c - V_d$

$= 7.617\,V$

$V_c = V_b - IR_2$

$= 12.693 - 2.307(2.2)$

$= 7.617\,V$

$V_{ab} = V_a - V_b$

$= 15 - 12.693 = 2.307\,V$

$V_{bc} = V_b - V_c$

$= 12.693 - 7.617 = 5.076\,V$

ii) $I = \frac{15}{3.3+2.2+1} = 2.307\,mA$

$V_c = 0V$

$V_d = V_c - IR_3$

$= 0 - 2.307(3.3)$

$= -7.613V$

$V_a = V_d + 15$

$= 7.387$

$V_b = V_c + IR_2$

$= 0 + 2.307 \times 2.2$

$= 5.075V$

$V_{ab} = V_a - V_b$

$= 7.387 - 5.075$

$= 2.312\,V$

$V_{cd} = V_c - V_d$

$= 7.613\,V$

$V_{bc} = V_b - V_c$

$= 5.075\,V$

iv) Current and P.d across resistors remain same. Because potential is dependant on reference assumed but P.d is independent of potential assumed.

Date: _____

b) $V_a = 15\ V$

$$\frac{15 - V_b}{2.2} + \frac{15 - V_c}{1} = 0$$

$$-V_b - 2.2V_c = -15 = 15 \times 2.2$$

$$V_b + 2.2V_c = 48 \quad \text{—(i)}$$

$$\frac{V_b - 15}{2.2} + \frac{V_b - V_c}{5.1} + \frac{V_b}{3.3} = 0$$

$$V_b\left[\frac{1}{2.2} + \frac{1}{5.1} + \frac{1}{3.3}\right] - \frac{V_c}{5.1} = 15$$

$V_b = 22.43 \qquad V_c = 11.619$

$I_x = 6.796\ mA$

$-15 + V_x + V_c = 0$

$V_x = 3.381$

KVL mesh 1a

$$-15 + 2.2(I_A - I_C) + 3.3(I_A - I_B) = 0$$

$$I_A(5.5) - 3.3I_B - 2.2I_C = 15 \quad -i$$

$$3.3(I_B - I_A) + 5.1(I_B - I_C) + I_B = 0$$

$$-3.3I_A + 9.4I_B - 5.1I_C = 0 \quad -ii$$

$$-2.2I_A - 5.1I_B + 8.3I_C \quad \text{— iii}$$

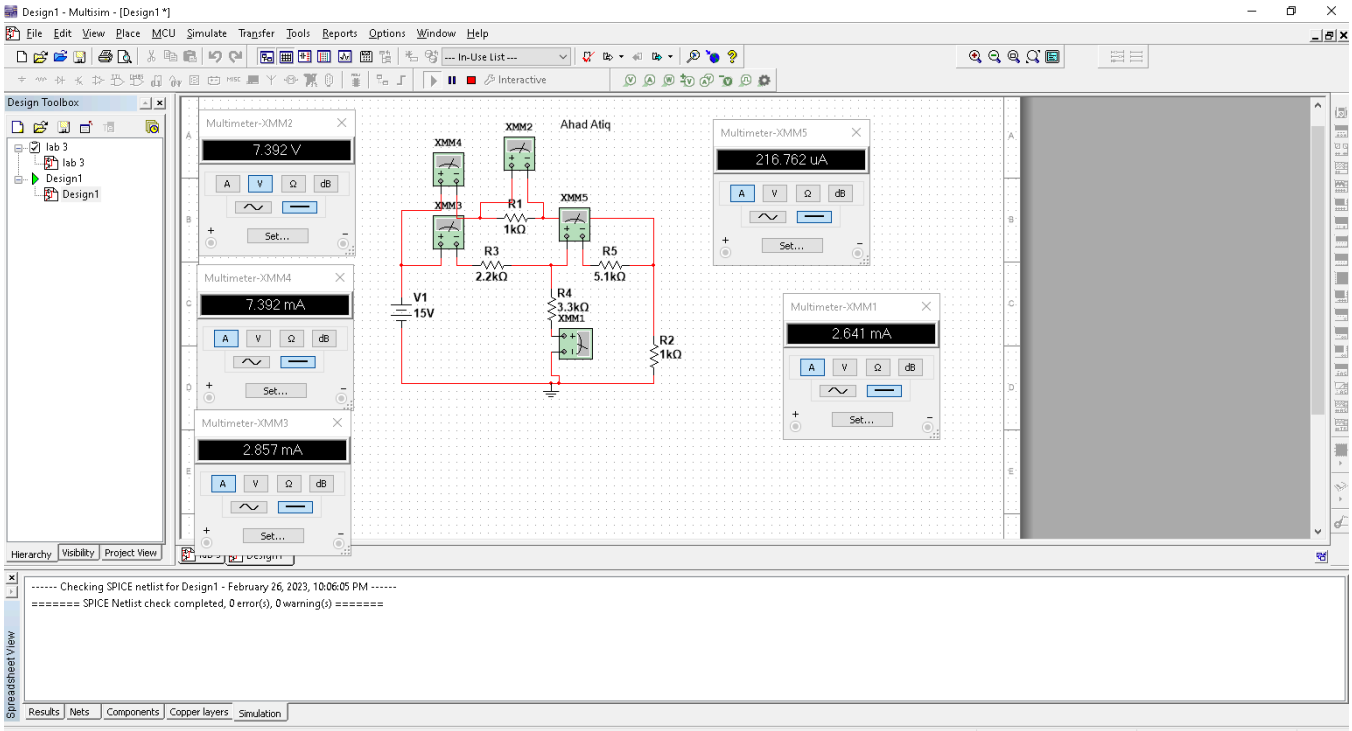
$I_A = 10\ mA$	$I_B = 7.6\ mA$	$I_C = 7.3\ mA$	$I_x = 2.4\ mA$
$I_1 = 2.7\ mA$	$I_2 = 0.3\ mA$	$I_3 = 7.3\ mA$	$V_x = 7.3$

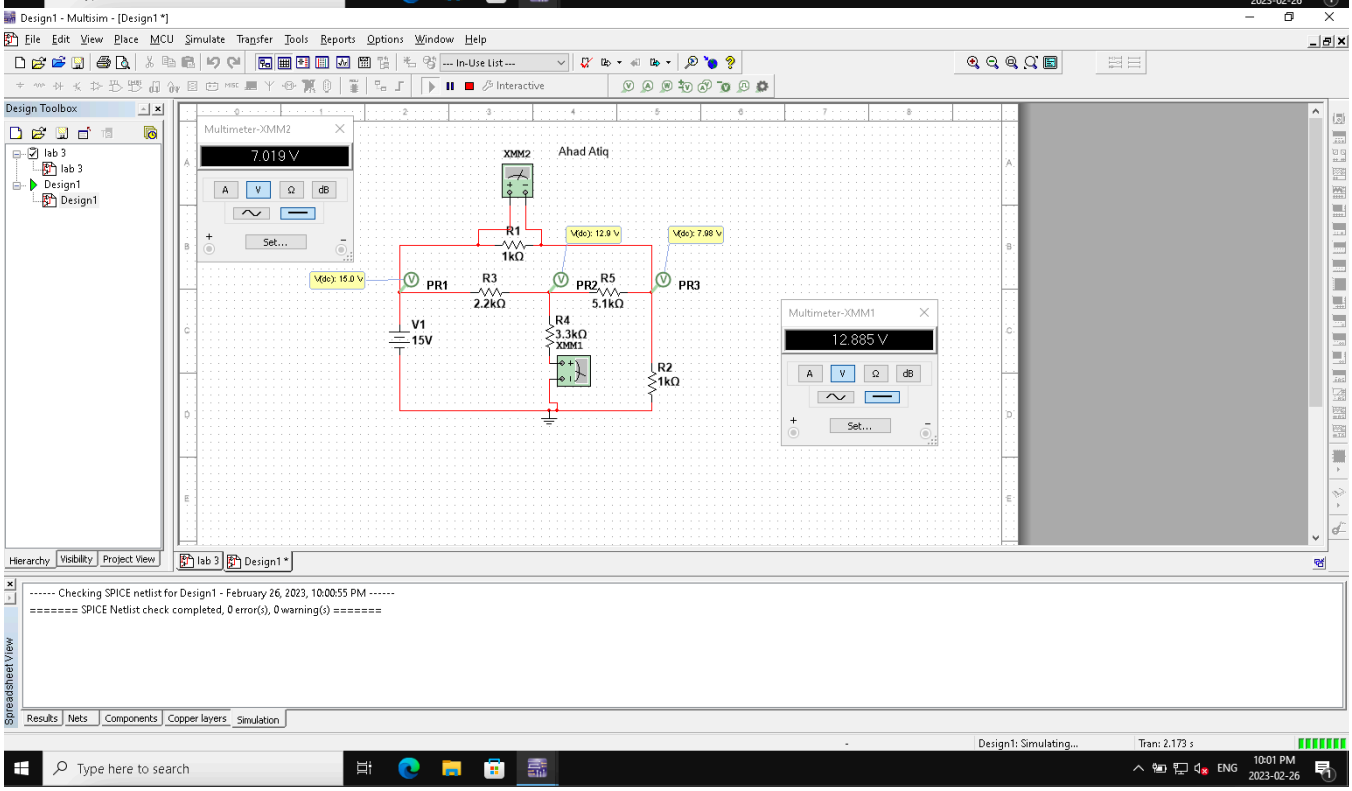
		Using *Reference* Node "d"	Using *Reference* Node "c"
I (mA)	Theoretical value =>	2.307	2.307
	MultiSIM value =>	2.308	2.308
V_a (Volts)	Theoretical value =>	15	7.387
	MultiSIM value =>	15	7.39
V_b (Volts)	Theoretical value =>	12.693	5.075
	MultiSIM value =>	12.693	5.075
V_c (Volts)	Theoretical value =>	7.617	0
	MultiSIM value =>	7.617	0
V_d (Volts)	Theoretical value =>	0	-7.613
	MultiSIM value =>	0	-7.62
V_{ab} (Volts)	Theoretical value =>	2.307	2.312
	MultiSIM value =>	2.308	2.308
V_{bc} (Volts)	Theoretical value =>	5.076	5.075
	MultiSIM value =>	5.076	5.077
V_{cd} (Volts)	Theoretical value =>	7.617	7.613
	MultiSIM value =>	7.62	7.615

Table 2.0: Theoretical and MultiSIM results of the Figure 2.0 circuits

		Nodal Analysis	***Mesh*** Analysis
V_a (Volts)	Theoretical value =>	15	
	MultiSIM value =>	15	
V_b (Volts)	Theoretical value =>	22.43	
	MultiSIM value =>	12.9	
V_c (Volts)	Theoretical value =>	11.619	
	MultiSIM value =>	7.98	
I_A (mA)	Theoretical value =>		10
	MultiSIM derived =>		10
I_B (mA)	Theoretical value =>		7.6
	MultiSIM derived =>		7.6
I_C (mA)	Theoretical value =>		7.3
	MultiSIM derived =>		7.3
I_X (mA)	Theoretical value =>	6.796	2.4
	MultiSIM value =>	6.8	2.6
V_X (Volts)	Theoretical value =>	3.381	7.3
	MultiSIM value =>	7.09	7.39

I_1 (mA)	Theoretical value =>		2.7
	MultiSIM value =>		2.61
I_2 (mA)	Theoretical value =>		0.3
	MultiSIM value =>		0.21
I_3 (mA)	Theoretical value =>		7.3
	MultiSIM value =>		7.39


Design1 - Multisim - [Design1 *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Design Toolbox
lab 3
lab 3
Design1
Design1
Multimeter-XMM2
7.392 V
Multimeter-XMM4
7.392 mA
Multimeter-XMM3
2.857 mA
Multimeter-XMM5
216.762 uA
Multimeter-XMM1
2.641 mA
Ahad Atiq
XMM4
XMM2
XMM3
XMM5
XMM1
R1
1kΩ
R3
2.2kΩ
R5
5.1kΩ
R4
3.3kΩ
R2
1kΩ
V1
15V
Set...
Hierarchy
Visibility
Project View
------ Checking SPICE netlist for Design1 - February 26, 2023, 10:06:05 PM ------
======= SPICE Netlist check completed, 0 error(s), 0 warning(s) =======
Spreadsheet View
Results
Nets
Components
Copper layers
Simulation
Design1: Simulating...
Tran: 0.786 s
Type here to search
ENG
10:06 PM
2023-02-26


Design1 - Multisim - [Design1 *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Design Toolbox
lab 3
lab 3
Design1
Design1
Multimeter-XMM2
7.019 V
Multimeter-XMM1
12.885 V
Ahad Atiq
XMM2
R1
1kΩ
V(dc): 12.9 V
V(dc): 7.98 V
V(dc): 15.0 V
PR1
PR2
PR3
R3
2.2kΩ
R5
5.1kΩ
R4
3.3kΩ
XMM1
R2
1kΩ
V1
15V
Set...
Hierarchy
Visibility
Project View
lab 3
Design1 *
------ Checking SPICE netlist for Design1 - February 26, 2023, 10:00:55 PM ------
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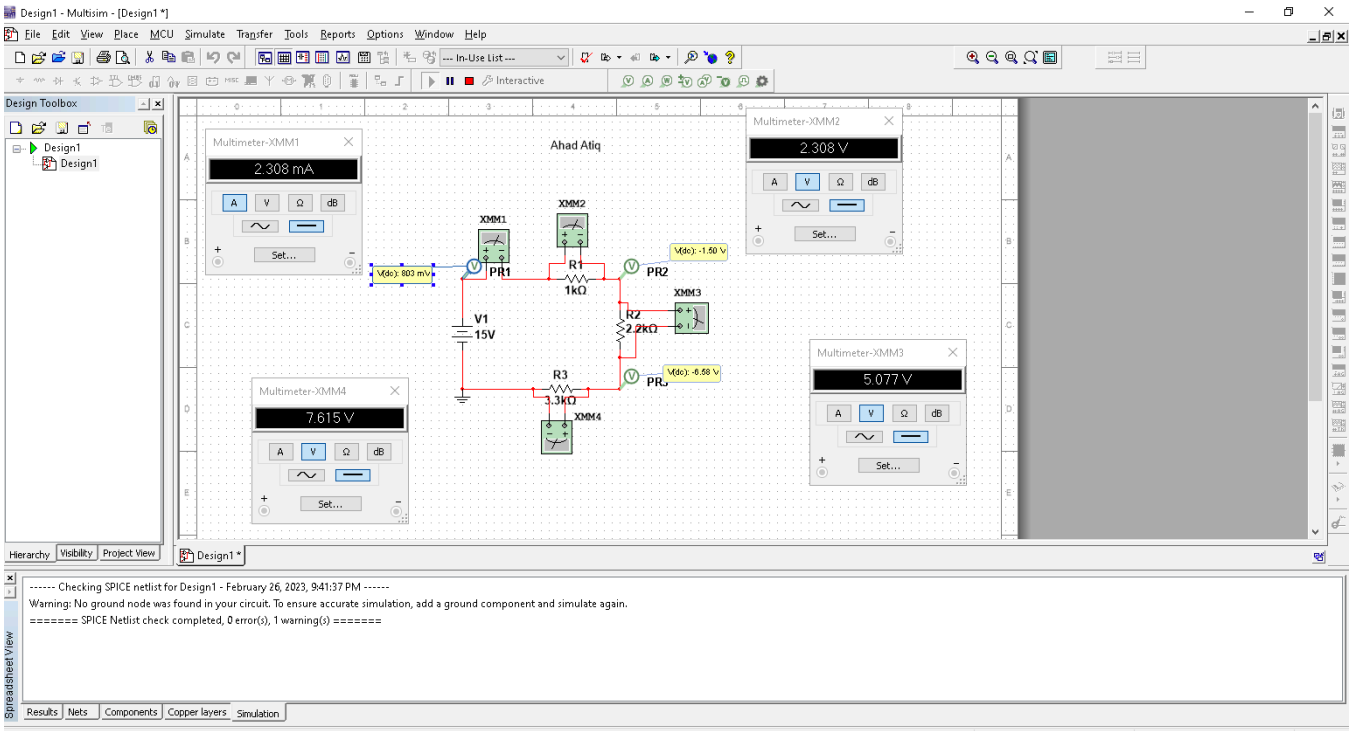
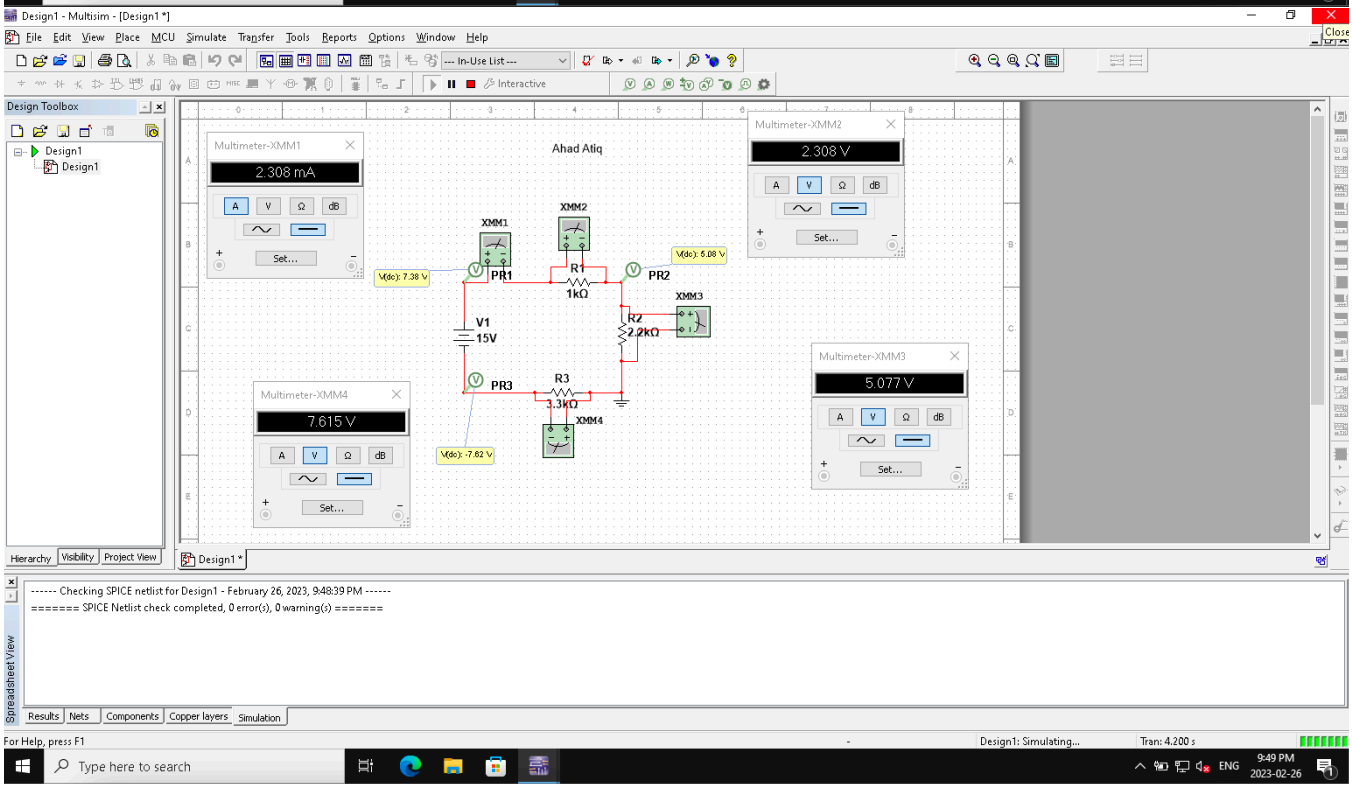
Spreadsheet View
Results
Nets
Components
Copper layers
Simulation
Design1: Simulating...
Tran: 2.173 s
Type here to search
ENG
10:01 PM
2023-02-26


Design1 - Multisim - [Design1 *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Design Toolbox
Design1
Design1
Multimeter-XMM1
2.308 mA
Multimeter-XMM2
2.308 V
Ahad Atiq
XMM1
XMM2
R1
1kΩ
PR1
PR2
V1
15V
R2
2.2kΩ
XMM3
R3
3.3kΩ
XMM4
Multimeter-XMM3
5.077 V
Multimeter-XMM4
7.615 V
Set...
Hierarchy
Visibility
Project View
Design1 *
------ Checking SPICE netlist for Design1 - February 26, 2023, 9:41:37 PM ------
Warning: No ground node was found in your circuit. To ensure accurate simulation, add a ground component and simulate again.
======= SPICE Netlist check completed, 0 error(s), 1 warning(s) =======
Spreadsheet View
Results
Nets
Components
Copper layers
Simulation
For Help, press F1
Design1: Simulating...
Tran: 26.044 s
Type here to search
ENG
9:45 PM
2023-02-26


Design1 - Multisim - [Design1 *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Design Toolbox
Design1
Design1
Multimeter-XMM1
2.308 mA
Multimeter-XMM2
2.308 V
Ahad Atiq
XMM1
XMM2
R1
1kΩ
PR1
PR2
V1
15V
R2
2.2kΩ
XMM3
PR3
R3
3.3kΩ
XMM4
Multimeter-XMM3
5.077 V
Multimeter-XMM4
7.615 V
Set...
Hierarchy
Visibility
Project View
Design1 *
------ Checking SPICE netlist for Design1 - February 26, 2023, 9:48:39 PM ------
======= SPICE Netlist check completed, 0 error(s), 0 warning(s) =======
Spreadsheet View
Results
Nets
Components
Copper layers
Simulation
For Help, press F1
Design1: Simulating...
Tran: 4.200 s
Type here to search
ENG
9:49 PM
2023-02-26