Solution & Marking Scheme

Ryerson University
Department of Electrical and Computer Engineering
ELE404 (Electronic Circuits I)
Midterm Examination (W2013)
February 2013
Duration: 100 minutes
Examiner: Prof. A. Yazdani

Name:...
[Print Last Name] [Print First Name]

Student No:.......................... Section:....

NOTES

1. This is a closed-book examination. No aids other than basic calculators are permitted.

2. The examination paper is comprised of **FOUR QUESTIONS**, *each* question worth as indicated in the following Table. The entire examination is worth *100* marks.

Question #	Maximum Mark	Mark Earned
1	**25**	
2	**25**	
3	**25**	
4	**25**	
Total	100	

3. Answer all questions in the booklet, within the blank spaces provided under each question in this booklet. Use the reverse if needed.

4. ***No Questions to be asked during the examination***. *If in doubt about any question, clearly state your assumptions in answering the question.*

5. Part marks for an answer will only be given if the *correct methodology* is clearly shown.

6. **DO NOT DETACH** any pages from this booklet.

7. Please **WRITE YOUR FINAL ANSWER IN INK.**

Q1: **Fig. 1a** shows the cascade connection of a voltage amplifier and a current amplifier. Provide expressions for the open-circuit voltage gain A_{vo}, input resistance R_i, and output resistance R_o of an equivalent voltage amplifier, i.e., **Fig. 1b**.

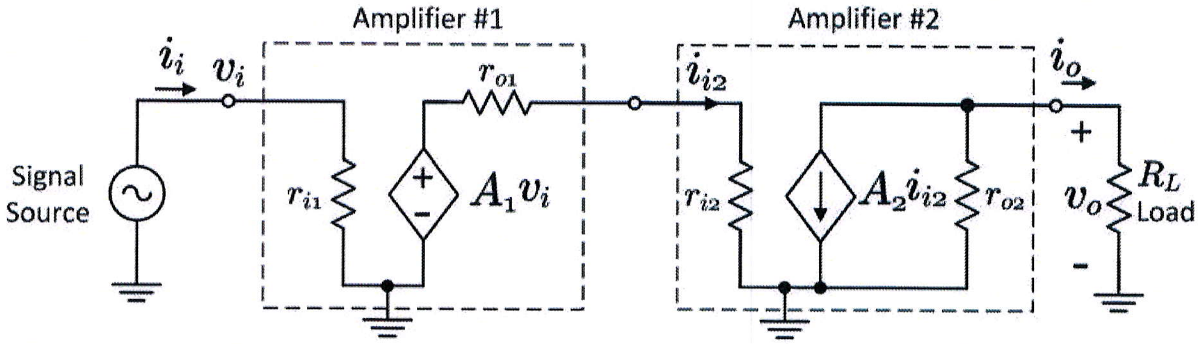

Fig. 1a: cascaded amplifiers of Q1.

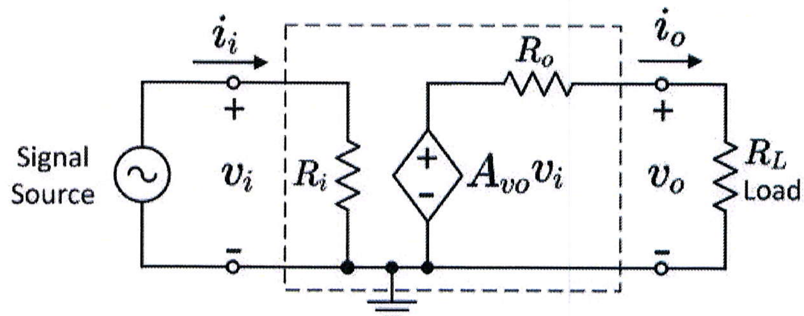

Fig. 1b: voltage amplifier equivalent to the cascaded amplifiers of Fig. 1a.

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Open-circuit voltage gain

$R_L = \infty$; $v_o = A_{vo} v_i \Rightarrow \frac{v_o}{v_i} = A_{vo}$ if $R_L = \infty$

But ;

$v_o = -A_2 i_{i2} r_{o2} \Rightarrow \frac{v_o}{i_{i2}} = -A_2 r_{o2}$ (1)

$i_{i2} = \frac{A_1 v_i}{r_{o1}+r_{i2}} \Rightarrow \frac{i_{i2}}{v_i} = \frac{A_1}{r_{o1}+r_{i2}}$ (2)

$(1)\times(2) \Rightarrow \frac{v_o}{i_{i2}} \times \frac{i_{i2}}{v_i} = \frac{v_o}{v_i} = \boxed{-A_1 A_2 \left(\frac{r_{o2}}{r_{o1}+r_{i2}}\right)}$

15

Input resistance

$\boxed{R_i = r_{i1}}$ from inspection and recognition of the fact that the input resistance is the resistance that sits between the input terminal and the ground.

5

Output resistance

$\boxed{R_o = r_{o2}}$ from inspection and recognition of the fact that it is the resistance that sits between the output terminal and the ground, if $v_i = 0$.

In ourcase, if $v_i = 0$, then i_{i2} and, therefore, $A_2 i_{i2}$ are zero. Hence, the current source acts as an open circuit and leaves r_{o2} as the only element between the output terminal and the ground.

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Q2: In the circuit of **Fig. 2**, the capacitor may be assumed to be very large and the time function of the input signal is $v_S = 5 + 9\cos(\omega t)$ $[V]$. Determine the time function of the input voltage v_I and that of the output voltage v_O. The parameters are $R_s = 1.8\ k\Omega$, $R_1 = 12\ k\Omega$, $R_2 = 18\ k\Omega$, and $V_{CC} = 15\ V$ [***hint:*** regard v_S as the series connection of a dc source $V_S = 5\ V$ and a sinusoidal source $v_s = 9\cos(\omega t)$].

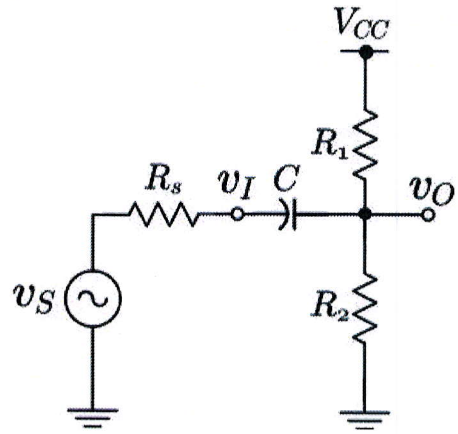
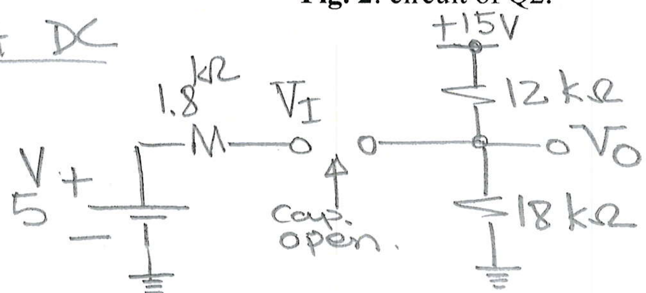


Fig. 2: circuit of Q2.

Circuit at DC

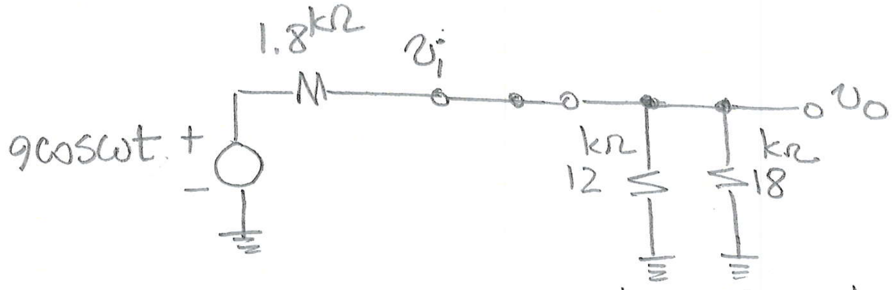


Methodology (this or any other method) 15

$V_I = 5^V$ (1)

$V_O = \frac{15}{12+18} \times 18 = 9^V$ (2)

Circuit at AC



$12 \| 18 = 7.2^{k\Omega}$

$v_i = v_o = \frac{9\cos\omega t}{1.8 + 7.2} \times 7.2 = 7.2\cos\omega t$ (3)

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Complete waveforms

(1) & (3) $\boxed{v_I = 5 + 7.2\cos\omega t}$ 5

(2) & (3) $\boxed{v_O = 9 + 7.2\cos\omega t}$ 5

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Q3: In the diode circuit of **Fig. 3**, the diodes may be assumed to be ideal, $V_x = 10\ V$, $I_x = 4\ mA$, $R_1 = 1\ k\Omega$, and $R_2 = 2\ k\Omega$. Showing all the work, determine the conduction states ("on" or "off") of the diodes, and calculate the voltages V_1, V_2, V_3, and V_4. Summarize your findings in **Table 3**.

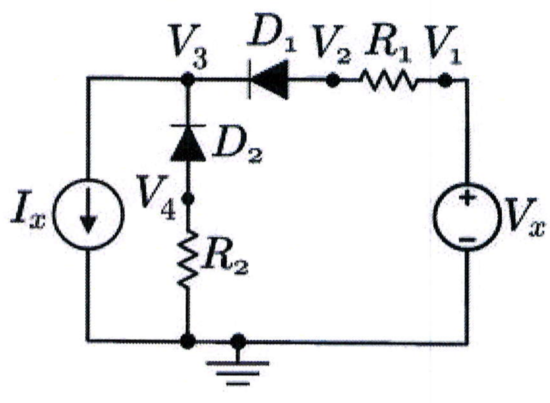

Fig. 3: diode circuit of Q3.

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Each 2.5 marks

Table 3: results of the circuit of Q3

D_1	D_2	V_1 [V]	V_2 [V]	V_3 [V]	V_4 [V]
ON	OFF	10	6	6	0

Systematically, one can start testing the following set of states, one by one, until the right one is found.

#	D1	D2
1	ON	ON
2	ON	OFF
3	OFF	ON
4	OFF	OFF

We demonstrate that state #2 (D1:ON, D2:OFF) is the only possible state; all the other states are not viable.

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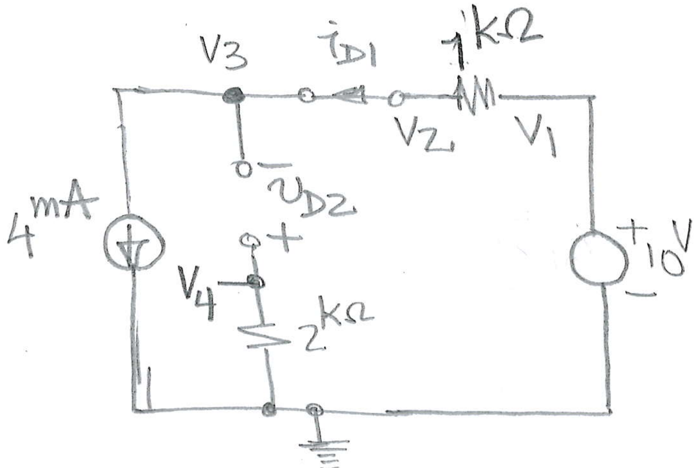
Assume D_1: ON, D_2: OFF



$V_1 = 10^V$, ; $V_3 = V_2 = 6^V$

$V_2 = 10^V - 1^{k\Omega} \times 4^{mA} = 6^V$; $V4 = 0$

$i_{D1} = 4mA > 0$ ✓

$v_{D2} = V4 - V3 = 0 - 6 = -6^V < 0$ ✓

Mark Breakdown

- Correct states supported by checking criteria (15)
- Correct values for V_1 through V_4 (10) (each 2.5 marks)

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Q4: In the Common-Emitter (CE) amplifier of **Fig. 4**, $R_1 = 68\ k\Omega$, $R_2 = 33\ k\Omega$ $R_3 = 3.9\ k\Omega$, $R_4 = 4.7\ k\Omega$, $R_S = 0.6\ k\Omega$, $R_L = 10\ k\Omega$, $\beta = 200$, $V_{BE} = 0.7\ V$, $V_{CEsat} = 0.3\ V$, and $V_{CC} = +15\ V$. The capacitances may be assumed to be very large, and the Early effect is negligible.

First, demonstrate that the transistor is in the active mode when the signal is zero. Then, calculate the gain v_o/v_i, the input resistance r_i, the overall gain v_o/v_s, and the maximum permissible peak-to-peak value of v_i for which v_o remains undistorted. Summarize your findings in **Table 4**.

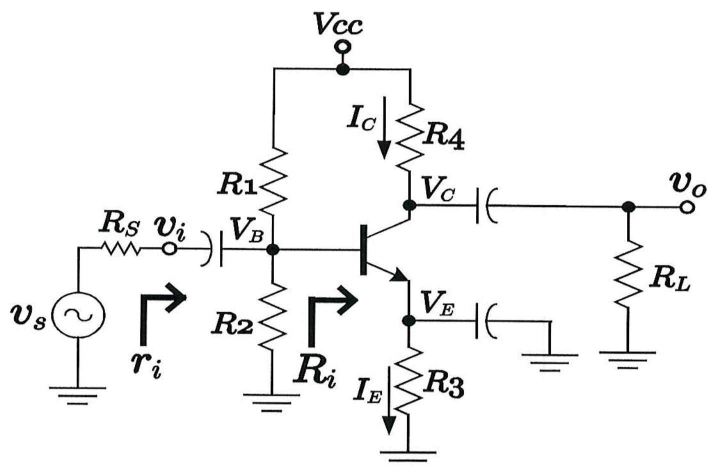

Fig. 4: Common-Emitter amplifier of Q4.

Table 4: results for the amplifier of Fig. 4.

v_o/v_i [V/V]	r_i [kΩ]	v_o/v_s [V/V]	**maximum permissible peak-to-peak swing of v_i**
−138.3	3.82	−119.5	0.073V

Active mode proof : 5

Each value 5 : 4x5 = 20

Full mark requires supporting calculations, similar to those shown on the following pages.

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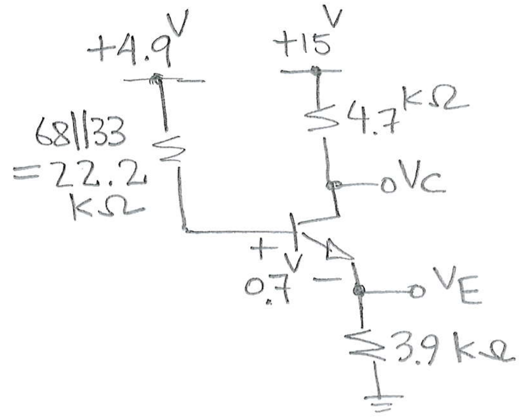
Circuit at DC



KVL: $4.9 - 22.2\,I_B - 0.7 - 3.9\,I_E = 0$

$I_B = \frac{I_C}{\beta} = \frac{I_C}{200}$; $I_E = \frac{\beta+1}{\beta} I_C = \frac{201}{200} I_C$

$\Rightarrow 4.9 - 22.2 \times \frac{1}{200} I_C - 0.7 - 3.9 \times \frac{201}{200} I_C = 0 \Rightarrow \boxed{I_C = 1.07\ mA}$

$I_E = \frac{201}{200} I_C = \frac{201}{200} \times 1.07 = \boxed{1.075\ mA}$

$V_C = 15^V - 4.7^{k\Omega} \times 1.07^{mA} = \boxed{9.97^V}$

$V_E = 3.9^{k\Omega} \times 1.075^{mA} = \boxed{4.19^V}$

$V_{CE} = 9.97 - 4.19 = 5.78^V > 0.3^V$ active mode ✓

Very similar results would be obtained if the base current was ignored. In that case:

$I_B = 0 \Rightarrow V_B = \frac{15}{68+33} \times 33 = 4.9^V \Rightarrow V_E = 4.9 - 0.7 = 4.2^V$

$\Rightarrow I_E = \frac{4.2}{3.9} = 1.077\ mA \Rightarrow I_C \simeq 1.077\ mA$, etc.

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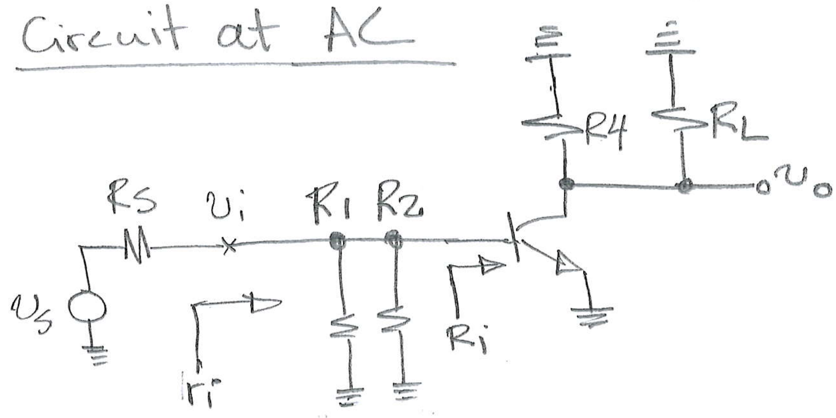
Circuit at AC



$$\frac{v_o}{v_i} = \frac{-\alpha(R_4 \| R_L)}{r_e + \cancel{R_E}} = \frac{-\alpha(R_4 \| R_L)}{r_e}$$

$$g_m \simeq 40 I_C = 42.8 \text{ mS}$$

$$\alpha = \frac{\beta}{\beta+1} = \frac{200}{201} = 0.995$$

$$r_e = \frac{\alpha}{g_m} = \frac{0.995}{42.8} = 0.023 \text{ k}\Omega$$

$$\Rightarrow \boxed{\frac{v_o}{v_i} = \frac{-0.995 \times (4.7 \| 10)}{0.023} = -138.3 \ \frac{V}{V}}$$

$$R_i = r_\pi + (\beta+1)R_E = (\beta+1)(r_e + \cancel{R_E}) = 201 \times 0.023 \text{ k}\Omega$$
$$= 4.62 \text{ k}\Omega$$

$$\boxed{r_i = R_1 \| R_2 \| R_i = 68 \| 33 \| 4.62 = 3.82 \text{ k}\Omega}$$

$$v_i = \frac{v_s}{R_s + r_i} r_i \Rightarrow \frac{v_i}{v_s} = \frac{r_i}{R_s + r_i} = \frac{3.82}{0.6 + 3.82} = 0.864 \ \frac{V}{V}$$

$$\boxed{\frac{v_o}{v_s} = \frac{v_o}{v_i} \times \frac{v_i}{v_s} = -138.3 \times 0.864 = -119.5 \ \frac{V}{V}}$$

Input Voltage Swing

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From the high side, v_C can swing up to $V_{CC} = 15^V$. This corresponds to a swing of $15 - 9.97 = 5.03^V$

From the low side, v_C can swing down to $V_E + V_{CEsat}$, that is, to $4.19 + 0.3 = 4.49^V$. This correspond to a swing of $9.97 - 4.49 = 5.48^V$.

For a symmetrical waveform, therefore, the swing is limitted to the smaller of the two values mentioned above, that is, 5.03^V. The peak-to-peak output voltage swing is then $2 \times 5.03^V = 10.06^V$.

The corresponding input voltage swing is found by dividing the output swing by the gain v_o / v_i:

maximum permissible peak-to-peak swing of v_i $= \dfrac{2 \times 5.03}{138.3} \cong 0.073\,V$ or $73\,mV$

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Last updated Feb. 8, 2013—AY