

Department of Electrical, Computer, & Biomedical Engineering

Faculty of Engineering & Architectural Science

ELE 202

Electric Circuit Analysis

LAB COVER PAGE for Part I submission.

Lab #:	Lab Title:
Last Name:	
First Name:	
Student #:	
Signature:	Sayeed Ahamad

Section #:	
Submission date and time:	
Due date and time:	

Document submission for Part I:

- A completed and signed "COVER PAGE **Part I**" has to be included with your submission. The report will not be graded if the signed cover page is not included.
- Your completed handwritten pages of **Section 4.0** should be scanned (via a scanner or phone images), together with the required MultiSIM images. **Note:** MultiSIM results must be generated using the Department's licensed version of MultiSIM, and the captured screenshots should show your name (at the center-top) and the timestamp (at the bottom-right corner of your screen).
- Collate and create a *.pdf* or *.docx* file of the above, and upload it via D2L any time prior to the start of your scheduled lab. Upload instructions are provided on D2L.

Zero marks will be assigned for the entire lab if this Part I is not submitted prior to your scheduled lab.

*By signing above, you attest that you have contributed to this submission and confirm that all work you have contributed to this submission is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: www.ryerson.ca/senate/current/pol60.pdf.

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