Ryerson University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

ELE 202
Electric Circuit Analysis
LAB COVER PAGE for **Part I** submission.

Lab #:	4	**Lab Title:**	Circuit Theorems and the Superposition Principle

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***Signature*:**	Sayeed Ahamad

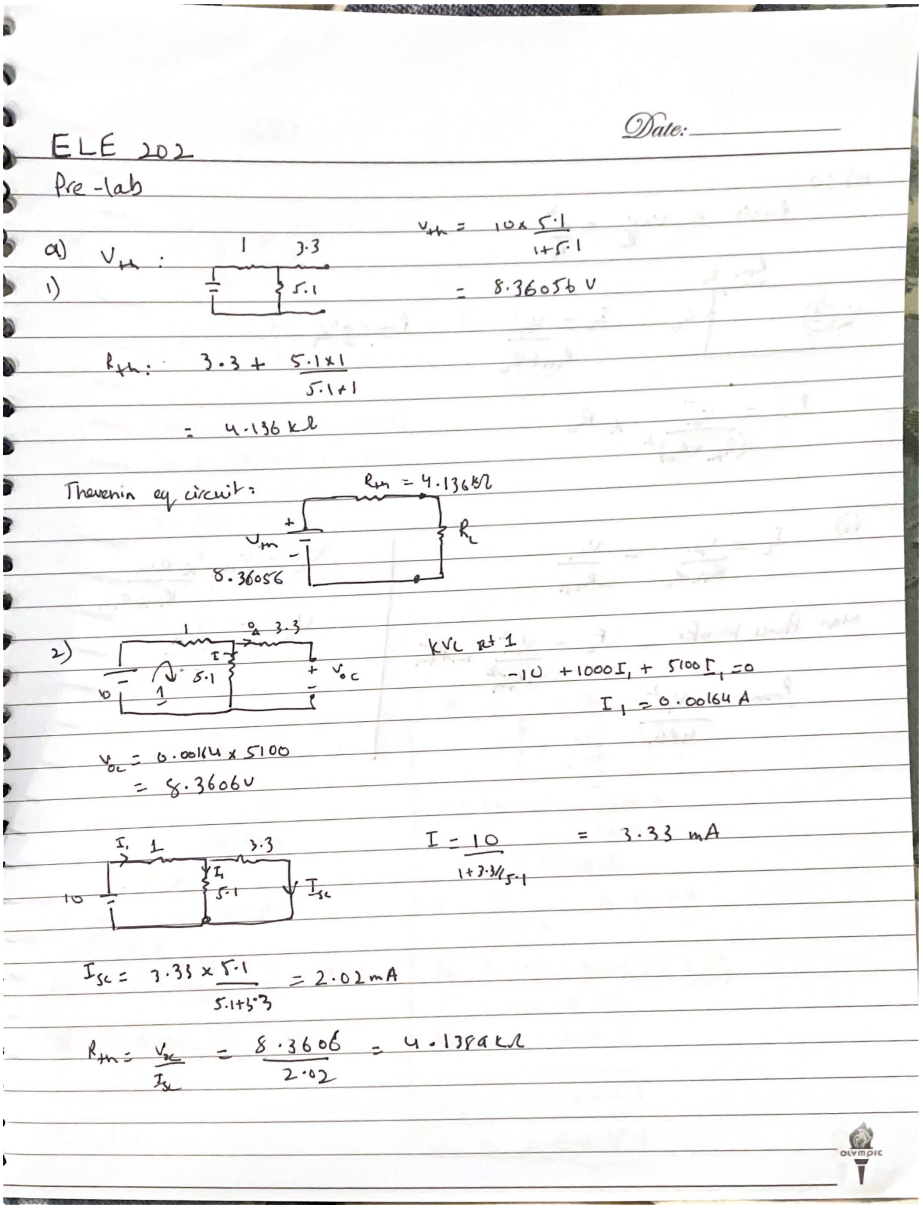
Section #:	11
Submission date and time:	8/3/2023 - 15:00
Due date and time:	8/3/2023 - 15:00

Document submission for Part I:

- A completed and signed "COVER PAGE – **Part I**" has to be included with your submission. The report will not be graded if the signed cover page is not included.
- Your completed handwritten pages of **Section 4.0** should be scanned (via a scanner or phone images), together with the required MultiSIM images. **Note:** *MultiSIM results must be generated using the Department's licensed version of MultiSIM, and the captured screenshots should show your name (at the center-top) and the timestamp (at the bottom-right corner of your screen).*
- Collate and create a ***.pdf*** or ***.docx*** file of the above, and upload it via D2L **any time prior to the start of your scheduled lab**. Upload instructions are provided on D2L.

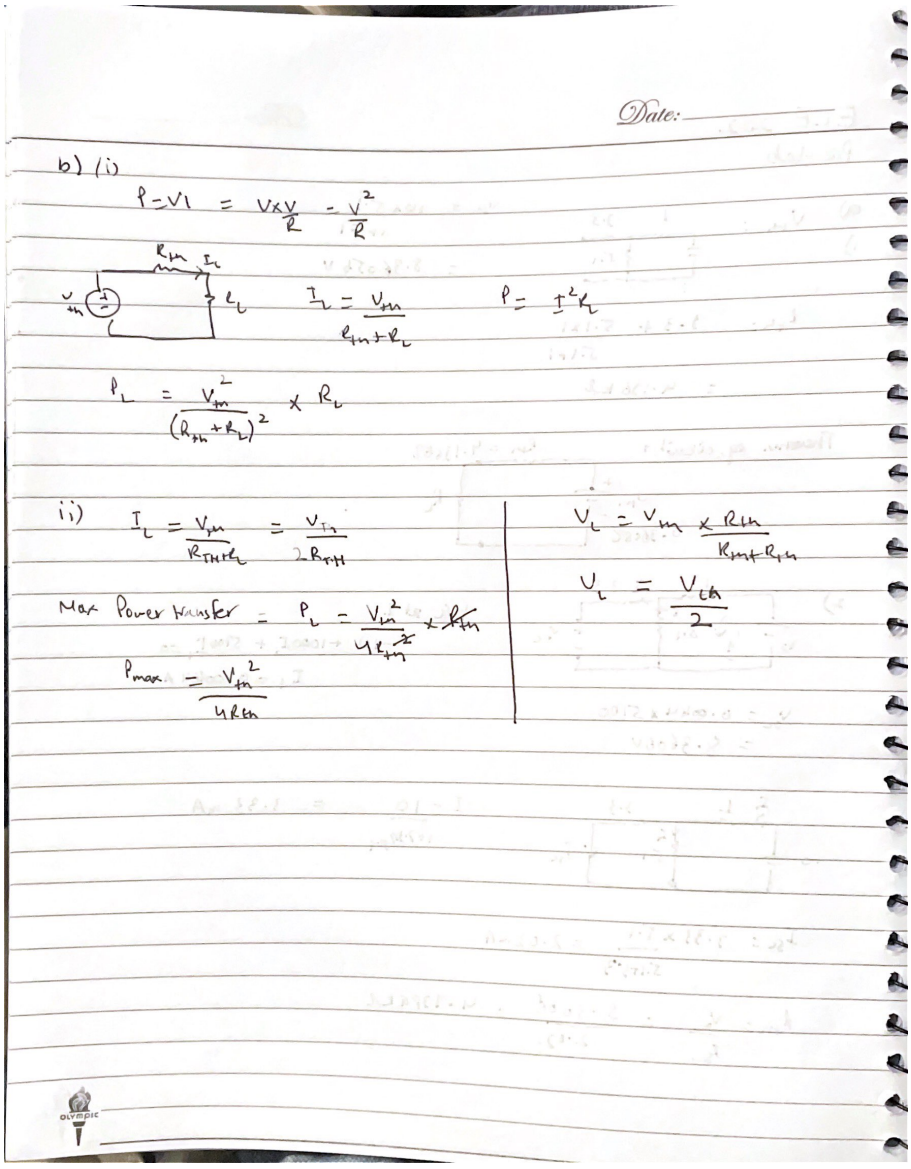
Zero marks will be assigned for the entire lab if this Part I is not submitted prior to your scheduled lab.

**By signing above, you attest that you have contributed to this submission and confirm that all work you have contributed to this submission is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: www.ryerson.ca/senate/current/pol60.pdf.*

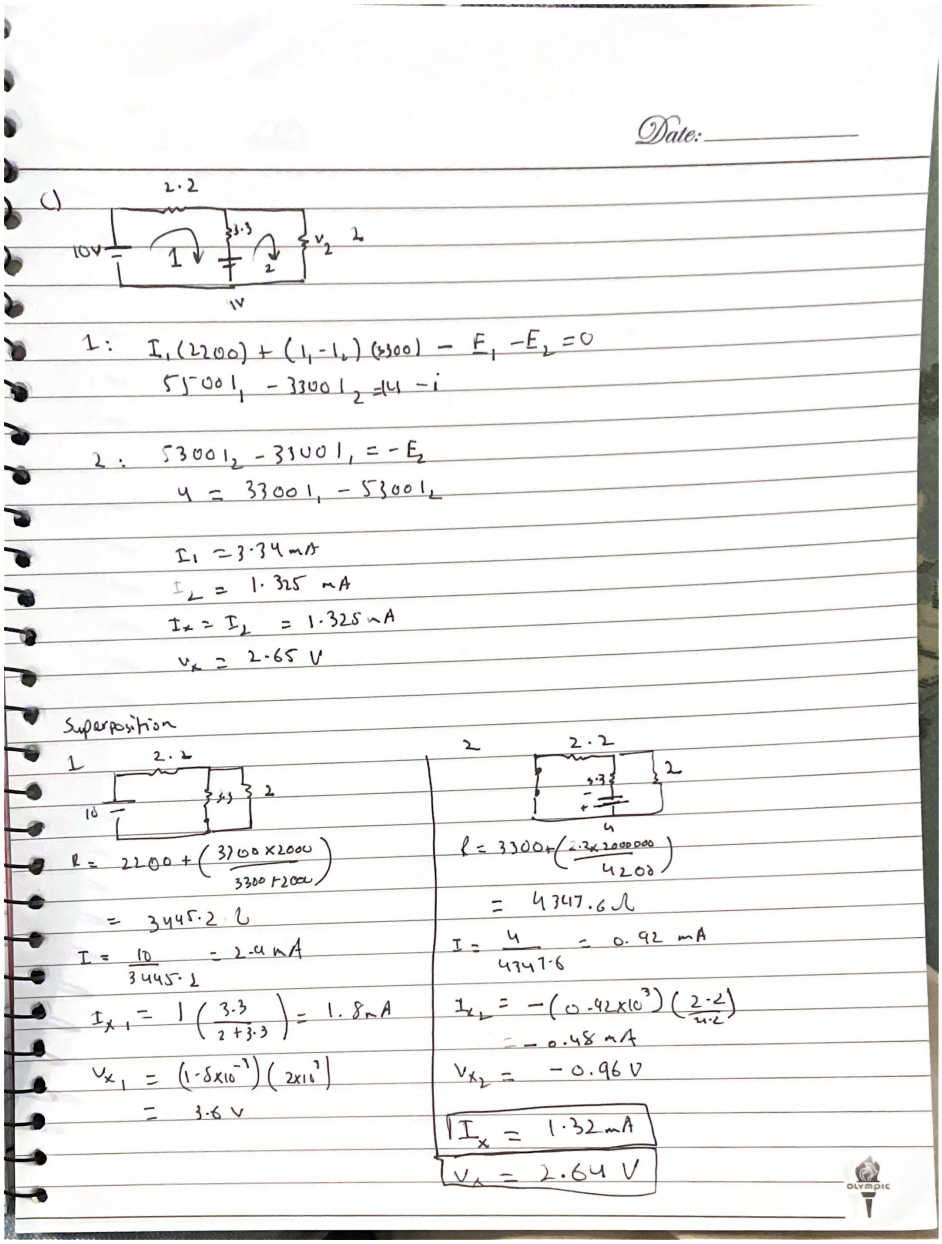


	V_{Th}	R_{Th}	V_{OC}		I_{SC}		$V_{Th} = V_{OC}$		$R_{Th} = V_{OC}/I_{SC}$	
E	Theory **(volts)**	Theory **(kΩ)**	Theory **(volts)**	MultiSIM **(volts)**	Theory **(mA)**	MultiSIM **(mA)**	Theory **(volts)**	MultiSIM **(volts)**	Theory **(kΩ)**	MultiSIM **(kΩ)**
10 (volts)	8.361	4.136	8.361	8.367	2.02	2.021	8.361	8.367	4.14	4.15

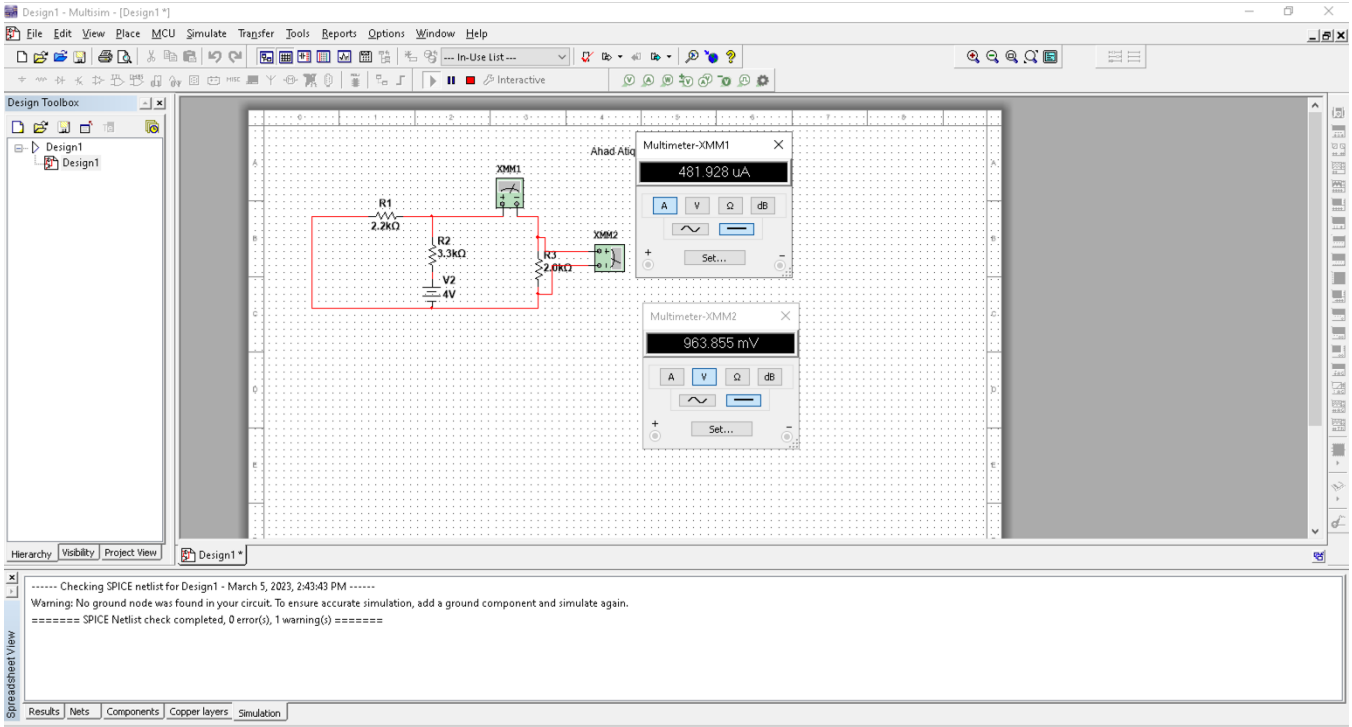
Table 2.0: Theoretical and MultiSIM results of the Figure 2.0 circuits

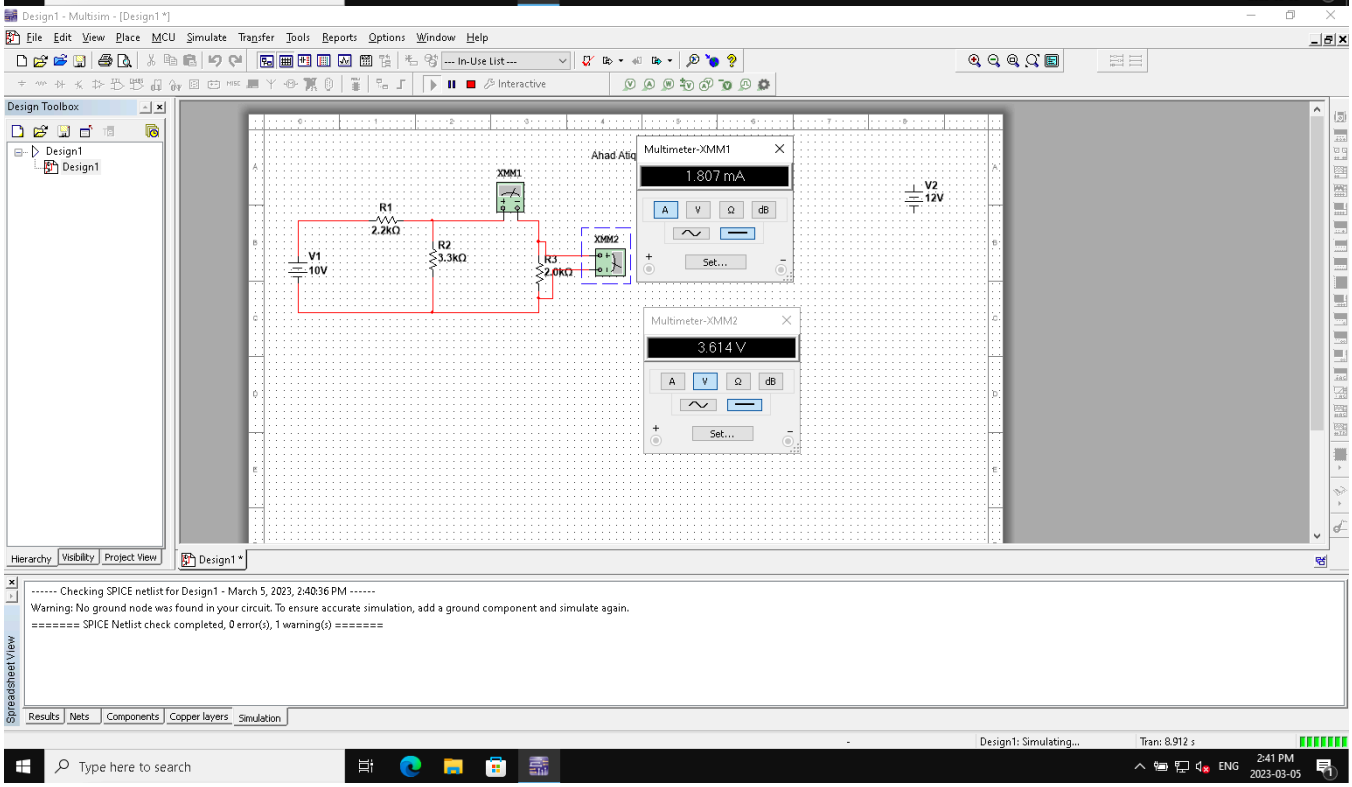


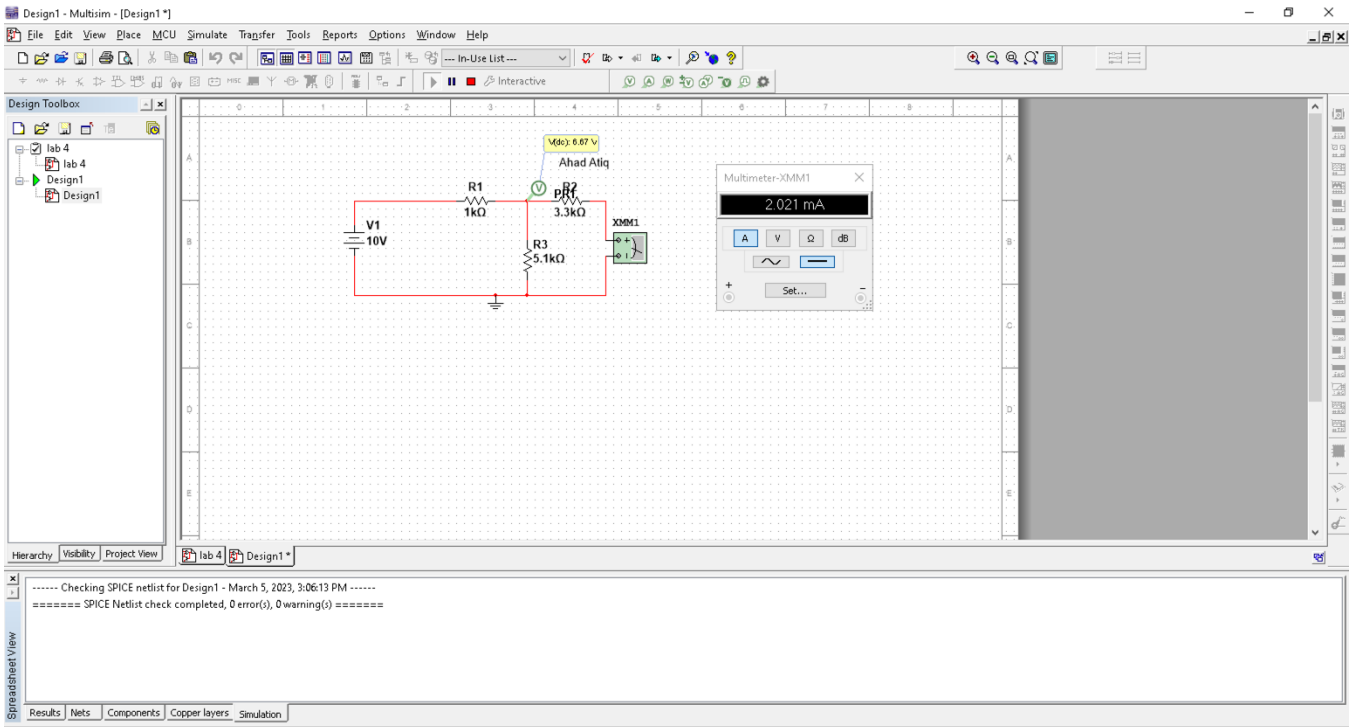
Input Source, **E**	Thevenin voltage, **V_{TH}** (volts)	Measured load voltage, **V_L** (volts)	Load resistance **R_L** per resultant potentiometer, **R_P** reading. (kΩ)
	From **Table 2.0**	MultiSIM	MultiSIM
10 (volts)	8.361	8.36	4.13

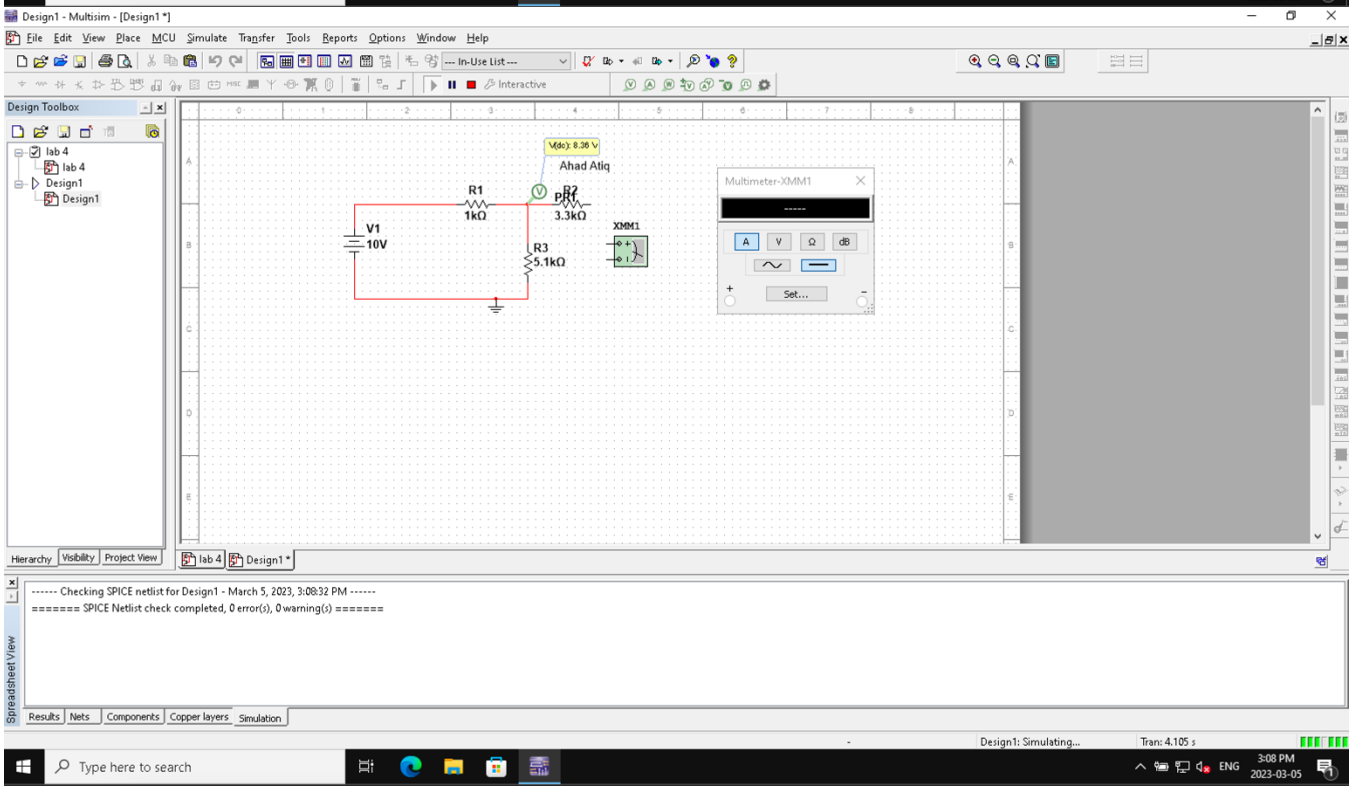


V_X (volts)		**I_X** (mA)		**V_{X1}** (volts)		**I_{X1}** (mA)		**V_{X2}** (volts)		**I_{X2}** (mA)		**$V_X = V_{X1} + V_{X2}$**		**$I_X = I_{X1} + I_{X2}$**	
Th.	MS.	Th.	MS.	Th.	MS.	Th.	MS.	Th.	MS.	Th.	MS.	Th.	MS.	Th.	MS.
2.64	2.661	1.32	1.33	3.62	3.62	1.87	1.81	-0.96	-0.96	-0.48	-0.48	2.641	2.66	1.32	1.33


Design1 - Multisim - [Design1 *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Design Toolbox
Design1
Design1
Ahad Atiq
Multimeter-XMM1
481.928 uA
A V Ω dB
Set...
XMM1
XMM2
R1
2.2kΩ
R2
3.3kΩ
R3
2.0kΩ
V2
4V
Multimeter-XMM2
963.855 mV
A V Ω dB
Set...
Design1 *
Hierarchy Visibility Project View
------ Checking SPICE netlist for Design1 - March 5, 2023, 2:43:43 PM ------
Warning: No ground node was found in your circuit. To ensure accurate simulation, add a ground component and simulate again.
======= SPICE Netlist check completed, 0 error(s), 1 warning(s) =======
Spreadsheet View
Results Nets Components Copper layers Simulation
Design1: Simulating...
Tran: 5.578 s
Type here to search
ENG
2:44 PM
2023-03-05


Design1 - Multisim - [Design1 *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Design Toolbox
Design1
Design1
Ahad Atiq
Multimeter-XMM1
1.807 mA
A V Ω dB
Set...
XMM1
XMM2
R1
2.2kΩ
R2
3.3kΩ
R3
2.0kΩ
V1
10V
V2
12V
Multimeter-XMM2
3.614 V
A V Ω dB
Set...
Design1 *
Hierarchy Visibility Project View
------ Checking SPICE netlist for Design1 - March 5, 2023, 2:40:36 PM ------
Warning: No ground node was found in your circuit. To ensure accurate simulation, add a ground component and simulate again.
======= SPICE Netlist check completed, 0 error(s), 1 warning(s) =======
Spreadsheet View
Results Nets Components Copper layers Simulation
Design1: Simulating...
Tran: 8.912 s
Type here to search
ENG
2:41 PM
2023-03-05


Design1 - Multisim - [Design1 *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Design Toolbox
lab 4
lab 4
Design1
Design1
V(dc): 0.67 V
Ahad Atiq
R1
1kΩ
R2
PRT
3.3kΩ
V1
10V
R3
5.1kΩ
XMM1
Multimeter-XMM1
2.021 mA
A V Ω dB
Set...
Hierarchy Visibility Project View
lab 4 Design1 *
------ Checking SPICE netlist for Design1 - March 5, 2023, 3:06:13 PM ------
======= SPICE Netlist check completed, 0 error(s), 0 warning(s) =======
Spreadsheet View
Results Nets Components Copper layers Simulation
Design1: Simulating...
Tran: 4.372 s
Type here to search
ENG
3:06 PM
2023-03-05


Design1 - Multisim - [Design1 *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Design Toolbox
lab 4
lab 4
Design1
Design1
V(dc): 8.36 V
Ahad Atiq
R1
1kΩ
R2
PRT
3.3kΩ
V1
10V
R3
5.1kΩ
XMM1
Multimeter-XMM1
A V Ω dB
Set...
Hierarchy Visibility Project View
lab 4 Design1 *
------ Checking SPICE netlist for Design1 - March 5, 2023, 3:08:32 PM ------
======= SPICE Netlist check completed, 0 error(s), 0 warning(s) =======
Spreadsheet View
Results Nets Components Copper layers Simulation
Design1: Simulating...
Tran: 4.105 s
Type here to search
ENG
3:08 PM
2023-03-05