

CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 2

Project Teams Group #: 1_2_7

Team Members: Alek Norris
Drew Kearns

Discuss the following aspects of teamwork with your team – make sure to get input from each member. Write down your team's consensus for each of the bolded headings. Italicized text contains instructions and examples and should be deleted once you've read it. Please see the example contract for rough length expectations.

Course Goals: *List and acknowledge the goals of your individual team members. Examples may include:*

- Get a good grade B-A
- Understand how a processor works from the base level
- Minimize the number of points lost
- Understand the security concepts of the hardware of a processor

Team Expectations:

- **Conduct:**
 - Good communication between members (within reason)
 - Don't expect instant responses between 6pm-8am
 - Staying on task
 - Being on time (alert teammate if going to be late)
 - No procrastination, start working well before due date
 - Ask questions, make sure you understand what you're doing
- **Communication:**
 - Snapchat or text
 - Can call for urgent questions
 - Respond within 2 hours from 9am-5pm in normal circumstances
 - Inform teammate of non-normal circumstances ASAP
- **Group conventions:**
 - File names and component names are the same
 - TB file names are TB_<file name>.vhd

- Inputs have i_, outputs have o_, wires have w_, signals have s_ (TB exclusive)
- Put similar/exact labels and bit widths in drawings that will show up in VHDL file
- GitHub will be used for version control

- **Meetings:**

- Tuesday 1-3 (can vary) in person
- Sunday after 1 online (will vary)
- Wednesday-Saturday work separately with communication

- **Peer Evaluation Criteria:**

- As long as both teammates are contributing to the project and demonstrating effort.
- Let other teammate know if you think they are not putting in enough effort

Role Responsibilities: *Complete the following planning table. Each lab part should be the responsibility of one team member. Also make sure that no one team member is the lead on both the design and test aspects of a single lab part. These guidelines aid in all students having a complete view of the lab. Note that the non-lead is encouraged to participate and support the lead wherever possible, increasing both the quality of the lab part and each team member's knowledge.*

Lab Part		Estimated Time	Design		Test	
			Lead	Deadline	Lead	Deadline
Software-Scheduled Pipeline	Control Signals	0.5 hr	Alek	4/4/24	Drew	4/5/24
	Datapath	3 hr	Drew/ Alek	4/7/24	Alek	4/8/24
	Testing	3 hr	Alek	4/10/24	Drew	4/10/24
	Synthesis (human effort)	0.5 hr	Alek Drew	4/10/24	Alek Drew	4/10/24
Hardware-Scheduled Pipeline	Pipeline Register Update	1 hr	Drew	4/12/24	Alek	4/14/24
	Data Hazard Avoidance	4 hr	Alek	4/18/24	Drew	4/20/24
	Control Hazard Avoidance	2-6 hr based on group size	Drew	4/25/24	Alek	4/27/24
	Integration (Hardware-Schedule Pipeline)	3 hr	D/A	4/29/24	D/A	4/29/24
	Testing	3 hr	D/A	4/30/24	D/A	4/30/24
	Synthesis	0.5 hr	D/A	4/30/24	D/A	4/30/24

*Estimated Time is given as a **very rough** guide for even distribution of tasks assuming you've already read through the lab document and have the prerequisite knowledge. Please note that to be done properly, the test programs will require significant time investment, but will result in a much stronger final design.*

Integrity of Work: *Do not delete the following.* We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature _____ Alek Norris _____ **Date** 4/4/24

Student Signature _____ Drew Kearns _____ **Date** 4/4/24

Student Signature _____ **Date** _____