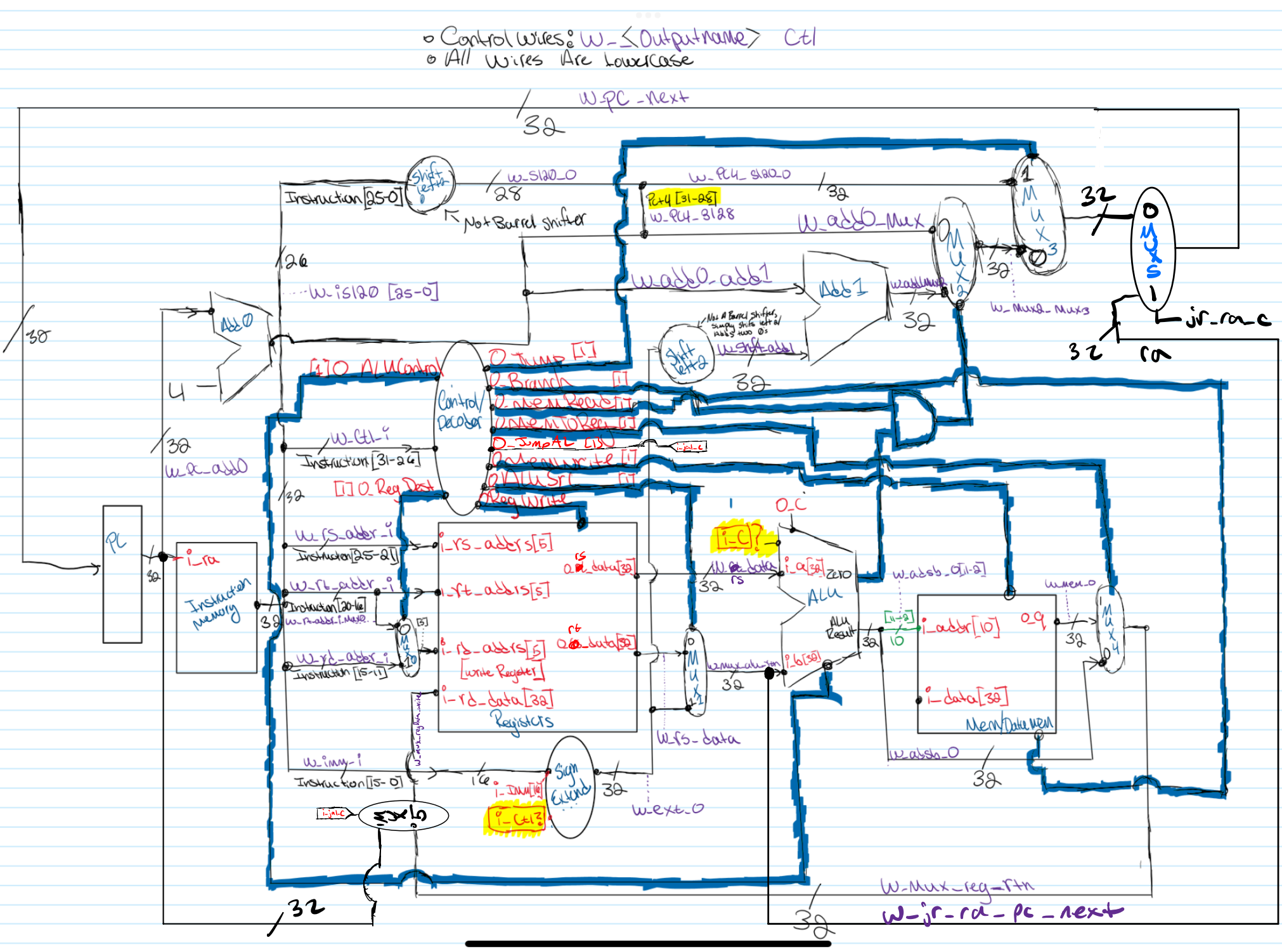
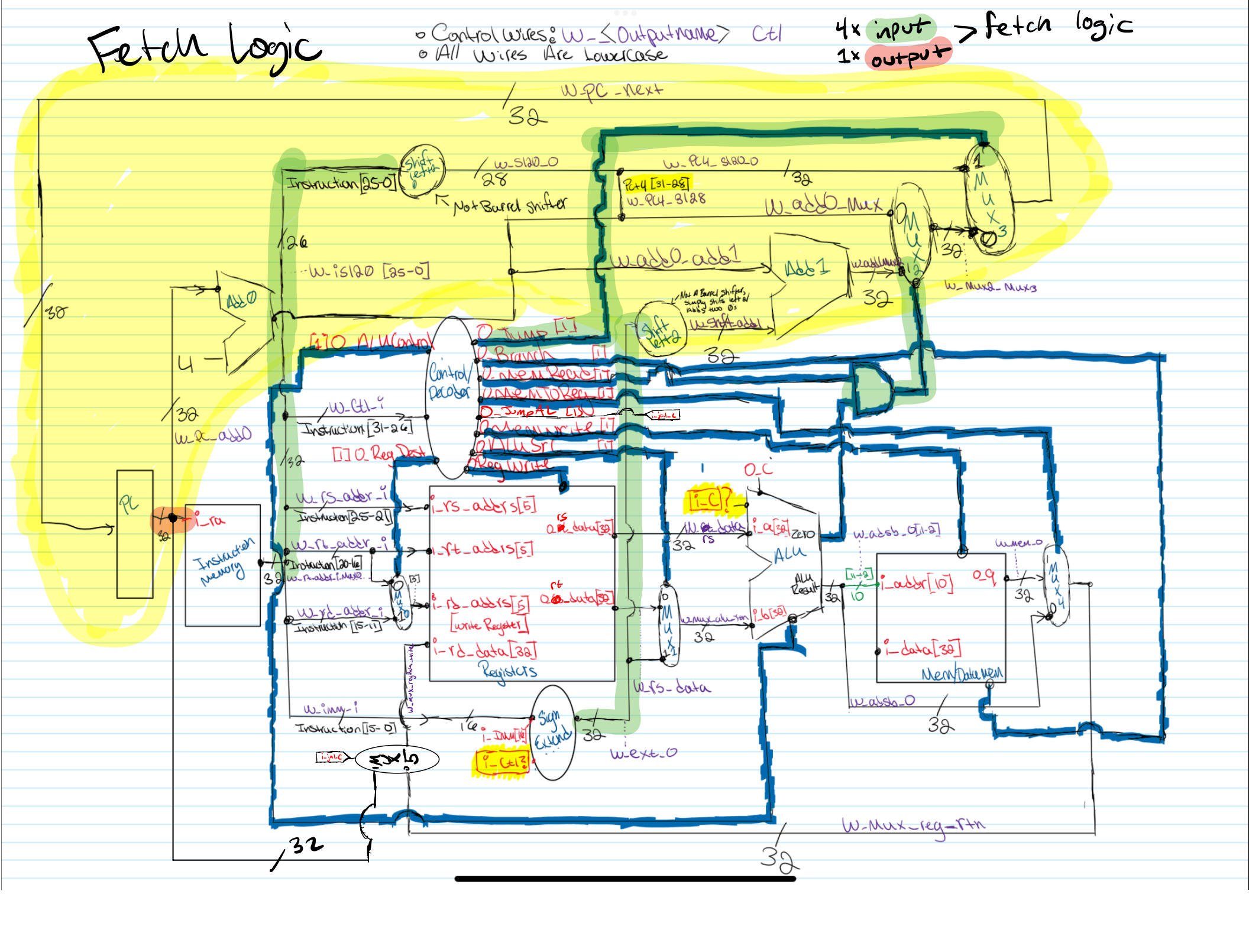

Control wires: w_<Output name> Ctl
All wires Are Lowercase
w_pc_next
32
Instruction [25-0]
shift left 2
28
w_s128_0
Not a Barrel shifter
pc+4 [31-28]
w_pc4_s128_0
w_pc4_s128
w_add0_Mux
w_is128 [25-0]
w_add0_add1
Add 1
Add 0
Shift left 2
Not A Barrel shifter, simply shifts left by two 0s
w_shft_add1
w_Mux0_Mux3
jr_ra_c
ra
Control/ Decoder
O_Jump [1]
O_Branch [1]
O_MemRead [1]
O_MemToReg [1]
O_JumpAL [1:0]
O_MemWrite [1]
O_ALUSrc [1]
O_RegWrite [1]
[1:0] O_ALUControl
[1] O_Reg Dest
w_ctl_i
Instruction [31-26]
w_a_add0
PC
i_ra
Instruction Memory
Instruction [20-16]
Instruction [15-11]
w_rs_addr_i
w_rt_addr_i
w_rd_addr_i
Instruction [25-21]
i_rs_addrs[5]
i_rt_addrs[5]
i_rd_addrs[5] [write Register]
i_rd_data[32]
Registers
rs_data[32]
rt_data[32]
w_rs_data
w_imm_i
Instruction [15-0]
i_imm[16]
Sign Extend
w_ext_0
i_ctl[2]
i_c
O_C
i_a[32]
i_b[32]
Zero
ALU
ALU Result
w_alu_rtn
w_addr_0[11-2]
i_addr[10]
O_Q
w_mem_0
i_data[32]
MemDataMem
w_data_0
w_Mux_reg_rtn
w_jr_ra_pc_next

Fetch Logic

- Control wires: w_<Outputname>_ctl
- All wires are lowercase

4x input → fetch logic
1x output



Fetch Logic

- Control Wires: w_<Outputname> Ctl
- All Wires Are Lowercase