Quiz 4 SC1005

Q1. What should be the constraint in verilog code to assign output oflow to the LED display (LD3)

For this question, look on the BASYS to see which port LD3 is at (e.g: V19)

a. set_property IOSTANDARD LVCMOS33 [get_ports {b[0]}]

b. set_property PACKAGE_PIN V19 [get_ports {LD3}]

c. set_property PACKAGE_PIN LD3 [get_ports {oflow}]

(d.) set_property PACKAGE_PIN V19 [get_ports {oflow}]

Q2. Given the following Verilog code for the 7-digit decoder from input x

```
module vsevenseg(
    input [3:0] x,          // 4 rightmost switches
        output [6:0] seg_L,     // active low segment display
        output [3:0] anode_L    // active low digit display
        );

    // declare internal active high segments
    reg [6:0] seg;                  // 1:on, 0:off

    // turn on only the two rightmost digits - active low
    assign anode_L = 4'b1100;

    assign seg_L = ~seg;

    always @*
        begin
            case (x)
                4'b0000: seg = 7'b0111111; // 0
                4'b0001: seg = 7'b0000110; // 1
                4'b0010: seg = 7'b1011011; // 2
                4'b0011: seg = [redacted]; // 3
                4'b0100: seg = [redacted]; // 4
                4'b0101: seg = 7'b1101101; // 5
                4'b0110: seg = [redacted]; // 6
                4'b0111: seg = [redacted]; // 7
                4'b1000: seg = [redacted]; // 8
                4'b1001: seg = 7'b1101111; // 9
                4'b1010: seg = 7'b1110111; // A
                4'b1011: seg = 7'b1111100; // b
                4'b1100: seg = [redacted]; // C
                4'b1101: seg = 7'b1011110; // d
                4'b1110: seg = [redacted]; // E
                4'b1111: seg = 7'b1110001; // F
                default: seg = 7'b0000000; // Off
            endcase
        end

endmodule
```

Show the decoder to assign to seg if

- The display shows number 3

1001111

- The display shows character F

1110001

Q3. Which one of the following is a sum of products expression?

- Free mark, I don't remember the options

Q4. Open drain outputs can be connected together to form a wired AND output which will be low when at least one of the individual output is low. True or False ?

Q5. Assume you have a module extract with 3-bit input x and 4-bit output y. Suppose you want to initiate the module with input danode and output seg_L. What is the correct way to run this in verilog?

a m1 extract (.input(danode), .output(seg_L))

b extract uut (.input(danode), .output(segL))

c m1 extract (.x(danode), y(seg_L))

d extract m1(.x(danode), .y(seg_L))

Q6. Given a maxterm $f(a,b,c) = \pi M(0,5,6)$. What is the following verilog code to express the maxterm?

x = (a|b|c) & (~a|b|~c) & (~a|~b|c)

Q7. Which of the following is correct.

a. Active low ⇒ output 0 when negated

b. Logic low can be connected to an active high

c. Logic high cannot be connected to an active low

d. Active high ⇒ output 0 when asserted