**EXPERIMENT NO.6**

**Sequential Circuit Design**

SUBMITTED TO:

Dr. Ubaid Ullah Fayyaz

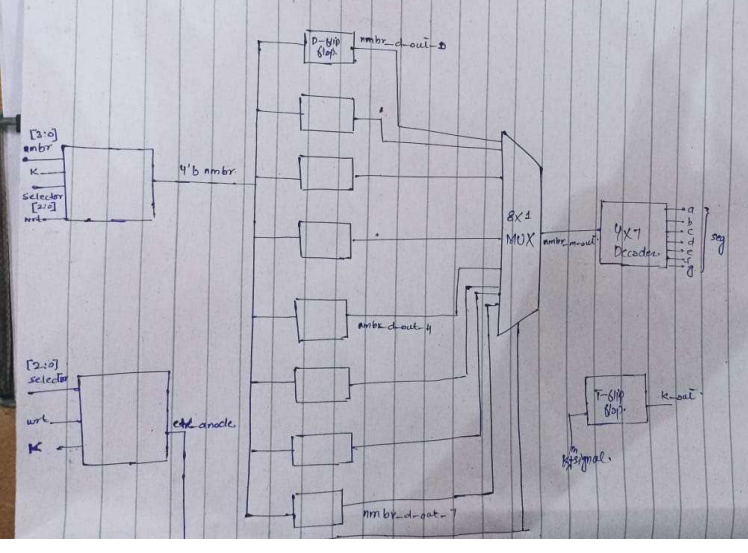
SUBMITTED BY:

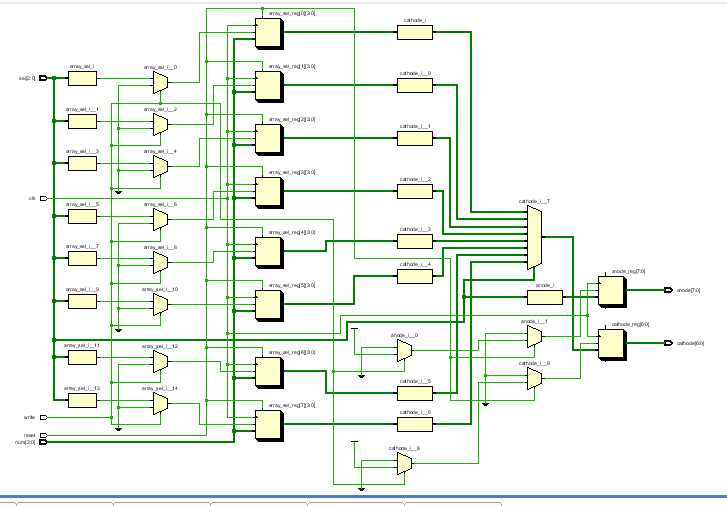
Ans Qasim

2022-EE-171

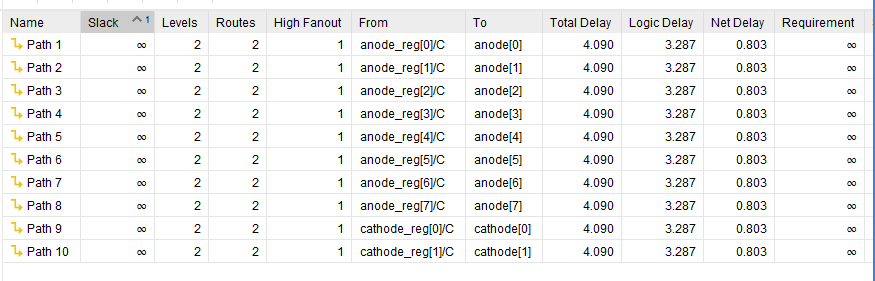
**UNIVERSITY OF ENGINEERING & TECHNOLOGY, LAHORE**

Hand sketched diagram:

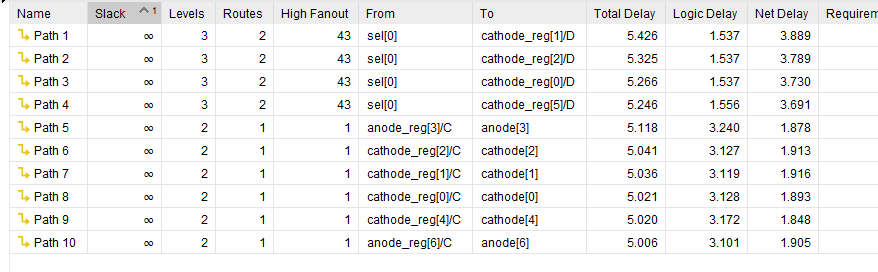




Synthesis Combinational Delay:

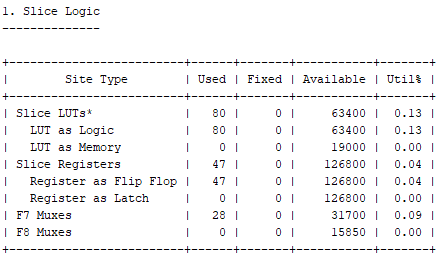


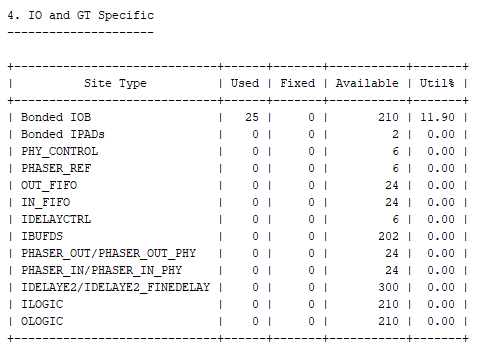
Implementation Combinational Delay:

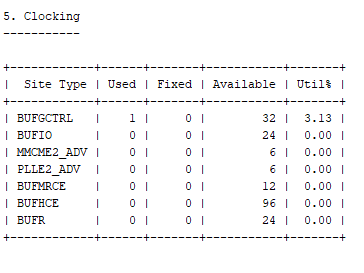


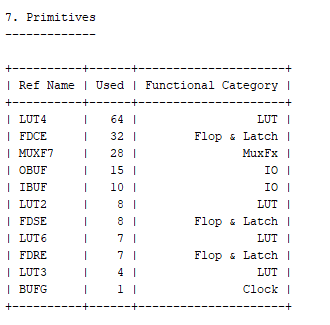
Path 1 has the maximum combinational delay.

**Resources Utilization Summary:**

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