**EXPERIMENT NO.4**

**COMBINATIONAL CIRCUIT DESIGN USING K-MAPS**

SUBMITTED TO:

Dr. Ubaid Ullah Fayyaz

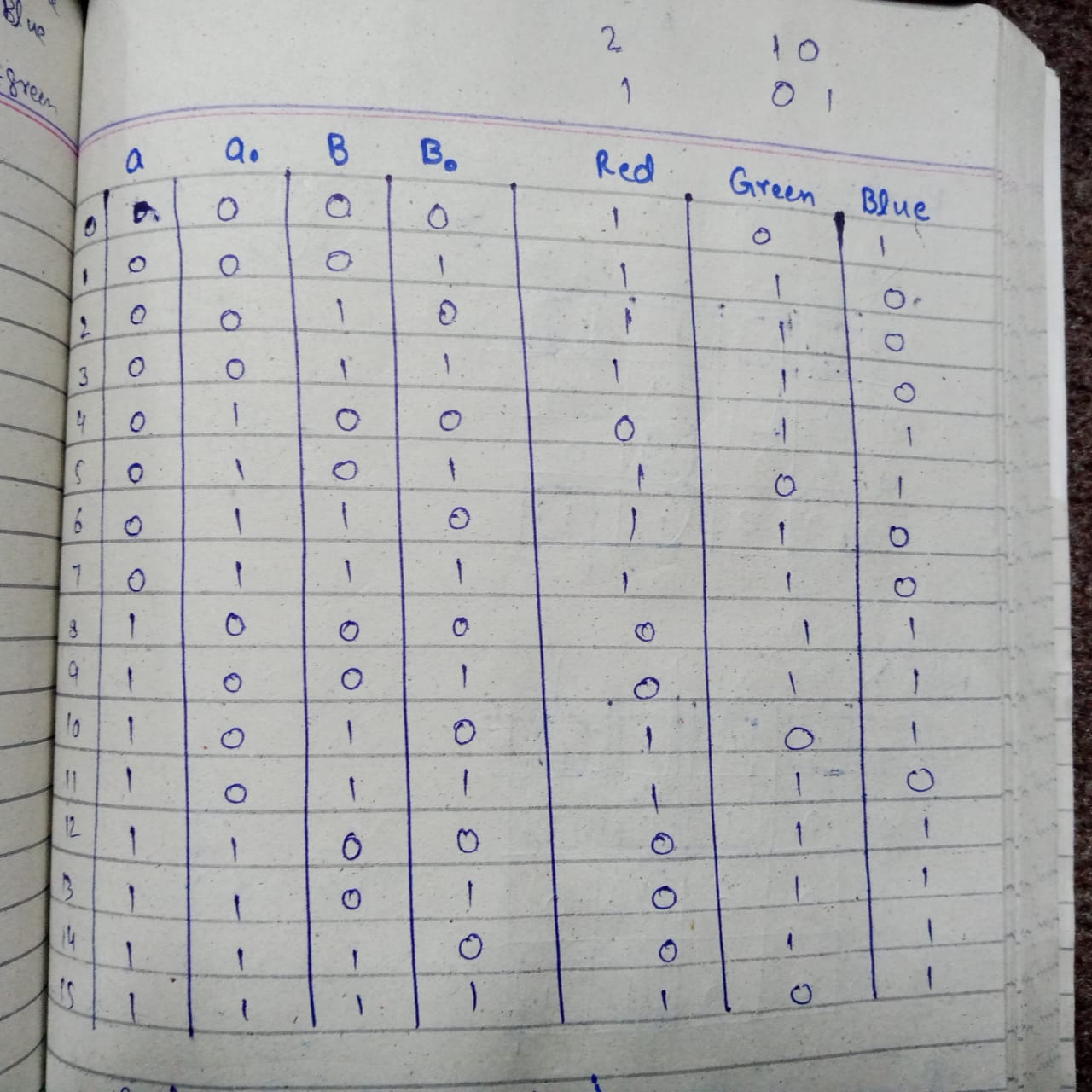
SUBMITTED BY:

Ans Qasim

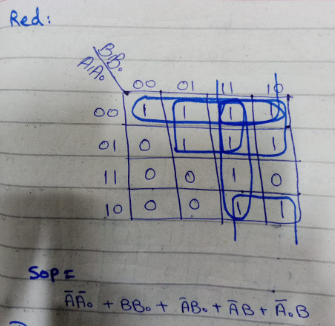
2022-EE-171

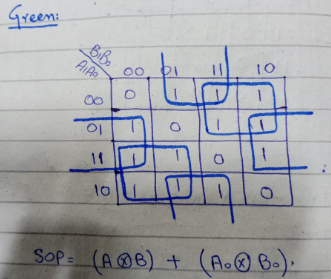
**UNIVERSITY OF ENGINEERING & TECHNOLOGY, LAHORE**

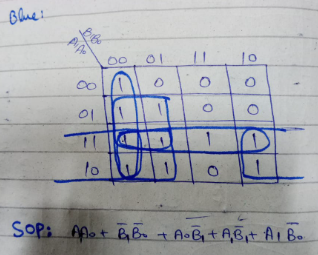
**Truth Table:**

****

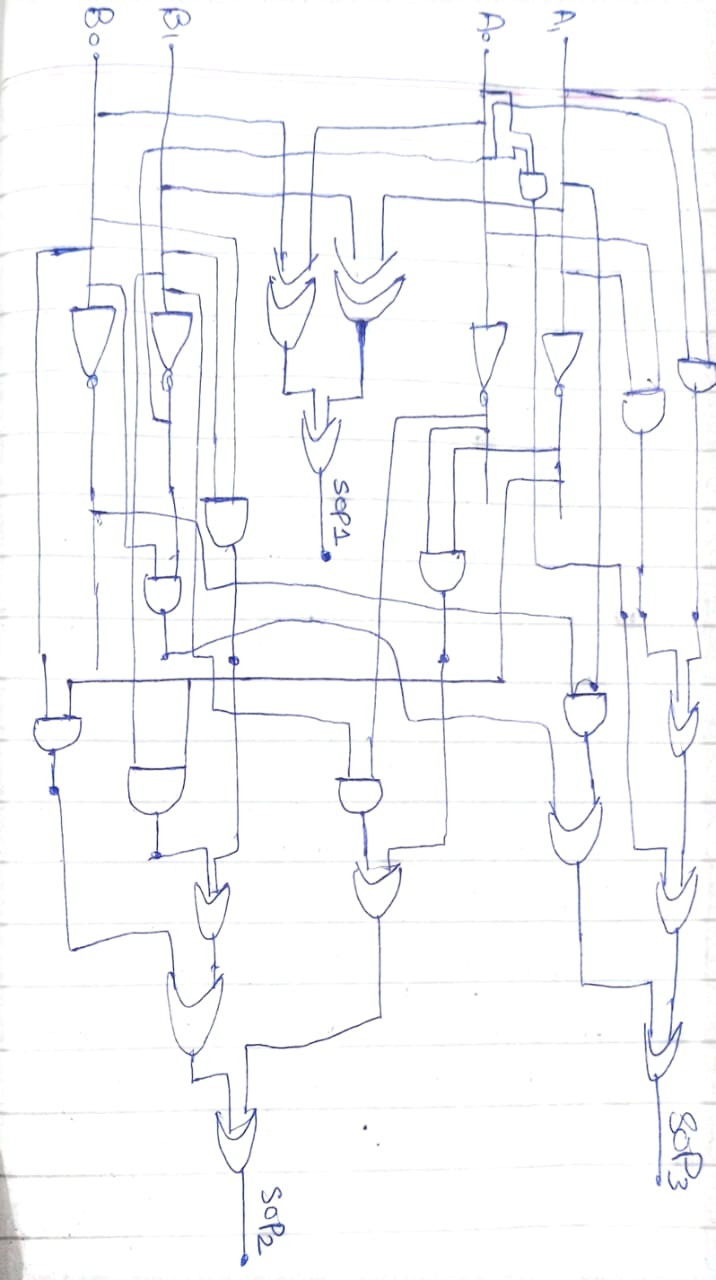
K-maps:



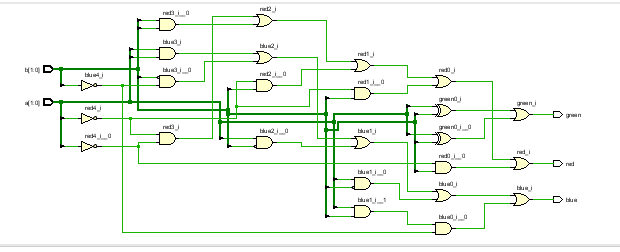




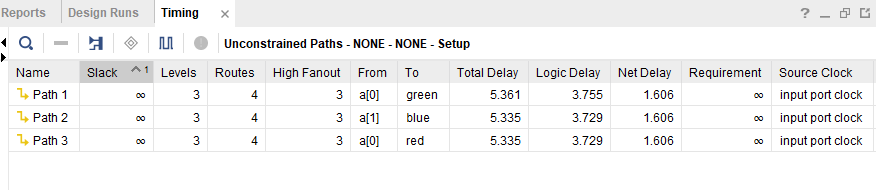
Circuit Diagram:



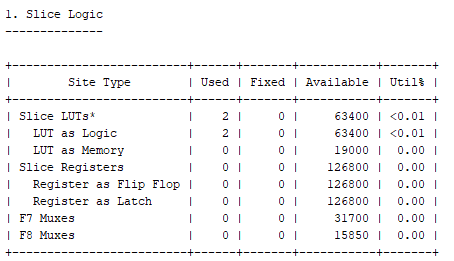
Circuit diagram using vivado:

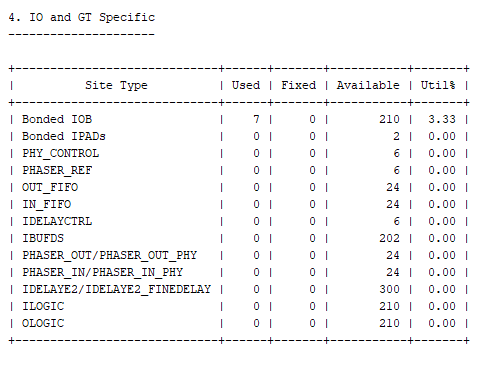


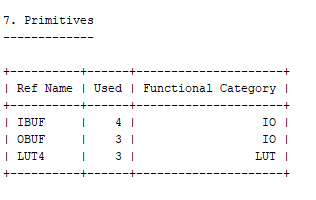
Delay in synthesis:



Resource Utilization:







**System Verilog Code:**

