Data Transfer Group -

mov Rd, Rs -

Operation - Rs → Rd
Addressing mode - Register addressing mode
No. of bytes - 1 byte
Description - Here content of register Rs will be copied to register Rd.
Eg - mov B, C
B = 20
C = 30
After execution B = 30 C = 30.
Flags - Not affected.

mov R, M -

Operation - M → R
Addressing mode - Indirect addressing mode.
No. of bytes - 1 byte.
Description - The content of ML whose address is stored in HL pair will be copied to register R.
Eg - mov B, M
Flags - Not affected.
B = 20
H = 40
L = 00
4000 = 10
After execution
B = 10.

mov m,R -

Operation - R → m
Addressing mode - Indirect addressing mode.
No of bytes - 1 byte
Description - The contents of register will be copied to the memory location whose address is stored in HL pair.
Flag - Not affected

Eg - mov m,B

B = 10
H = 60
L = 03
6003 = 20

After execution -

6003 = 10

mvI R,data -

Operation - Data → R
Addressing mode - Implied Immediate addressing mode
No of bytes - 2 bytes.
Description - Move immediate data to register R
Flag - not affected.

Eg - mvi C,50

C = 10

After execution

C = 50

LXI Rp, Data [16 bit data] -

Operation - Data → Rp
Addressing mode - Immediate addressing mode
No. of bytes - 3 bytes
Description - mov immediate 16 bit data to the register pair.

Eg - LXI H, 20 30

H = 50
L = 70

After execution
H = 20
L = 30

LDA Address -

Operation - (Address) → A
Addressing mode - Direct addressing mode.
No. of bytes - 3 bytes
Description - Load the accumulator from the address given in the instruction.

Eg - LDA 4000 = 20 Flags - Not affected.
A = 10
4000 = 20
After execution
A = 20

STA Address -

Operation - A → (Address)
Addressing mode - Direct addressing mode
No of bytes - 3 bytes
Description - Store the contents of accumulator to the address given in the instruction

Eg - STA 4000 Flags - not affected.
A = 10
4000 = 20
After execution
4000 = 10

mvI M, Data -

Operation - Data → M
Addressing mode - Immediate / Indirect addressing mode
No of bytes - 2 bytes
Description - move immediate data to the ML whose address is stored in HL pair.

Eg - mvI M, 20 Flags - Not affected.
H = 40
L = 02
4002 = 30
After execution
4002 = 20.

LHLD Address-

Operation - (Address) → L
Addressing mode - Direct
No of bytes - 3 bytes
Description - Load the contents of the address to register L and content of H to address + 1.

Eg- LHLD 3001 Flags - not affected
H = 40
L = 30
3001 = 33
3002 = 44

SHLD Address-

Operation - L → (Address) H → (Address + 1)
Addressing mode - Direct addressing mode
No of bytes - 3
Description - Here content of L will be stored to address and content of H to address + 1

Eg- SHLD 5000
H = 60
L = 70
5000 = 50
5001 = 40
After execution
5000 = 70
5001 = 40

LDAX Rp -

Opeation - (Rp) → A
Addesing mode - Indirect / Register addesing mode
No of byte - 1 byte
Desciption - Load the content of accumulator from the memory location whose addess is given by register pair.

Eg - LDAX B Flags - not affected
A = 10
B = 60
C = 03
6003 = 20
After execution
A = 20.

STA X, Rp -

Opeation - A → (Rp)
Addesing mode - 1 byte
No of byte - Indirect / Register
Desciption - Store the contents of accumulator to the memory location whose address is given by register pair.

Eg - STA X, B
Let A = 20
B = 60
C = 03
6003 = 10
After execution
6003 = 20.

XCHG -

Operation - HL ↔ DE H → D, D → H & L → E, E → L
Addressing mode - Register addressing mode
No of byte - 1 byte.
Description - This instruction exchange the content of HL pair with DE pair.

Eg - XCHG

H = 10	H = 40
L = 20	L = 50
D = 40	D = 10
E = 50	E = 20

After execution

Flags - not affected.

IN address -

Operation - (Port address) → A
Addressing mode - Direct addressing mode
No of byte - 2 bytes.
Description - The content of the port address given in the instruction will be inputted to accumulator.

Eg - IN 24

A = 24
24 = 40

After execution
A = 40.

Flag - Not affected.

OUT Address-

Operation- A → (Port address)
Addressing mode- Direct
No of bytes - 2 bytes
Description- The content of accumulator will be outputted to the port address given in the instruction.

Eg- OUT 24
A = 10
24 = 40
After execution
24 = 10

EI -

No of bytes - 1 byte
Addressing mode - Implied addressing mode
Operation - Flip-flop = 1
Description - This instruction enables maskable interrupts. When this instruction is executed the interrupt enable FF is set, so that all interrupts are enabled.

DI -

Operation - FF = 0
No of bytes - 1 byte
Addressing modes - Implied addressing mode
Description - When this instruction is executed the interrupt enable FF is reset so that all maskable interrupts are disabled.

RIM-

Operation - A = Status of interrupt
Addressing mode - Implied addressing mode
No of bytes - 1 byte
Description - When this instruction is executed the status of interrupt is copied into accumulator

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SID	I7.5	I6.5	I5.5	IE	M7.5	M6.5	M5.5

RIM format

1 = Mask
0 = Unmask

1 = Pending 0 = Not pending.

SIM-

Operation - enabled / disabled interrupts
No of bytes - 1 byte
Addressing modes - Implied addressing mode
Description - When the instruction is executed the interrupts are masked or kept pending as specified in accumulator.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SOD	SOE	X	X	MSE	M7.5	M6.5	M5.5

SIM format

1 = Enable
0 = Disable

1 = Mask
0 = no mask

R7.5 ⇒ 1 - reset
0 - no effect.

* 8085 has 74 basic instructions. Total instructions can be executed.

Arithmetic Group :→

(i) ADC : Add Register to Accumulator with carry

Opcode	operand
ADC	Reg (R)
	Memory (M)

→ It is a 1 byte instruction.
→ Addressing mode is Register Addressing Mode.
The contents of the operand (register or memory) and the carry flag are added to the contents of the accumulator & the result is place in the accumulator.

$[A] \leftarrow [A]+[R]+[C]$.

$[A] \leftarrow [[HL]]+[CS]+[A]$.

(ii) ADD : Add Register to Accumulator.

ADD Reg.	1.	$[A] \leftarrow [A]+[R]$.
Memory.		$[A] \leftarrow [A]+[[HL]]$.

→ It is 1 byte instruction.
→ Addressing mode is Register Addressing Mode.
→ The content of the operand (register or memory) are added to the contents of the accumulator and the result is stored in the accumulator.

* ADI : Add Immediate to Accumulator

opcode operand
ADI : 8 bit data [A] ← [A] + [data]

- It is 2 byte.
- The 8-bit data are added to the content to the accumulator and the result is placed in the accumulator.
- Addressing mode is Immediate addressing mode.

* ACI : → Add Immediate to Accumulator with carry.

opcode operand.
ACI data (8-bit) [A] ← [A] + [data] + [carry].

- It is 2-byte.
- It 8-bit data (operand) and the carry flag are added to the contents of the accumulator and the result is stored in the
- Addressing mode is immediate

* DAD : Add Register Pair to H & L Registers.

DAD Rp pair [HL] ← [HL] + [RP]

* It is a 1-byte instruction.
* The 16 bit contents of the specified register pair are added to the content of HL register & the sum is saved in the HL register. The content of the source register pair are not altered.
* Addressing mode is Register Addressing Mode.

* Decimal Adjust Accumulator: DAA -

opcode	operand
DAA	None

- It is 1 byte instruction.
- The contents of the accumulator are changed from a binary value to two 4-bit binary coded decimal (BCD) digits. This is the only instruction that uses auxiliary flag (internally) to perform the binary to BCD conversion.

* DCR: Decrement Source by 1.

DCR Reg (Register addressing mode).
Memory (Register indirect addressing mode).

- It is 1 byte instruction.
- The contents of the designated register/memory is decremented by 1 and the results are stored in same place. If the operand is a memory location, it is specified by the contents of HL register pair.

* DCX: Decrement Register Pair by 1.

opcode	operand
DCX	Reg. pair

- It is 1-byte instruction.
- The contents of the specified register pair are decremented by 1. This instruction views the content of two registers as 16-bit number.
- Addressing mode is Register direct.