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Digital Logic Lab Assignment # 1

1. **To verify the operation of Derived Gates.**

Submitted By

Name

Year/SEM

Roll No.

Submitted To

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OBJECTIVE 1.1:

TO VERIFY THE OPERATION OF NOR GATE.

THEORY:

NOR gate can be defined as the combination of OR gate and NOT gate. In other words output of OR gate is connected to the input of NOR gate. Note that output of OR gate is inverted to form NOR gate.

Boolean expression's= (A+B)

CIRCUIT DIAGRAM:

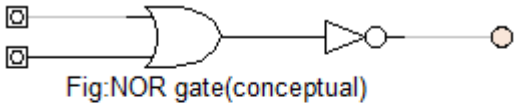

Fig:NOR gate(conceptual)

Fig:NOR gate(circuit)

TRUTH TABLE:

INPUTS		OUTPUT
A	**B**	**(A+B)'**
0	**0**	**1**
0	**1**	**0**
1	**0**	**0**
1	**1**	**0**

OBSERVATION:

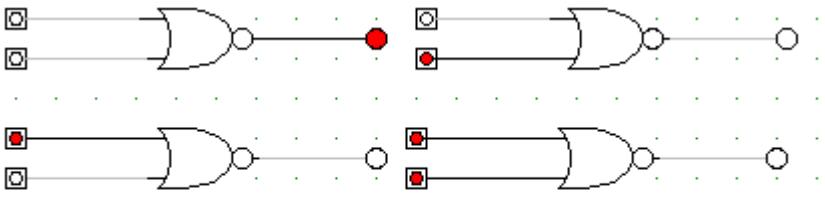

Fig: Logical operation of NOR gate

OBSERVATION TABLE:

INPUTS		OUTPUT
A	**B**	**(A+B)′**
0	**0**	**1**
0	**1**	**0**
1	**0**	**0**
1	**1**	**0**

CONCLUSION:

Hence, the logical operation of NOR gate was verified.

REFERENCE:

http://www.physicshandbook.com/topic/topicc/combgates.htm

DL LAB ASSIGNMENT #1

OBJECTIVE 1.2:

TO VERIFY OPERATION OF NOR GATE.

THEORY:

Combination of AND gate NOT gate results in the formation of NAND gate as shown in fig below. Here in this gate output is opposite of the AND gate and output of AND gate is connected to the input of NOT gate.

Boolean expression: F=(A.B)′

CIRCUIT DIAGRAM:

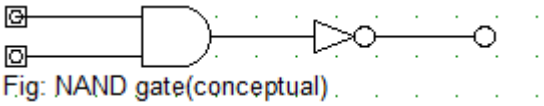

Fig: NAND gate(conceptual)

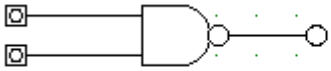

Fig: NAND gate(circuit)

TRUTH TABLE:

INPUTS		OUTPUT
A	**B**	**(A.B)′**
0	**0**	**1**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

OBSRVATION:

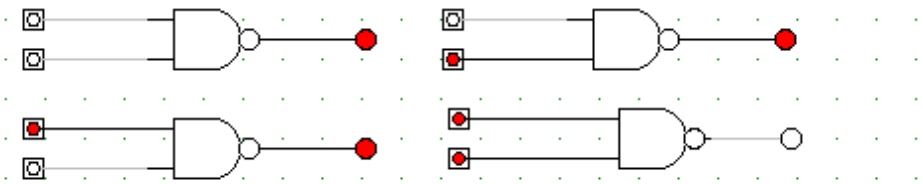

Fig:Logical operation of NAND gate

OBSERVATION TABLE:

INPUTS		OUTPUT
A	**B**	**(A.B)′**
0	**0**	**1**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

CONCLUSION:

Hence, the property of NAND gate was verified.

REFERENCE:

http://www.physicshandbook.com/topic/topicc/combgates.htm