LAB 1: Familiarization with Basic Gates

Objectives:-

The objective for this lab is to understand the fundamentals of logic gates and its use in implementing basic Boolean function.

Apparatus Required:-

-NOT gate (74HC04D-6V)

- AND gate (74HC080-6V)

-OR gate (7432N)

-Switch

-VCC

-Ground

-LED light

Theory:-

AND Gate: -

AND gate is an electronic circuit which produces high (1) output when all the inputs are high (1), otherwise the output will be low (0). It can have a two or more inputs and produces single output.

OR Gate:-

OR gate is an electronic circuit which produces high (1) when one of the input is high (1). If all inputs are Low (0), then output will also be low (0). It has two or more inputs and produces single output.

NOT Gate:- NOT gate is an electronic circuit whose output is the complement of the input. It is also called inverter. If we provide high input (1) to the gate, it will produce low (0) output. It has single input and single output.

Functional Expression:-

AND: - F=X.Y

OR: - F=X+Y

NOT: - X=X'

'Y+XY'
X'Y'+XY

NOR Gate.

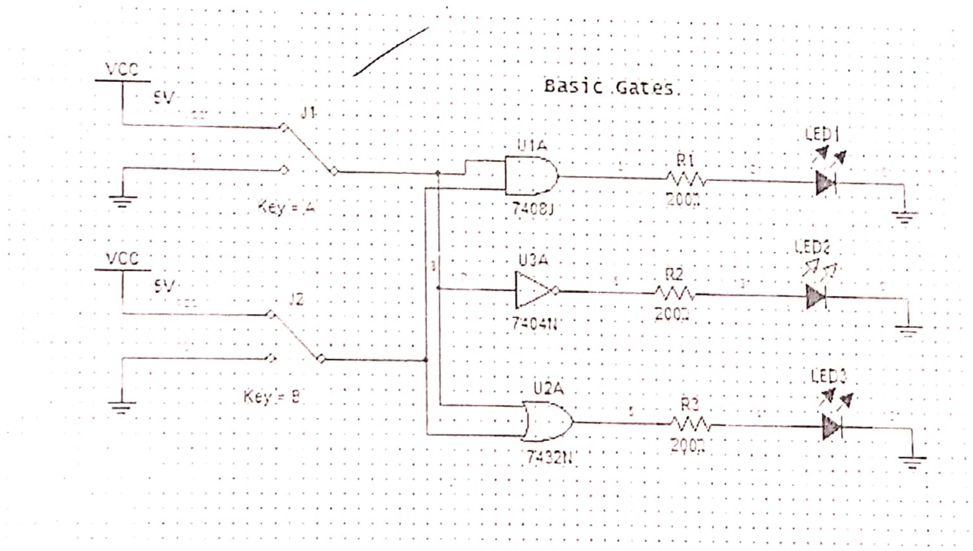
Truth Table of NOT gate: -

Input	Output
X	X'
1	0
0	1

Truth Table of AND and OR gate: -

Input		Output	
X	Y	F=X.Y	F=X+Y
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1

Circuit Diagram: -



Conclusion: -

Hence, the output of basic gate is observed.

LAB 2: Derived Gates

2

Objective: -

Understand how to use the breadboard to patch up, test your logic design and debug. Understand how to implement simple circuits based on a schematic diagram using logic gates

Apparatus Required: -

-NAND (74NC00D_6V)
-NOR (74HC02N_6V)
-XOR (7486N0)
-XNOR (74HC266N)
-Switch
-VCC
-Ground
-Resister
-LED Light

Theory: -

NAND: -

The NAND gate is the combination of AND and NOT gate. The electric gate produces low (0) output, when all inputs are high (1), otherwise the output will be high (1). It is the complement of AND gate. It has two or more inputs and produces single output.

NOR: -

NOR gate is the combination of OR and NOT gate. This electric gate produces high (1) output when all the inputs are low (0) otherwise, output will be low (0). It is the complement of OR Gate. It has two or more inputs and produces single output.

Exclusive-OR (XOR): -

The XOR gate produces low output (0) when both the inputs are same otherwise, the output will be high (1). It can also have multiple inputs and produces single output.

Exclusive-NOR (XNOR): -

XNOR gate is equivalent to an XOR gate followed by an inverter. This gate produces high (1) output when all the inputs are either low (0) or high (1). It can also have two or more inputs and a single output.

Functional Expression: -

NAND: F= (X.Y)'
NOR: F= (X+Y)'

LAB 3:- DE Morgan's Theorem/ 3

XOR: F= X'Y+XY'
XNOR: F= X'Y'+XY

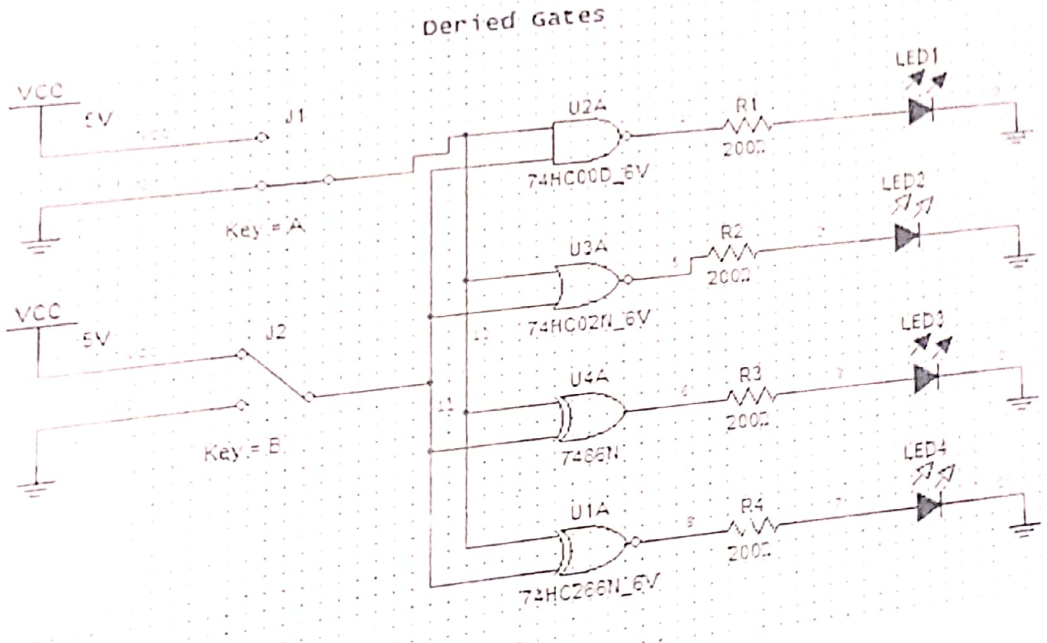
Truth Table of NAND and NOR Gate.

Input				Output 1	Output 2
X	Y	X+Y	X.Y	F=(X+Y)'	F=(X.Y)'
0	0	0	0	1	1
0	1	1	0	0	1
1	0	1	0	0	1
1	1	1	1	0	0

Truth table of XOR and XNOR Gate:

Input								Output 1	Output 2
X	Y	X'	Y'	X'Y'	XY	X'Y	XY'	F=X'Y'+ XY	F=X'Y+X Y'
0	0	1	1	1	0	0	0	1	0
0	1	1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	1	0	1
1	1	0	0	0	1	0	0	1	0

Circuit Diagram:



Conclusion:- Hence, the output of the derived gate is observed.

LAB 3:- DE Morgan's Theorem 3

Objective:-

Students will be able evaluate DE Morgan's Theorem. Moreover, DE Morgan's Theorem can help new programmers to develop correct expressions for it statements. Thus, we can use DE Morgan's Law to find the logic negation (NOT), or opposite of an expression formed with the logical operators.

Apparatus Required: -

-AND (7408J)
- OR
-NOT
-NAND
-NOR
- Switch
-VCC
-LED Light
-Ground
-Resister

Theory: -

DE Morgan's First Law: - DE Morgan's First Law states that, "The complement of a sum equals to the product of the individual complement".
i.e. (X+Y)'=X'.Y'
DE Morgan's Second Law: -DE Morgan's Second Law states that," The complement of a product is equal to the sum of individual complement".
i.e. (X.Y)'=X'+Y'

Functional Expression:-

DE Morgans's First Law: - (X+Y)'=X'.Y'
DE Morgan's Second Law: -(X.Y)'=X'+Y'

LAB 4: Decoder

Objectives:-

To use decoders to implement logic functions and to accep two or more inputs singal and generate a multibit output code.

Appratus Required: -

-AND
-NOT
-Switch
-VCC
-Ground
-LED light
-Resister

Theory: -

A decoder is the combinational circuit which has n inputs and 2^n output. A decoder is a circuit that changes a code into a set of signals. It is called decoder because it does the reverse of encoding.

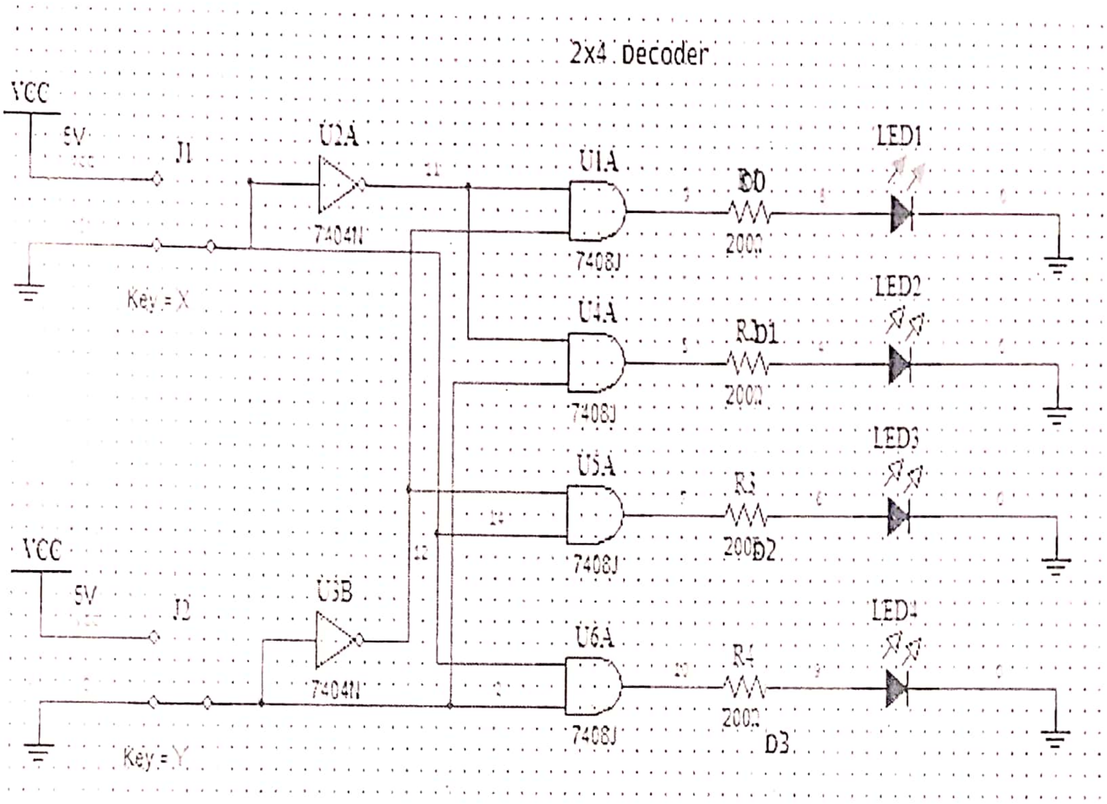
Functional Expression: -

$D_0 = X'Y'$
$D_1 = X'Y$
$D_2 = XY'$
$D_3 = XY$

Truth Table: -

Input		Output			
X	Y	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Circuit Diagram: -



Conclusion: -

Hence. The required output of decoder is observed.

LAB 5 : Encoder

Objectives:-

The objective of encoder is to standardization, speed, security, secrecy, or saving space by shrinking size.

Apparatus Required: -

-OR(7432N)
-Switch
-Resister
-Ground
-LED Light
-VCC

Theory: -

Encoder is a combinational circuit which produces n output for 2^n inputs. Encoder are combinational logic circuits and they are exactly opposite of decoders. They accept one or more inputs and generate a multiple output code.

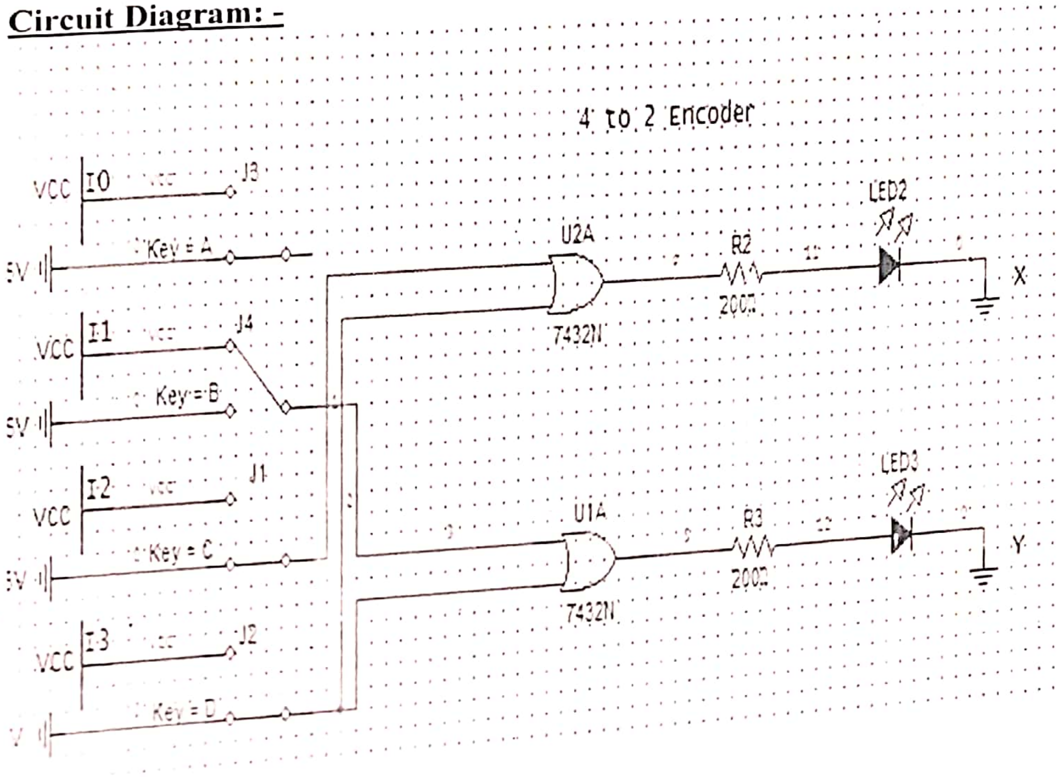
Functional Expression: -

$X= I_2+I_3$
$Y= I_1+I_3$

Truth Table: -

Input				Output	
I_0	I_1	I_2	I_3	X	Y
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

Circuit Diagram: -



Conclusion:-

Hence, required output of the encoder is observed.

LAB 6: Multiplexer

Objectives: -

The objective of this laboratory experiment is to provide students and opportunity to design basic multiplexer circuit and to implement then into a data transmission system.

Apparatus Required: -

-AND (AND3)
-NOT
-OR (OR4)
-Switch
-Resister
-Ground
-VCC
-LED Light

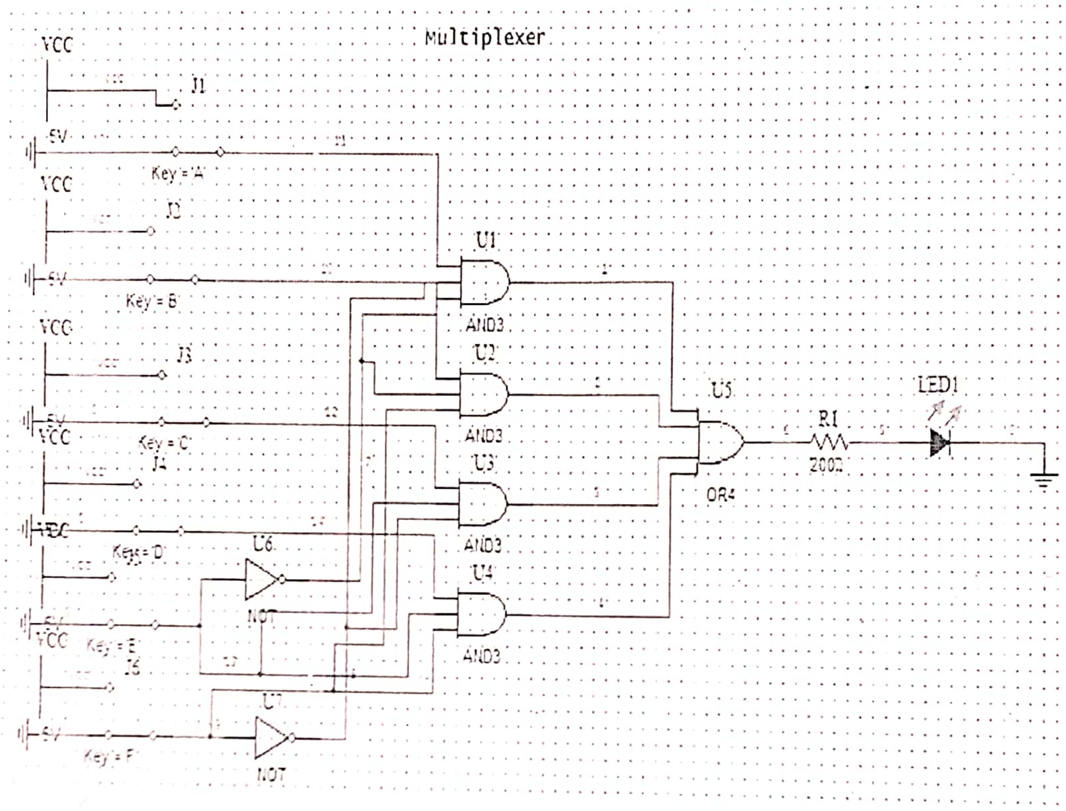
Theory: -

Multiplexer is the combinational circuit that is given a certain number (usually a power of two) data inputs, let us say 2^n , and n address inputs used as a binary number to select one of the data inputs. The multiplexer has a single output, which has the same value as the select data input.

Truth Table:-

Input		Output			
S_1	S_0	I_0	I_1	I_2	I_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Circuit Diagram: -



Conclusion: -

Hence it is concluded that the required output is generated through Multiplexer.

LAB 7 : DE multiplexer

Objectives:-

To provide students an opportunity to design basic DE multiplexer circuit and to implement them into data transmission system.

Apparatus Required: -

-NOT

-AND (AND3)

-Ground

-Resister

-VCC

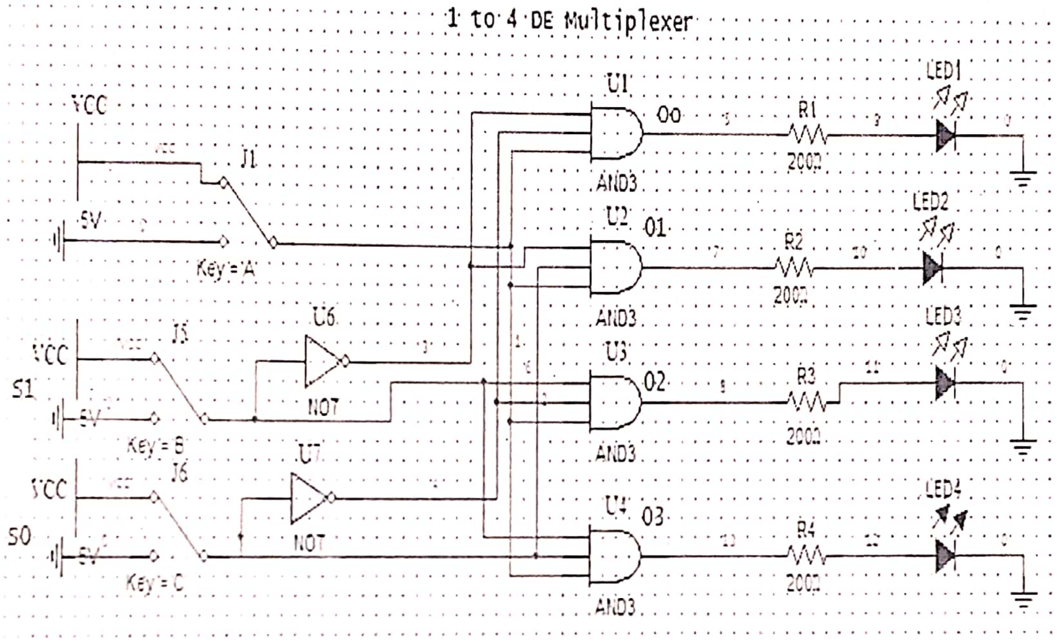
-LED Light

-Switch

Truth Table: -

Input		Output			
S_1	S_0	O_0	O_1	O_2	O_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Circuit Diagram: -



Conclusion:-

Hence. DE multiplexer can produce multiple output of single input.

LAB: 8 Full Adders

Objectives: -

The objective for this lab is to understand the design of a half adder and a full adder using logic gates and to determine the function of 'n' bit adder.

Apparatus Required: -

-Exclusive OR gate

-AND

-OR

-Resister

-Switch

-LED Light

-Ground

-VCC

Theory: -

A full adder is a logical circuit that perform s an addition operation on three binary digits. The full adder produces a sum and carry value, which are both binary digits. It can be combined with other full adders or work on its own. A full adder has three inputs A, B and a carry in C, such that multiple adders can be used to add large numbers. To remove ambiguity between the input and output carry lines, the carry in is labeled C_i and C_{in} while the carry out is labeled C_o and C_{out}.

Truth Table: -

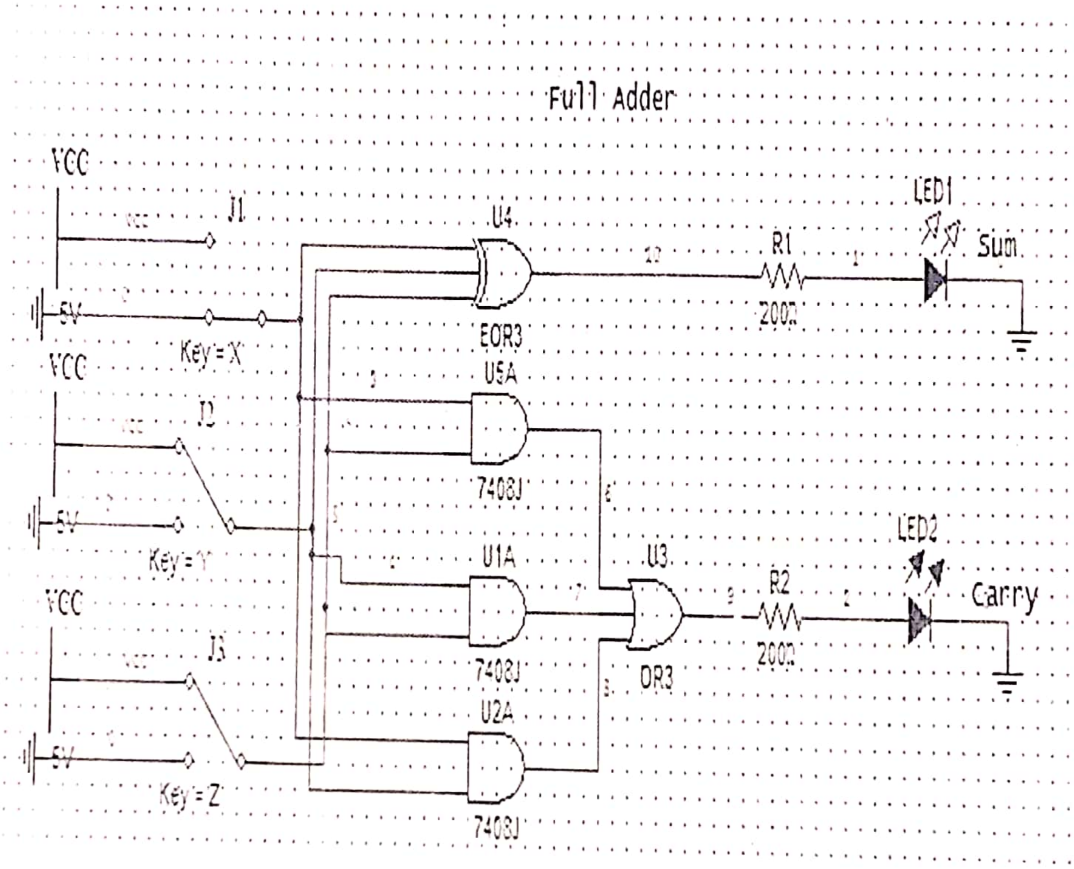
Input			Output	
X	Y	Z	Carry(c)	Sum(s)
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Equations: -

Sum Equation: - $X'Y+XY'$

Carry Equation: - $XZ+YZ+XY$

Circuit Diagram: -



Conclusion: -

Hence, the required output is generated through full adder.

LAB 9: Full Subtractor

Objectives: -

Full Subtractor is a combinational circuit that performs 1 bit subtraction with borrow-in. The Main objective of this project is to design 1-bit Full Subtract by using CMOS 180nm technology with reduced number of transistors and hence it is efficient in area, speed and power consumption.

Apparatus Required: -

-Exclusive OR gate
-AND
-OR
-Resister
-Switch
-LED Light
-Ground
-VCC

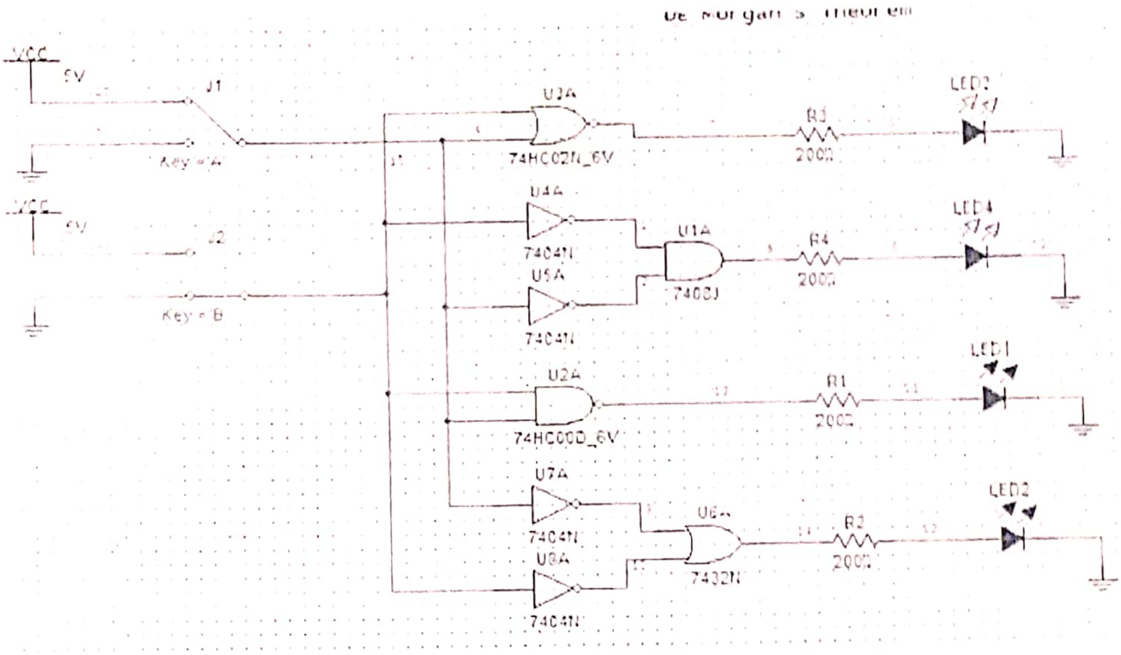
Theory: -

In electronics, a Subtractor can be designed using the same approach as that of an adder. The binary subtraction process is summarized below. As with an adder, in the general case of calculations on multi-bit numbers, three bits are involved in performing the subtraction for each but, the minuend (XI), subtrahend (YI) ad a borrow in from the previous (less significant) bit order position (BI). The output are the difference bit(DI) and borrow bit (BI+1).

Truth Table: -

Input			Output	
X	Y	Z	Carry(c)	Sum(s)
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Circuit Diagram: -



Truth Table of DE morgan's First Theorm: -

Input			Output 1			Output 2
X	Y	X+Y	(X+Y)'	X`	Y`	X`.Y`
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

Conclusion: -Comapring the values of (X+Y)' and X`.Y` From the table , both are equal . hence DE morgan's First Theoram prove.

Truth Table of DE morgan's Second Theorm: -

Input			Output 1			Output 2
X	Y	XY	(XY)'	X`	Y`	X`+Y`
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

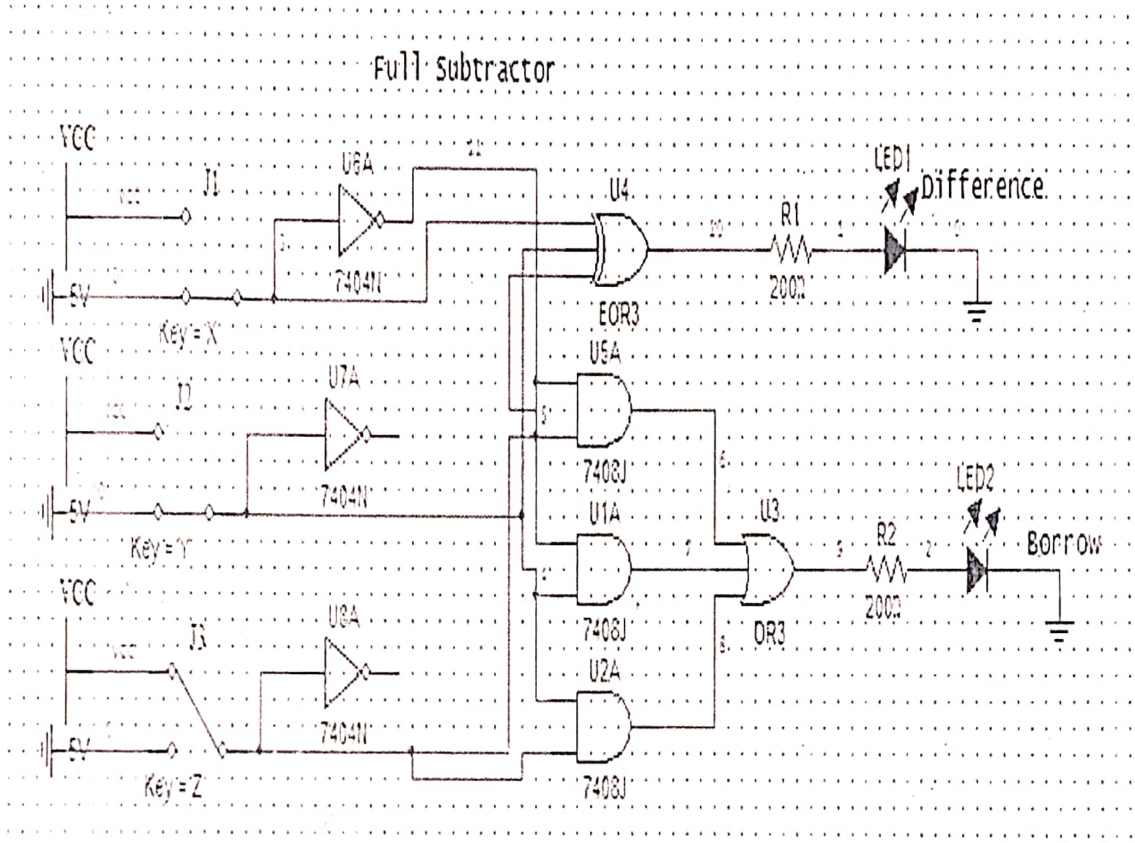
Conclusion: -Comapring the values of (X.Y)' and X`+Y` From the table , both are equal . hence DE morgan's Second Theoram prove.

Equations: -

Difference: - X’Y’+XY

Borrow: - X’Z+X’Y+YZ

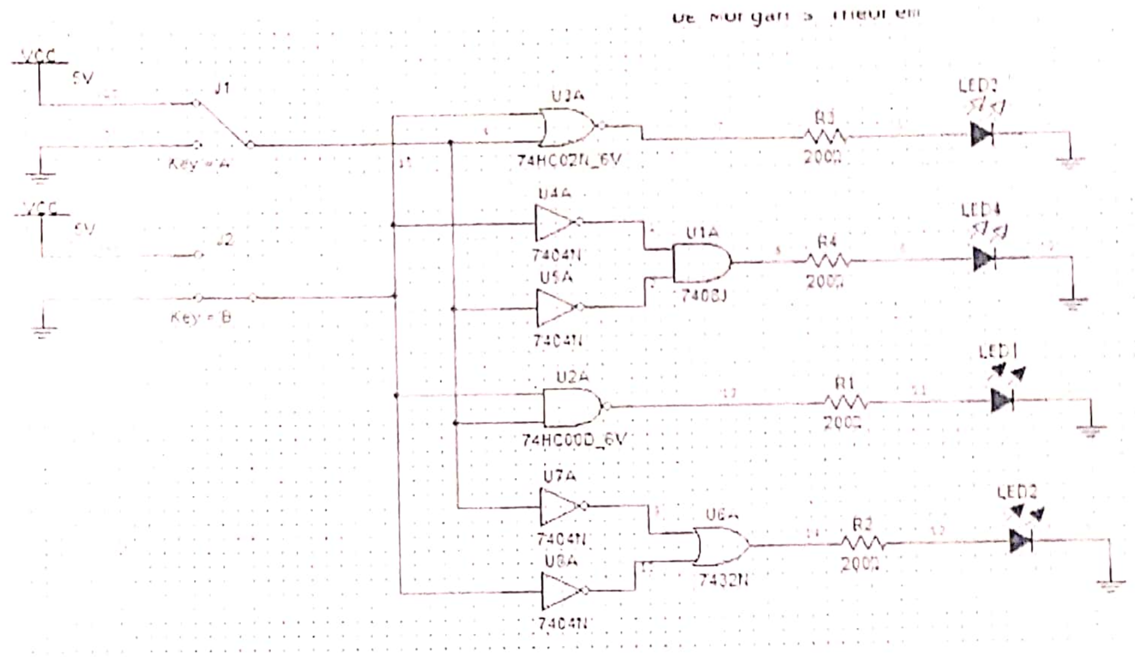
Circuit Diagram: -



Conclusion: -

Hence. the required output is generated.

Circuit Diagram: -



Truth Table of DE morgan's First Theorm: -

Input			Output 1			Output 2
X	Y	X+Y	(X+Y)'	X`	Y`	X`.Y`
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

Conclusion: -Comapring the values of (X+Y)' and X`.Y` From the table , both are equal , hence DE morgan's First Theoram prove.

Truth Table of DE morgan's Second Theorm: -

Input			Output 1			Output 2
X	Y	XY	(XY)'	X`	Y`	X`+Y`
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

Conclusion: -Comapring the values of (X.Y)' and X`+Y` From the table , both are equal , hence DE morgan's Second Theoram prove.