ST. XAVIER'S COLLEGE

MAITIGHAR, KATHMANDU

DIGITAL LOGIC PRACTICAL INDEX SHEET

BSCCSIT 1st SEMESTER

T.U. Regd. No. - …… **Class Roll No. - ……**

Name of Student - …… **Year/Sem -……..**

S.No.	Title of the Experiment	Final Submission Date	Signature	Remarks
1.	To verify the basic operation of logic gates.			
2.	To verify the operation of 3 input AND and OR gate using multiple gates.			
3.	To verify the operation of 3 input AND and OR gate using single gate.			
4.	To verify the operation of derived gates.			
5.	To verify the universality of NAND gate and NOR gate			
6.	To verify 2 and 3 variable De-Morgan's Law			
7.	To verify the operation of Half Adder circuit. To verify the operation of Full Adder circuit. To construct a Full Adder using 2 Half Adders and verify its operation.			
8.	To verify the operation of Half Subtractor circuit To verify the operation of full subtractor circuit.			
9.	To design bcd to excess 3 code converter.			
10.	To design 3-bit parity generator. To design 4-bit parity checker.			
11.	To verify the operation of 2x4 decoder To verify the operation of 3x8 decoder To verify the operation of 4x16 decoder			

12.	To verify the operation of bcd to decimal decoder			
13.	To construct a full adder using required decoders. To construct a full subtractor using required decoders.			
14.	To verify the operation of 2x1 encoder. To verify the operation of 4x2 encoder. To verify the operation of 8x3 encoder. To verify the operation of 16x4 encoder.			
15.	To construct 4 to 1 multiplexer. To construct 8 to 1 multiplexer using smaller blocks To construct 16 to 1 multiplexer using smaller blocks			
16.	To construct 1x4 demultiplexer To construct 1x8 demultiplexer using smaller blocks. To construct 1x16 demultiplexer using smaller blocks			
17.	To construct Serial In Serial Out Shift Register To construct Serial In parallel Out Shift Register To construct Parallel In Serial Out Shift Register. To construct Parallel In Parallel Out Shift Register.			
18.	To construct a 2-bit asynchronous counter To construct a 4-bit asynchronous counter			
19.	To construct a BCD asynchronous counter			
20.	To construct a 2-bit synchronous counter To construct a 4-bit synchronous counter			
21.	To construct a BCD synchronous counter			