TRIBHUVAN UNIVERSITY

Institution of Science and Technology

Course Title: Digital Logic
Course No.:CSC111
Nature of the Course: Theory + Lab
Semester: I

Full Marks: 60
Pass Marks: 24
Time: 3

Digital Logic

TU QUESTIONS-ANSWERS 2075

Attempt any TWO questions: **2×10=20**

1. **Implement the following function F = Σ(1, 2, 3, 4, 8) using**
   (a) Decoder
   (b) Multiplexer
   (c) PLA

Ans: (a) Given function F = Σ(1, 2, 3, 4, 8)

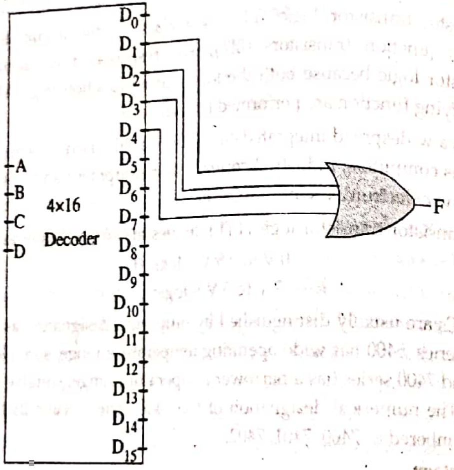


Figure: Implementation of given function using 4×16 Decoder

(b) Let's new take the variable A for input lines and B, C & D to n selection lines

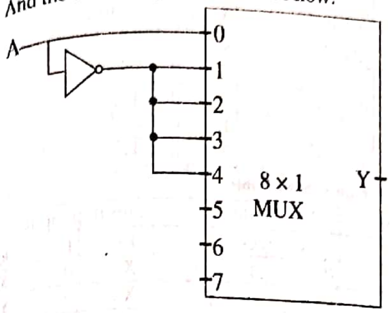
N = 4 so MUX is $2^{N4} = 2^3 = 8 \times 1$

So minterms with A complement term are 0-7

So we list the MIN TERMS as

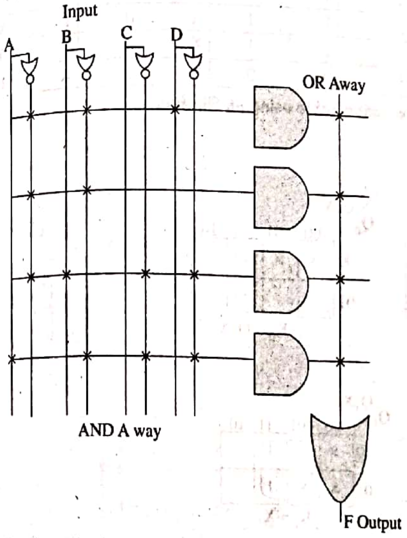
	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
A'	0	①	②	③	④	5	6	7
A	⑧	9	10	11	12	13	14	15
	A	A'	A'	A'	A'	0	0	0

And the circuit diagram is shown below:

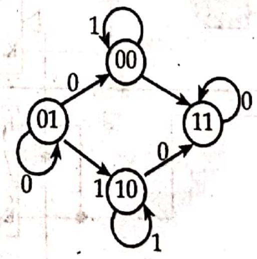


(c) $F = \bar{A}\,\bar{B}\,D = \bar{A}\,\bar{B}\,C + \bar{A}\,\bar{B}\,\bar{C}\,\bar{D} + \bar{A}\,\bar{B}\,\bar{C}\,\bar{D}$

AB \ CD	00	01	11	10
00		1	1	1
01	①			
	①			



2. **Design clocked sequential circuit of the following state diagram by using JK flip-flop.**



Ans: From the state diagram two flip-flops are needed to represent the four states and are designated Q_0Q_1. The input variable is labelled x.

Present state		Next state			
		X = 0		X = 1	
Q_0	Q_1	Q_0	Q_1	Q_0	Q_1
0	0	0	1	0	0
0	1	0	1	1	0
1	0	1	1	1	0
1	1	1	1	0	0

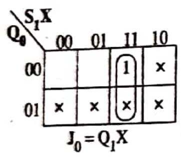
Figure: State Table

Present state		Input	Next state		Flip-flop inputs			
Q_0	Q_1	x	Q_0	Q_1	J_0	k_0	J_1	k_0
0	0	0	0	1	0	X	0	X
0	0	1	0	0	0	X	0	X
0	1	0	0	1	0	X	X	0
0	1	1	1	0	1	X	X	1
1	0	0	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

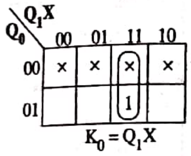
Figure: Excitation Table using j-k Flip-flops

k-map simplification

For J_0:

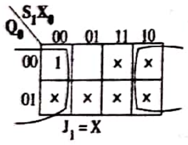


$J_0 = Q_1X$

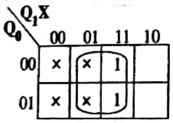


$K_0 = Q_1X$

For J_1:



$J_1 = X$



$K_1 = X$

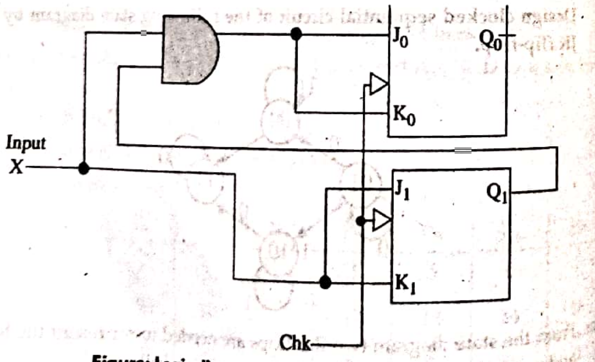


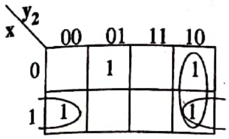
Figure: Logic diagram of the sequential circuit

3. **The following is a truth a table of a 3-input combinational circuit. Tabulate the PAL programming table for the circuit and mark the fuses to be blow in a PAL diagram.**

Inputs			Outputs			
X	Y	Z	A	B	C	D
0	0	0	0	0	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

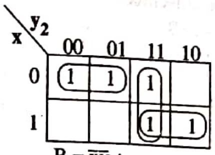
Ans: K-map simplification for four outputs A, B, C & D_0

For A



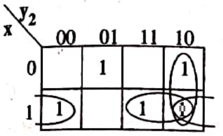
$A = x\bar{z} + y\bar{z} + \bar{x}\bar{y}z$

For B



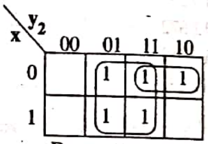
$B = \overline{xy} + yz + xy$

For C:



$C = x\bar{z} + xy + y\bar{z} + \bar{x}\bar{y}z$

For D:



$D = z + \bar{x}y$

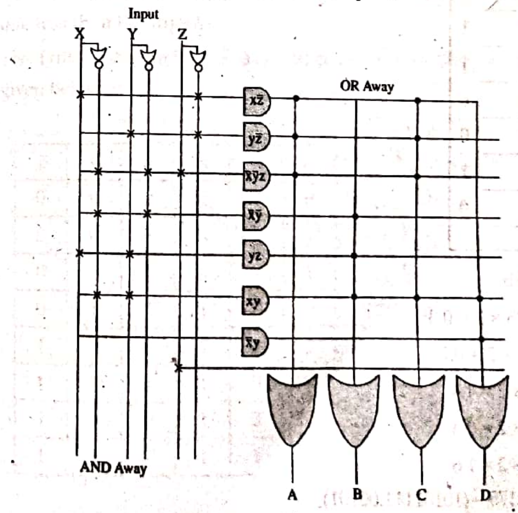


Fig: PAL diagram

Attempt any EIGHT questions. **8×5=40**

4. **Convert the following decimal numbers to the indicated bases.**

   (a) 7562.45 to octal

   (b) 1938.257 to hexadecimal

   (c) 175.175 to binary

Ans: (a) 7562.45 to octal

```
8 |7562   2 ↑LSB
8 |945    1 |
8 |118    6 |
8 |14     6 |
   1 _______|
   MSB
```

Also,

(b) 1938.257 to hexadecimal

```
16 |1938   2 ↑LSB
16 |121    9 |
    7 ______|
    MSB
```

Also,

$0.257 \times 16 = 4.112$

$0.112 \times 16 = 1.729$

$0.792 \times 16 = 12.672$

$0.672 \times 16 = 10.752$

$\therefore 1938.257 = (792.41CA)_{16}$

(c) 175.175 to binary

```
2 |175   1 ↑LSB
2 |87    1 |
2 |43    1 |
2 |21    6 |
2 |10    0 |
2 |5     1 |
2 |2     0 |
   1 ______|
   MSB
```

Also, $0.175 \times 2 = 0.35$

$0.35 \times 2 = 0.7$

$0.7 \times 2 = 1.4$

$0.4 \times 2 = 0.8$

$0.8 \times 2 = 1.6$

$\therefore \quad 175.175 = (10101111.00101)_2$

5. **Express the Boolean function F = A = B' C in sum of minterms**

Ans: Given function F = A + B'C

= A(B + B') + B'C(A + A') [∵ A + A' = 1]

= AB + AB' + AB'C + A'B'C

= (AB + AB') + (C + C') + AB'C + A'B'C

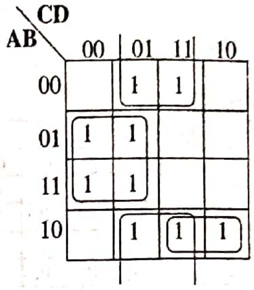
= ABC + ABC' + AB'C + AB'C' + AB'C + A'B'C

= ABC + ABC' + AB'C + AB'C' + A'B'C

6. **Reduce the following function using k-map**

   F = B'D + A'BC' + AB'C + ABC'.

Ans: Given function F = B'D + A'BC' + AB'C + ABC'



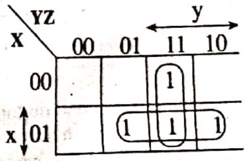
AB \ CD	00	01	11	10
00		1	1	
01	1	1		
11	1	1		
10		1	1	1

$F = B\bar{C} + \bar{B}D + A\overline{\overline{B}}C$

7. **Design a combinational circuit with three inputs x, y and z and three outputs, A, B and C. When the binary input 4, 5, 6 or 7 the binary output is one less than the input.**

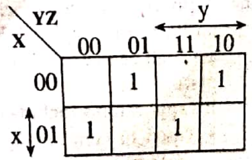
Ans: The Truth Table and it's K-map simplification for the given statement is as given below:

x	y	z	A	B	C
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0



X \ YZ	00	01	11	10
00			1	
01		1	1	1

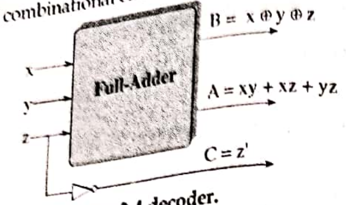
A = xy + xz + yz



X \ YZ	00	01	11	10
00		1		1
01	1		1	

B = x ⊕ y ⊕ z C = z'

Implementation of combinational circuit



8. **Implement half adder using 2-4 decoder.**

Ans: Implementation of Half Adder with 2x4 Decoder.

Truth Table of Half Adder

i/p's		o/p's	
x	y	S_{HA}	C_{HA}
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth Table of 2X4 Decoder

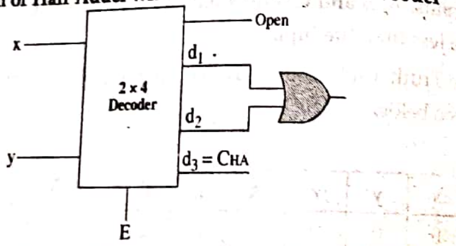
i/p's		o/p's			
x	y	d_0	d_1	d_2	d_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

By comparing Truth Tables of half Adder and 2 X 4 Decoder.

We can see that $S_{HA} = d_1 + d_2$

$C_{HA} = d_3$

Block Diagram of Half Adder with Truth Table of 2X4 Decoder



Note: By connecting an OR gate with output Pin 1 & 2 of 2X4 Decoder. Half Adder can be implemented with 2X4 decoder. Similarly by connecting two Half Adders, we can form a Full Adder by using 2, 2X4 Decoder IC's.

9. **Design the priority encoder circuit.**

Ans: A priority encoder provide n bits of binary coded output representing the position of the highest order active input of 2n inputs. If two or more inputs are high at the same time, the input having the highest priority will take precedence.

It's applications includes

- used to control interrupt requests by acting on the highest priority request
- to encode the output of a flash analog to digital converter

4 to 2 priority encoder

A 4-to-2 priority encoder takes 4 input bits and produces 2 output bits. In this truth table, for all the non-explicitly defined input combinations (i.e. inputs containing 2, 3, or 4 high bits) the lower priority bits are shown as don't cares (X). Similarly when the inputs are 0000, the outputs are not valid and therefore they are XX.

Truth Table

I3	I2	I1	I0	O1	O0
0	0	0	0	X	X
0	0	0	1	0	0
0	0	1	X	0	1
0	1	X	X	1	0
1	X	X	X	1	1

From the above truth table, we can obtain the full truth table required for our design.

Truth Table

I3	I2	I1	I0	O1	O0
0	0	0	0	X	X
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

From this truth table, we use the Karnaugh Map to minimise the logic to the following boolean expressions:

- O1 = I2 + I3
- O0 = ~I2 * I1 + I3

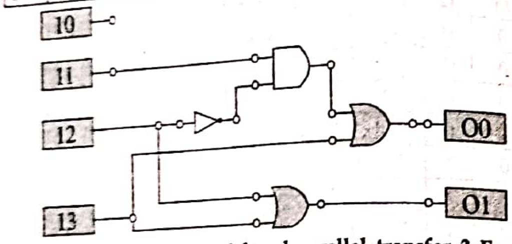
Implementation of the 4 to 2 priority encoder using combinational logic circuits.

Bool Expression

O1 = (I2 + I3)

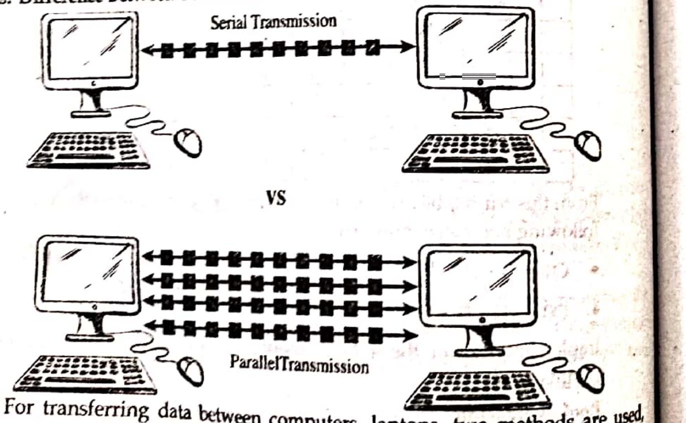
O0 = (~ I2 * I1 + I3)

I3	I2	I1	I0	O1	O0
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1



10. What is the difference a serial and parallel transfer ? Explain how to convert serial data to parallel and parallel data to serial. What type of register is needed ?

Ans: Difference Between Serial and Parallel Transmission



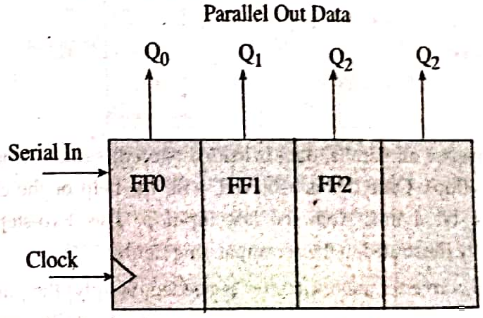
For transferring data between computers, laptops, two methods are used, namely, Serial Transmission and Parallel Transmission. There are some similarities and dissimilarities between them. One of the primary difference is that; in Serial Transmission, data is sent bit by bit whereas, in Parallel Transmission a byte (8 bits) or character is sent at a time.

Basis for Comparison	Serial Transmission	Parallel Transmission
Meaning	Data flows in bi-direction, bit by bit	Multiple lines are used to send data, i.e. 8 bits or 1 byte at a time.
Cost	Economical	Expensive
Bits transferred at a 1 clock pulse	1 bit	8 bits or 1 byte
Speed	Slow	Fast
Applications	Used for long-distance communication. E.g., computer to computer	Short distance E.g., computer to a printer
Number of communication channel required	Only one	N number of communication channels are needed
Need of converters	Required to convert the signals according to the need.	Not required.

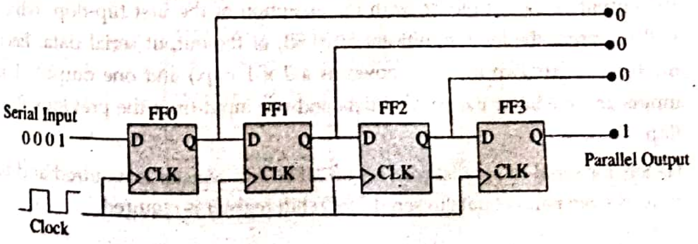
Conversions

Serial to Parallel Conversion

To convert serial data to parallel data a set of D flip-flops is needed. The number of flip-flops is exactly the size of the serial data to be transmitted. For example, to transmit four-bit serial stream four flip-flops a required. A schematic of a four-bit converter is depicted.



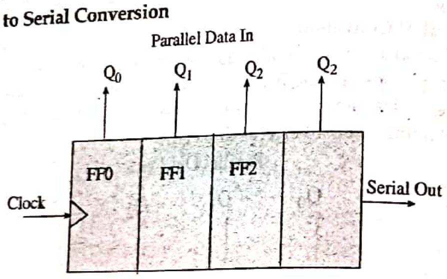
The serial data is delivered at the input of the first flip-flop, and bits are successfully transferred to the next flip-flop on the rising (or falling) edge of the clock. The next figure shows an actual circuit for a four-bit converter, where four bits (0, 0, 0, and 1) are stored at the input of the first flip-flop.



With the first rising edge (i.e. tick) of the clock, the first bit (1 in this case) is transferred to the input of the second flip-flop. Successive ticks moves the bits to the next flip-flop, until all four bits are stored at the output of each flip-flop. In this figure we have not shown all the circuitry of an actual converter. The converter does not release the parallel set of bits until all the bits (four in this case) are transferred, and each one is stored at the output (Q) of a corresponding flip-flop. Once all the outputs are filled, the converter releases all the bits at once. For this process to happen, the converter is disabled (by means of one or more control lines) during the transfer process and enabled once all the bits are at the output bus. This is summarized by stating that the conversion is carried out in three stages:

1. Disable the output bus. The converter can't send output data.
2. Load all the bits into the outputs of the flip-flops by moving them one bit at a time using the clock.
3. Once all the bits are loaded (all the flip-flops have one bit stored in the Q pin), then enable the bus operation. The four bits are sent at once.

Parallel to Serial Conversion



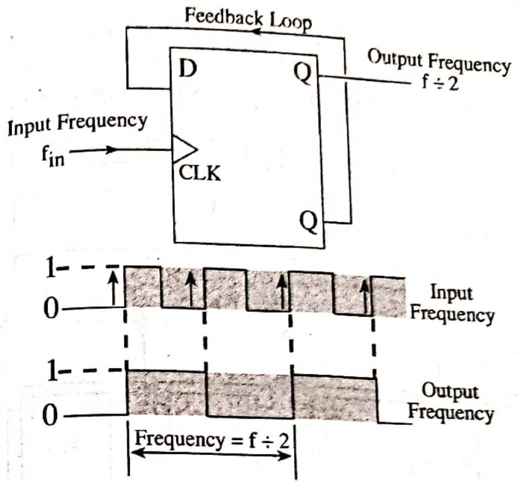
In this converter all parallel data is loaded (stored) simultaneously into the D-type flip-flops. Once this is achieved, with the help of the clock, data is shifted one bit a time from the last flip-flop. This two-step process is schematically illustrated in the accompanying figure.

In an actual converter, more circuitry is needed. Simply, the parallel data is multiplexed in order to convert it into serial data. The multiplexer will force the parallel data to be shifted one bit at a time through the last (most significant bit) flip-flop. The following figure is the diagram of a four bit converter. There are four flip-flops and three multiplexers. Each flip-flop is the output of a multiplexer, with the exception of the first flip-flop, which will represent the least significant bit (LSB) of the output serial data. Each multiplexer has two inputs (known as a 2 x 1 mux) and one output. The inputs are one bit of the parallel data and one input from the previous flip-flop.

Hence, for serial to parallel conversion SIPO shift register is required and to convert from parallel data to serial PISO shift register is required.

11. **Design a 4-bit binary ripple counter with D flip-flops.**

Ans:

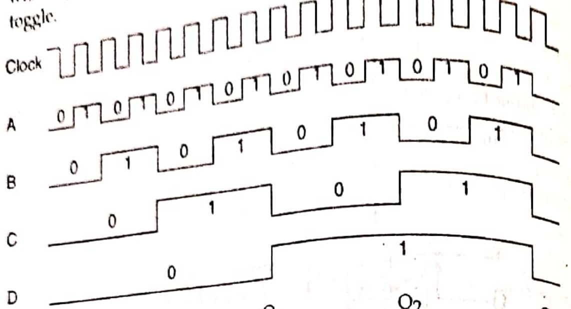


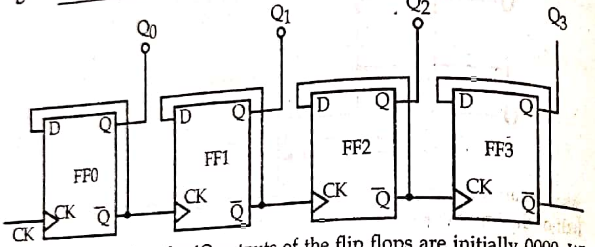
As you can see, the Frequency of Output (Q) and the feedback loop (~Q) is half of the input clock.

As I mentioned before, this circuit is a T_FF too. so the output will toggle in every cycle. (it will change between 0 & 1).

	toggle Frequency			
	f/16	f/8	f/4	f/2
	↓	↓	↓	↓
Decimal	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

As you can see in the table above, the terminal A changes between 0 and 1 with a speed equivalent to f/2. So as Terminal B is 0, we have enough time to toggle.





Let us assume that the 4Q outputs of the flip flops are initially 0000. When the rising edge of the clock pulse is applied to the FF0, then the output Q0 will change to logic 1 and the next clock pulse will change the Q0 output to logic 0. this means the output state of the clock pulse toggles (changes from 0 to 10 for one cycle.

As the Q of FF0 is connected to the clock input of FF1, then the clock input of second flip flop will become 1. This makes the output of FF1 to be high (i.e. Q1 = 1), which indicates the value 20. In this way the next clock pulse will make the Q0 to become high again.

So now both Q0 and Q1 are high, this results in making the 4 bit output 11002. Now if we apply the fourth clock pulse, it will make the Q0 and Q1 to low state and toggles the FF2. So the output Q2 will become 0010-2.

12. **Write short notes (Any TWO)**

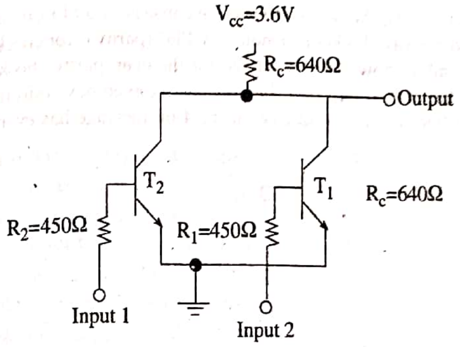
(a) SIMM

Ans: A SIMM (single in-line memory module) is a module containing one or several random access memory (RAM) chips on a small circuit board with pins that connect to the computer motherboard. Since the more RAM your computer has, the less frequently it will need to access your secondary storage (for example, hard disk or CD-ROM), PC owners sometimes expand RAM by installing additional SIMMs. SIMMs typically come with a 32 data bit (36 bits counting parity bits) path to the computer that requires a 72-pin connector. SIMMs usually come in memory chip multiples of four megabytes.

The memory chips on a SIMM are typically dynamic RAM (DRAM) chips. An improved form of RAM called Synchronous DRAM (SDRAM) can also be used. Since SDRAM provides a 64 data bit path, it requires at least two SIMMs or a dual in-line memory module (DIMM).

(b) RTL

Ans: **Resistor-Transistor Logic (RTL) family**



The resistor-transistor logic, also termed as RTL, was most popular kind of logic before the invention of IC fabrication technologies. As its name suggests, RTL circuits mainly consists of resistors and transistors that comprises RTL devices. The basic RTL device is a NOR gate, shown in figure aside.

Inputs to the NOR gate shown above are 'input1' & 'input2'. The inputs applied at these terminals represent either logic level HIGH (1) or LOW (0). The logic level LOW is the voltage that drives corresponding transistor in cut-off region, while logic level HIGH drives it into saturation region. If both the inputs are LOW, then both the transistors are in cut-off i.e. they are turned-off. Thus, voltage Vcc appears at output I.e. HIGH.

If either transistor or both of them are applied HIGH input, the voltage Vcc drops across Rc and output is LOW. RTL family is characterized by poor noise margin, poor fan-out capability, low speed and high power dissipation. Due to these undesirable characteristics, this family is now obsolete.

(c) Parity Checker

Ans: It is a logic circuit that checks for possible errors in the transmission. This circuit can be an even parity checker or odd parity checker depending on the type of parity generated at the transmission end. When this circuit is used as even parity checker, the number of input bits must always be even.

When a parity error occurs, the 'sum even' output goes low and 'sum odd' output goes high. If this logic circuit is used as an odd parity checker, the number of input bits should be odd, but if an error occurs the 'sum odd' output goes low and 'sum even' output goes high.

Even Parity Checker

Consider that three input message along with even parity bit is generated at the transmitting end. These 4 bits are applied as input to the parity checker circuit which checks the possibility of error on the data. Since the data is transmitted with even parity, four bits received at circuit must have an even number of 1s.

If any error occurs, the received message consists of odd number of 1s. The output of the parity checker is denoted by PEC (parity error check).

The below table shows the truth table for the even parity checker in which PEC = 1 if the error occurs, i.e., the four bits received have odd number of 1s and PEC = 0 if no error occurs, i.e., if the 4-bit message has even number of 1s.

❑❑❑