Tribhuvan University
Institute of Science and Technology
2066

Bachelor Level/ First Year/ First Semester/ Science — Full Marks: 60
Computer Science and Information Technology (CSc. 111) — Pass Marks: 24
(Digital Logic) — Time: 3 hours.

Candidates are required to give their answers in their own words as for as practicable.
The figures in the margin indicate full marks.

Long Questions:

Attempt any two questions: (2 × 10=20)

1. Design the 4-bit synchronous up/down counter with timing diagram, logic diagram and truth table.
2. Design a full subtractor with truth table and logic gates.
3. Design a decimal adder with logical diagram and truth table.

Short Questions:

Attempt any eight questions: (8 × 5=40)

4. Differentiate between Analog and Digital system.
5. Convert the following octal numbers to hexadecimal.
   a. 1760.46
   b. 6055.263
6. Which gates can be used as inverts in additional to the NOT gate and how?
7. Draw a logic gates that implements the following
   a) $A = (Y_1 \oplus Y_2)\,(Y_3 \odot Y_4) + (Y_5 \oplus Y_6 \oplus Y_7)$
   b) $A = (X_1 \odot X_2) + (X_3 \odot X_4) + (X_4 \odot X_5) \oplus (X_4 \odot X_7)$
8. State and prove De-Morgan's theorem 1st and 2nd with logic gates and truth table.
9. Reduce the following expressions using K-map

$$\overline{A} + B(A + \overline{B} + D)(\overline{B} + C)(B + C + D)$$

10. Differentiate between a MUX and a DEMUX.
11. Explain the operation of Decoder.
12. What are the various types of shift registers?
13. What do you mean by Synchronous counter?