ASSIGNMENT OF 25 PROGRAMS

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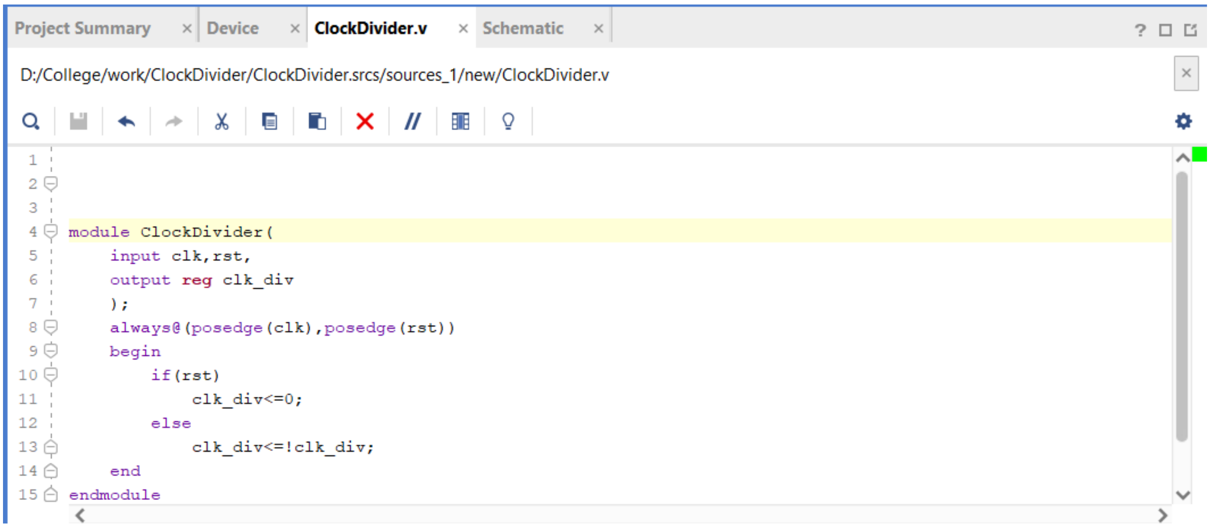
1. Clock Divider :-

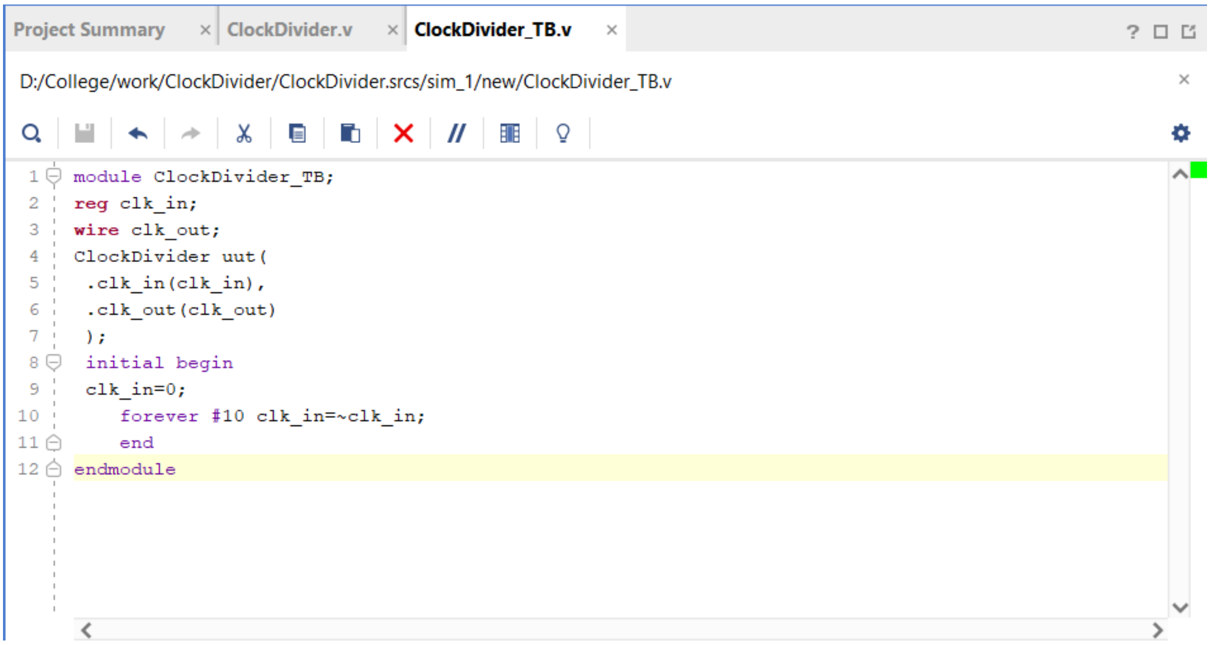
Verilog Code:



D:/College/work/ClockDivider/ClockDivider.srcs/sources_1/new/ClockDivider.v

```



module ClockDivider(
    input clk,rst,
    output reg clk_div
    );
    always@(posedge(clk),posedge(rst))
    begin
        if(rst)
            clk_div<=0;
        else
            clk_div<=!clk_div;
    end
endmodule
```

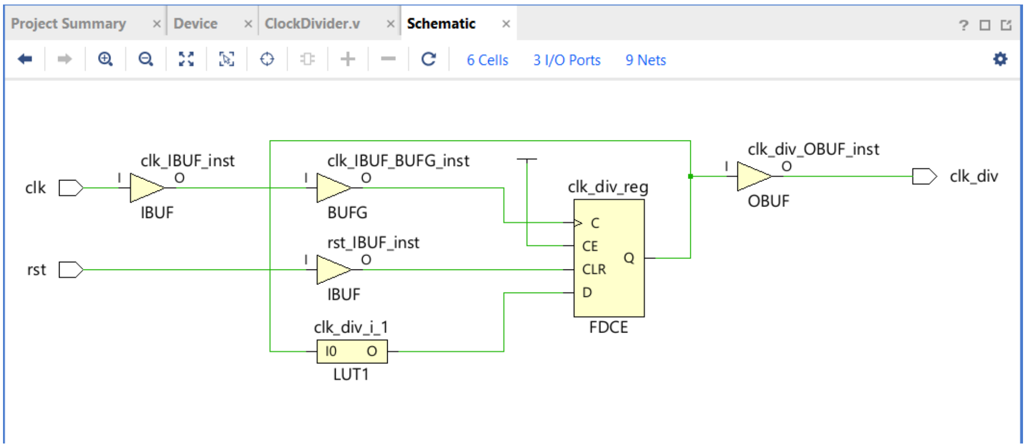
Test Bench:



D:/College/work/ClockDivider/ClockDivider.srcs/sim_1/new/ClockDivider_TB.v

```
module ClockDivider_TB;
reg clk_in;
wire clk_out;
ClockDivider uut(
 .clk_in(clk_in),
 .clk_out(clk_out)
 );
 initial begin
 clk_in=0;
    forever #10 clk_in=~clk_in;
    end
endmodule
```

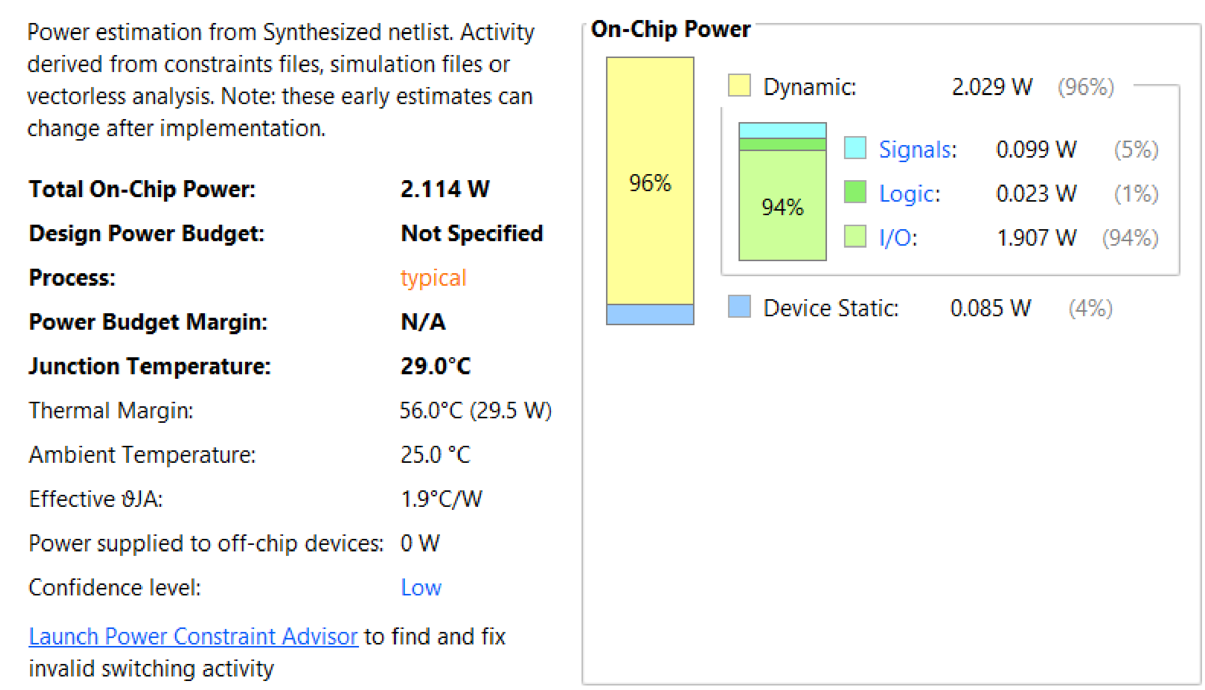
RTL Schematic:



Synthesis Report:

```
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+-----------+
| |BlackBox name |Instances |
+-+--------------+-----------+
+-+--------------+-----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT1 |     1|
|3     |FDCE |     1|
|4     |IBUF |     2|
|5     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     6|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:13 ; elapsed = 00:00:13 .
---------------------------------------------------------------------------------
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**2.114 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**29.0°C**
Thermal Margin:	56.0°C (29.5 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

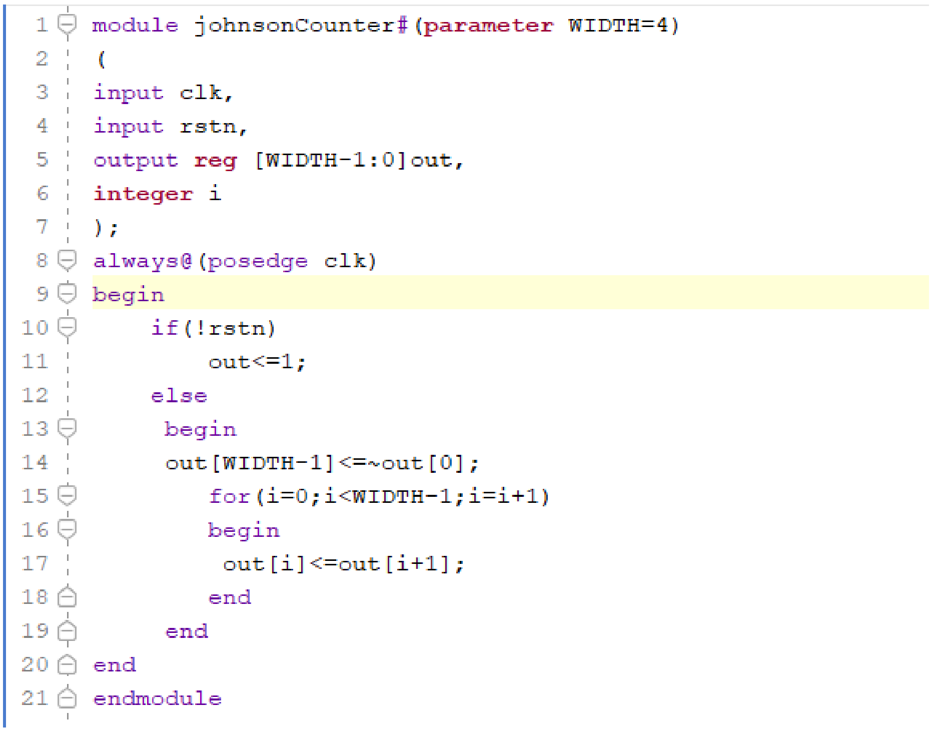
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨 Dynamic:	2.029 W	(96%)
🟦 Signals:	0.099 W	(5%)
🟩 Logic:	0.023 W	(1%)
🟩 I/O:	1.907 W	(94%)
🟦 Device Static:	0.085 W	(4%)

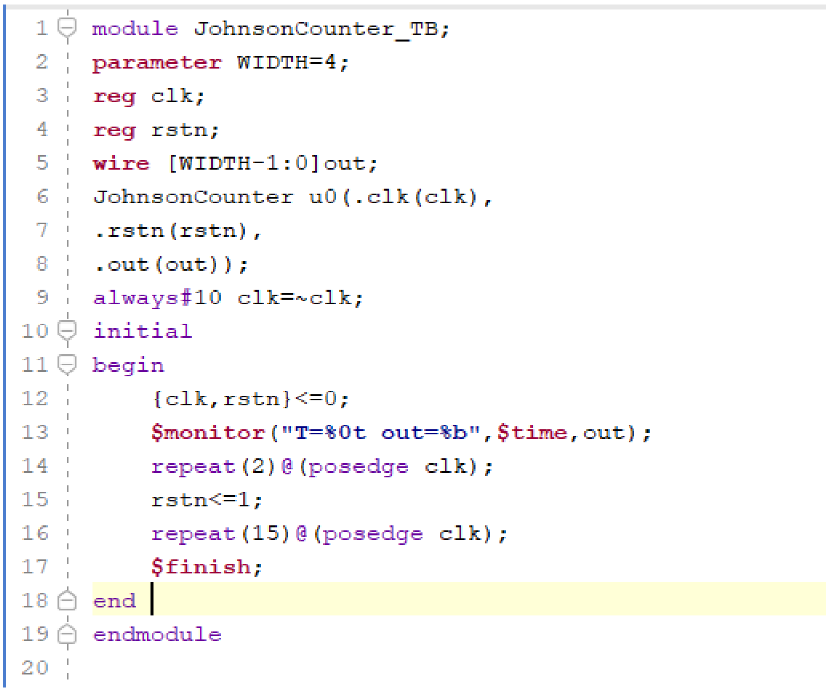
2. Johnson Counter :-

Verilog Code:



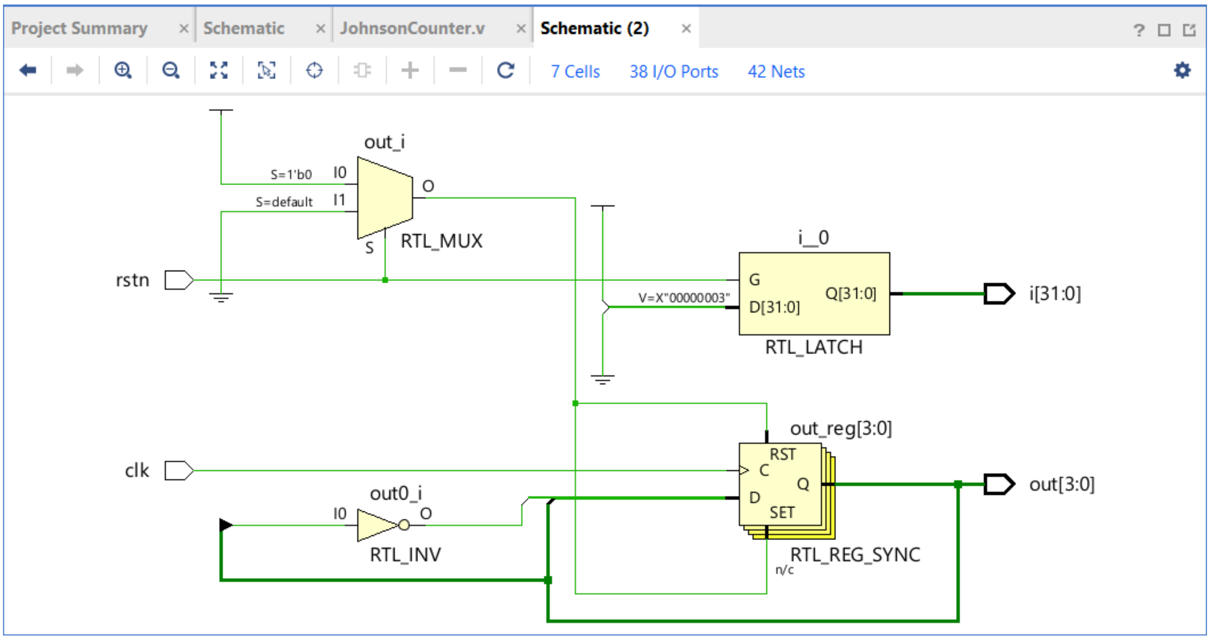
```
module johnsonCounter#(parameter WIDTH=4)
(
input clk,
input rstn,
output reg [WIDTH-1:0]out,
integer i
);
always@(posedge clk)
begin
    if(!rstn)
        out<=1;
    else
     begin
     out[WIDTH-1]<=~out[0];
        for(i=0;i<WIDTH-1;i=i+1)
        begin
         out[i]<=out[i+1];
        end
     end
end
endmodule
```

Test Bench:



```
module JohnsonCounter_TB;
parameter WIDTH=4;
reg clk;
reg rstn;
wire [WIDTH-1:0]out;
JohnsonCounter u0(.clk(clk),
.rstn(rstn),
.out(out));
always#10 clk=~clk;
initial
begin
    {clk,rstn}<=0;
    $monitor("T=%0t out=%b",$time,out);
    repeat(2)@(posedge clk);
    rstn<=1;
    repeat(15)@(posedge clk);
    $finish;
end
endmodule

```

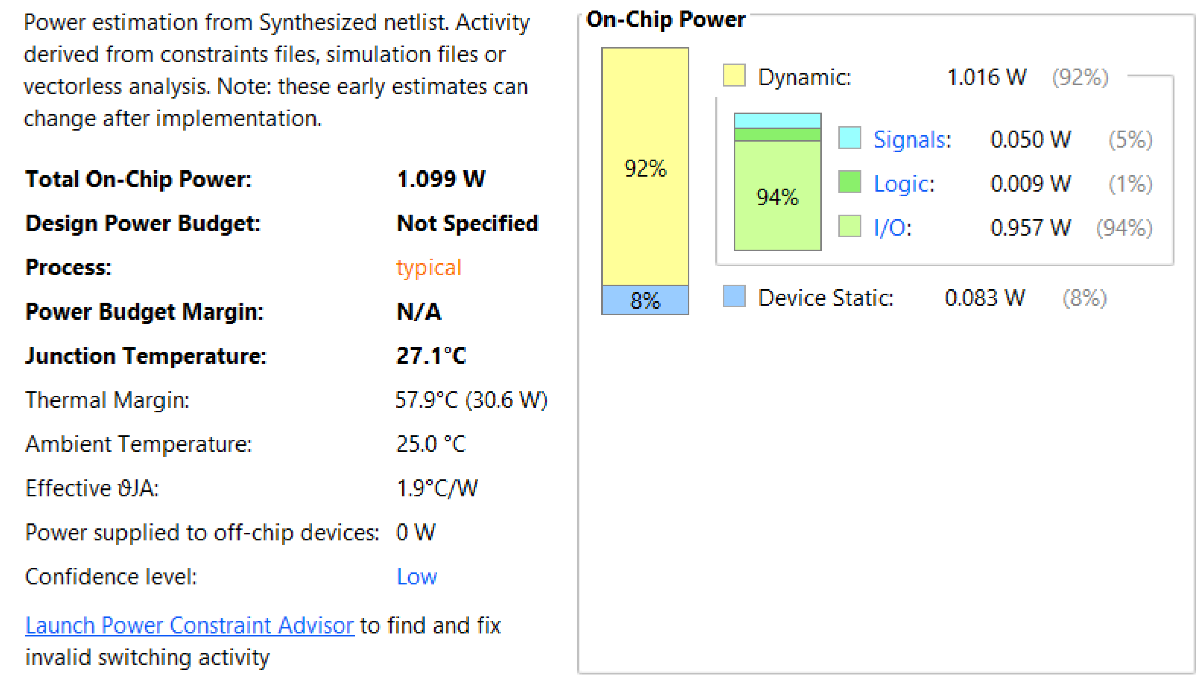
RTL Schematic:



Synthesis Report:

```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT1 |     2|
|3     |FDRE |     3|
|4     |FDSE |     1|
|5     |IBUF |     2|
|6     |OBUF |    36|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    45|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:16 ; elapsed = 00:00:16 .
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.099 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**27.1°C**
Thermal Margin:	57.9°C (30.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

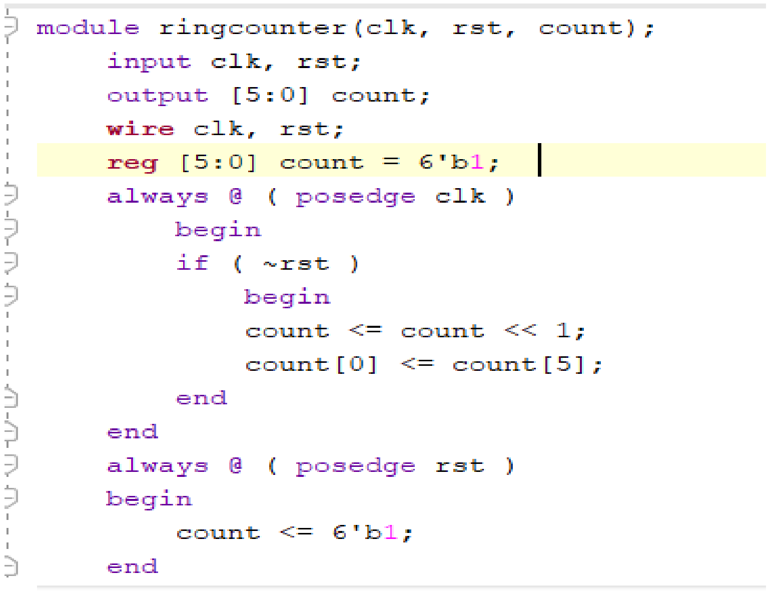
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨	Dynamic:	1.016 W	(92%)
🟦	Signals:	0.050 W	(5%)
🟩	Logic:	0.009 W	(1%)
🟩	I/O:	0.957 W	(94%)
🟦	Device Static:	0.083 W	(8%)

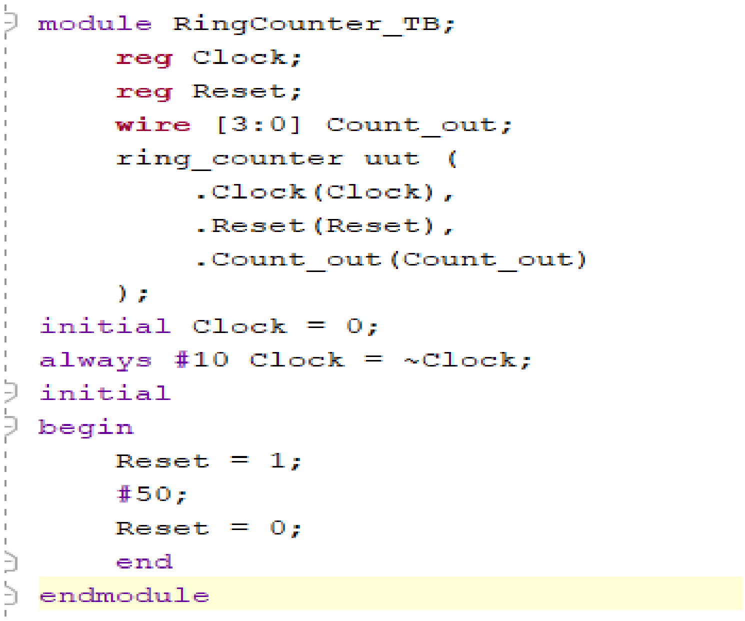
3. Ring Counter :-

Verilog Code:



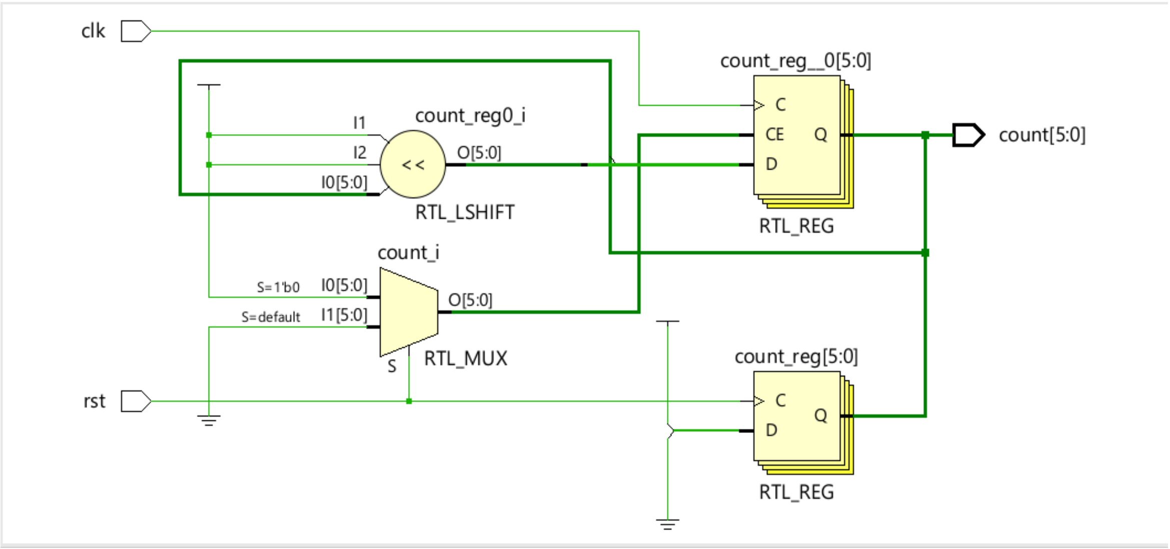
```
module ringcounter(clk, rst, count);
    input clk, rst;
    output [5:0] count;
    wire clk, rst;
    reg [5:0] count = 6'b1;
    always @ ( posedge clk )
        begin
        if ( ~rst )
            begin
            count <= count << 1;
            count[0] <= count[5];
        end
    end
    always @ ( posedge rst )
    begin
        count <= 6'b1;
    end
```

Test Bench:

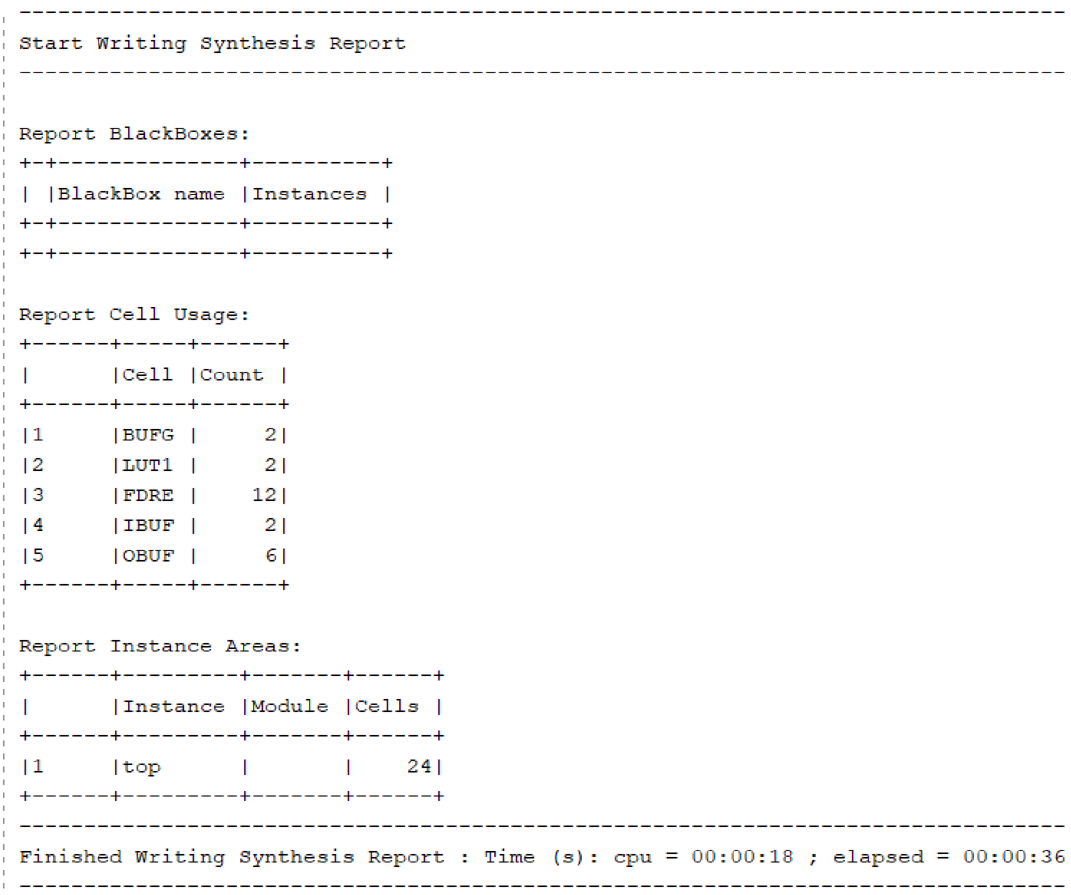


```
module RingCounter_TB;
    reg Clock;
    reg Reset;
    wire [3:0] Count_out;
    ring_counter uut (
        .Clock(Clock),
        .Reset(Reset),
        .Count_out(Count_out)
    );
initial Clock = 0;
always #10 Clock = ~Clock;
initial
begin
    Reset = 1;
    #50;
    Reset = 0;
    end
endmodule
```

RTL Schematic:

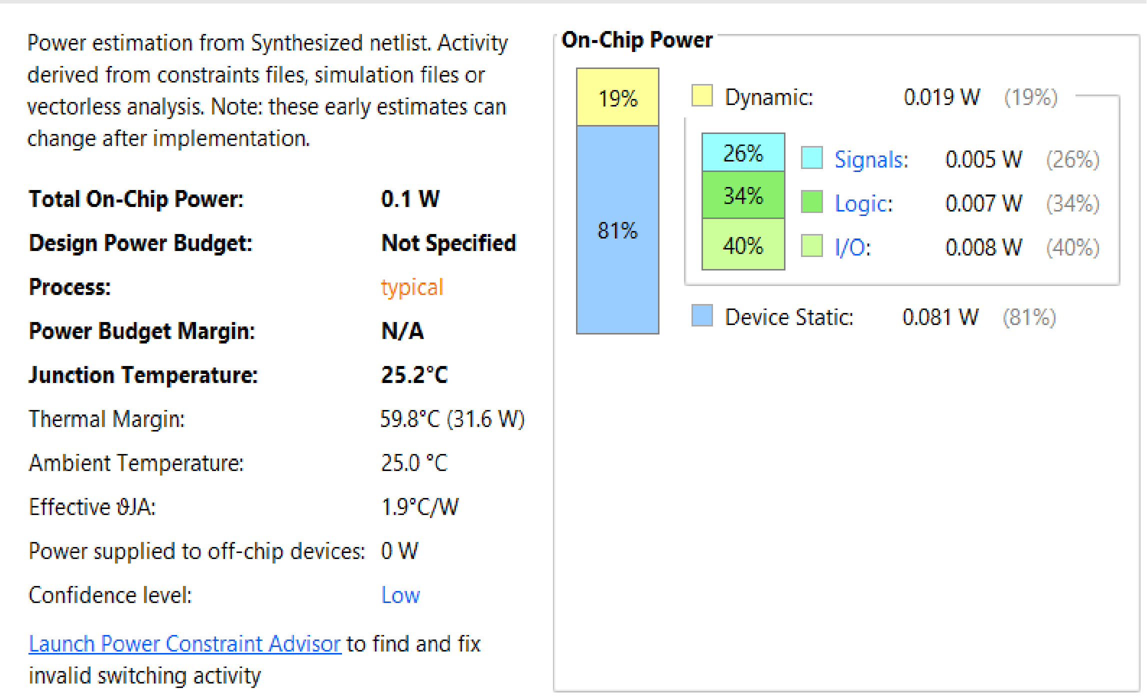


Synthesis Report:



```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     2|
|2     |LUT1 |     2|
|3     |FDRE |    12|
|4     |IBUF |     2|
|5     |OBUF |     6|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    24|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:18 ; elapsed = 00:00:36
---------------------------------------------------------------------------------
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.1 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.2°C**
Thermal Margin:	59.8°C (31.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

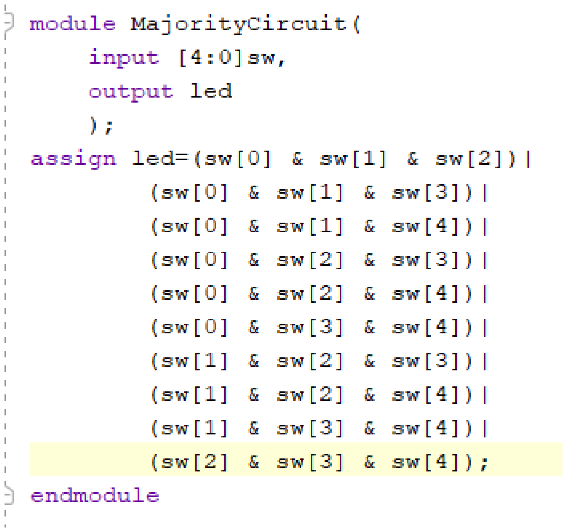
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨	Dynamic:	0.019 W	(19%)
🟦	Signals:	0.005 W	(26%)
🟩	Logic:	0.007 W	(34%)
🟩	I/O:	0.008 W	(40%)
🟦	Device Static:	0.081 W	(81%)

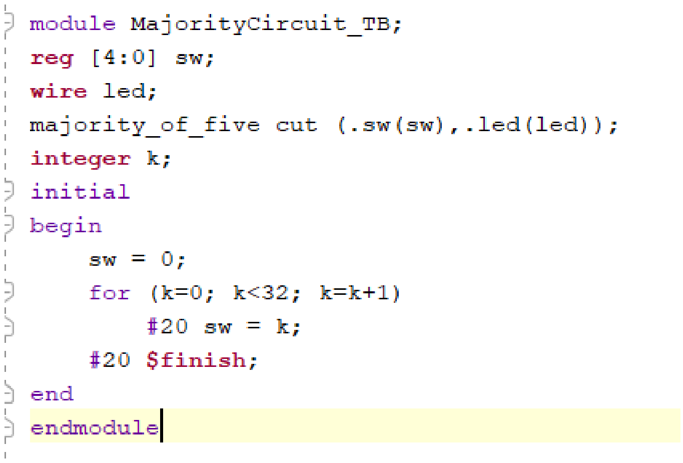
4. 5 Input Majority Circuit :-

Verilog Code:



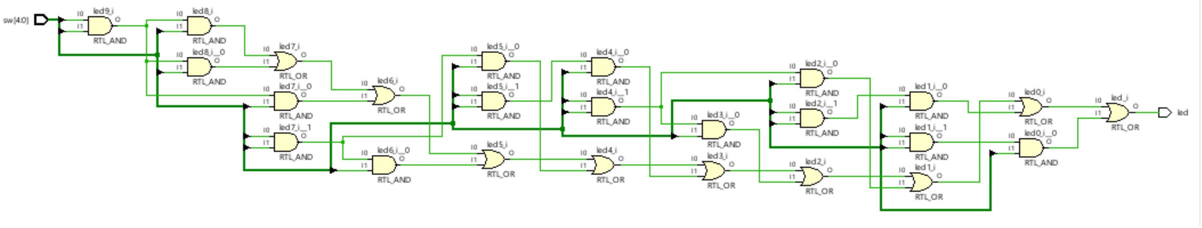
```
module MajorityCircuit(
    input [4:0]sw,
    output led
    );
assign led=(sw[0] & sw[1] & sw[2])|
        (sw[0] & sw[1] & sw[3])|
        (sw[0] & sw[1] & sw[4])|
        (sw[0] & sw[2] & sw[3])|
        (sw[0] & sw[2] & sw[4])|
        (sw[0] & sw[3] & sw[4])|
        (sw[1] & sw[2] & sw[3])|
        (sw[1] & sw[2] & sw[4])|
        (sw[1] & sw[3] & sw[4])|
        (sw[2] & sw[3] & sw[4]);
endmodule
```

Test Bench:

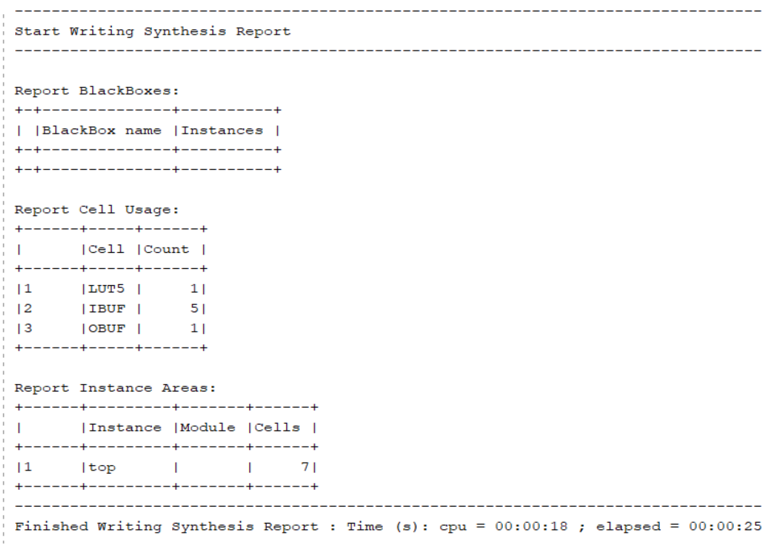


```
module MajorityCircuit_TB;
reg [4:0] sw;
wire led;
majority_of_five cut (.sw(sw),.led(led));
integer k;
initial
begin
    sw = 0;
    for (k=0; k<32; k=k+1)
        #20 sw = k;
    #20 $finish;
end
endmodule
```

RTL Schematic:

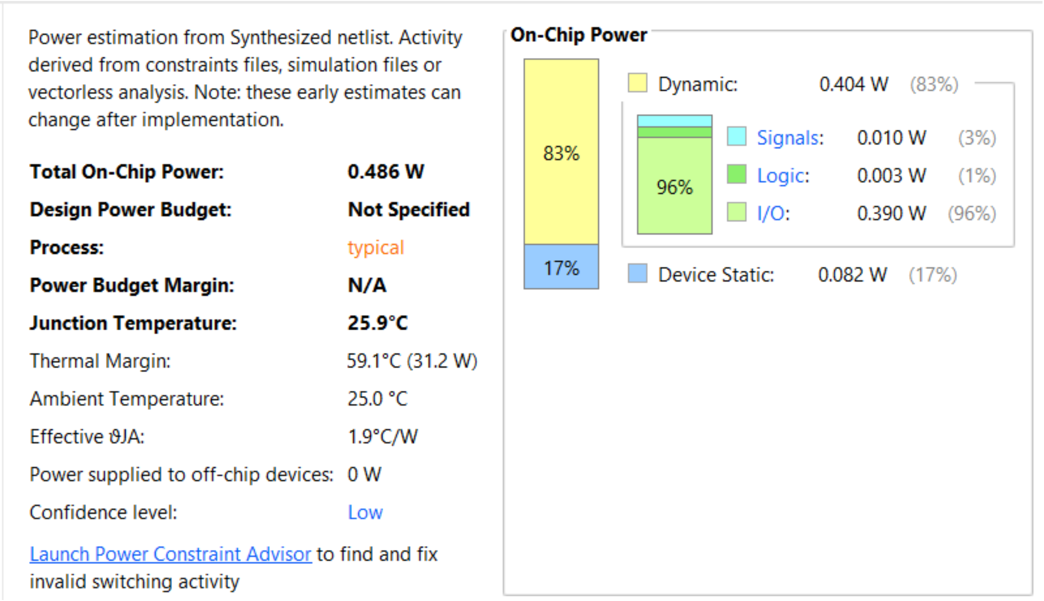


Synthesis Report:



```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT5 |     1|
|2     |IBUF |     5|
|3     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     7|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:18 ; elapsed = 00:00:25
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.486 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.9°C**
Thermal Margin:	59.1°C (31.2 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

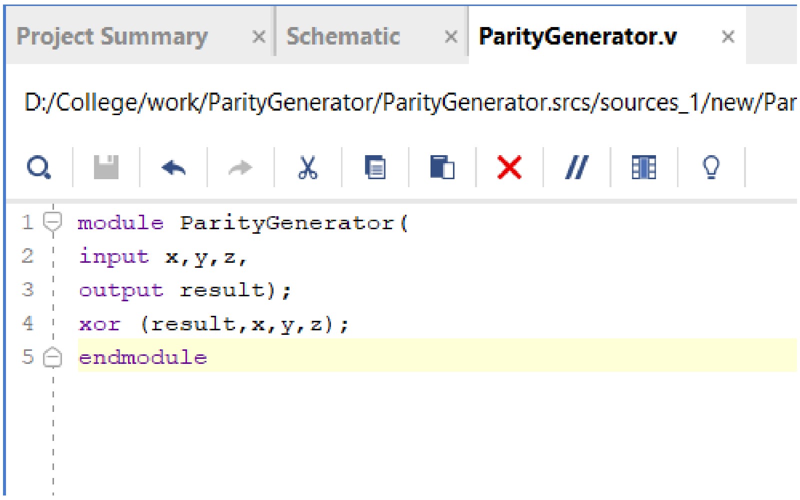
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨 Dynamic:	0.404 W	(83%)
🟦 Signals:	0.010 W	(3%)
🟩 Logic:	0.003 W	(1%)
🟩 I/O:	0.390 W	(96%)
🟦 Device Static:	0.082 W	(17%)

5. Parity Generator :-

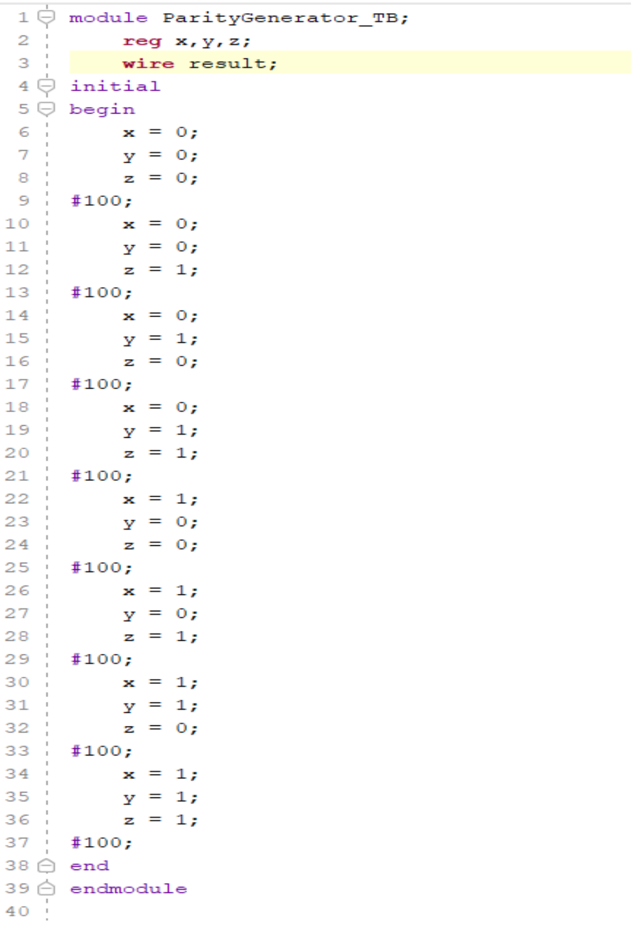
Verilog Code:



D:/College/work/ParityGenerator/ParityGenerator.srcs/sources_1/new/Par

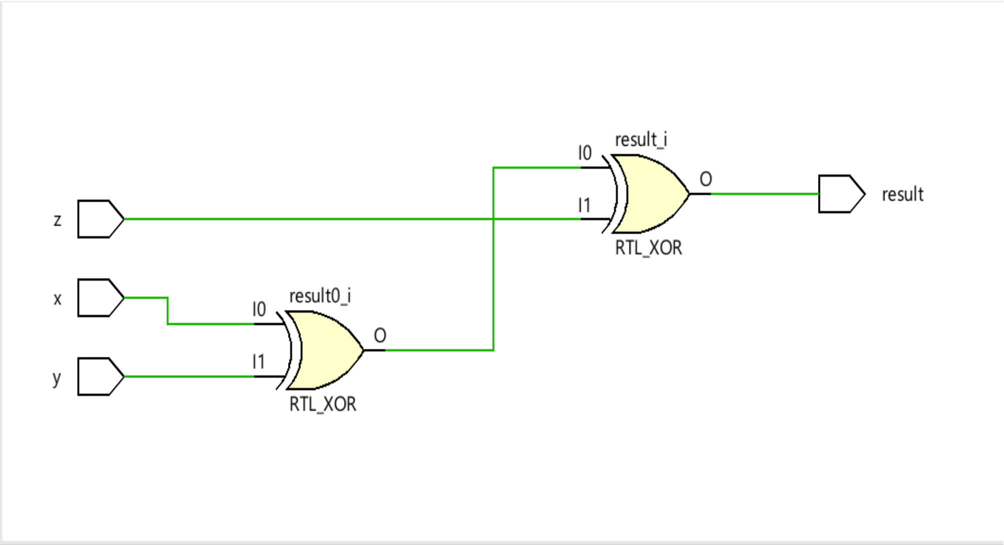
```
module ParityGenerator(
input x,y,z,
output result);
xor (result,x,y,z);
endmodule
```

Test Bench:



```
module ParityGenerator_TB;
    reg x,y,z;
    wire result;
initial
begin
    x = 0;
    y = 0;
    z = 0;
#100;
    x = 0;
    y = 0;
    z = 1;
#100;
    x = 0;
    y = 1;
    z = 0;
#100;
    x = 0;
    y = 1;
    z = 1;
#100;
    x = 1;
    y = 0;
    z = 0;
#100;
    x = 1;
    y = 0;
    z = 1;
#100;
    x = 1;
    y = 1;
    z = 0;
#100;
    x = 1;
    y = 1;
    z = 1;
#100;
end
endmodule
```

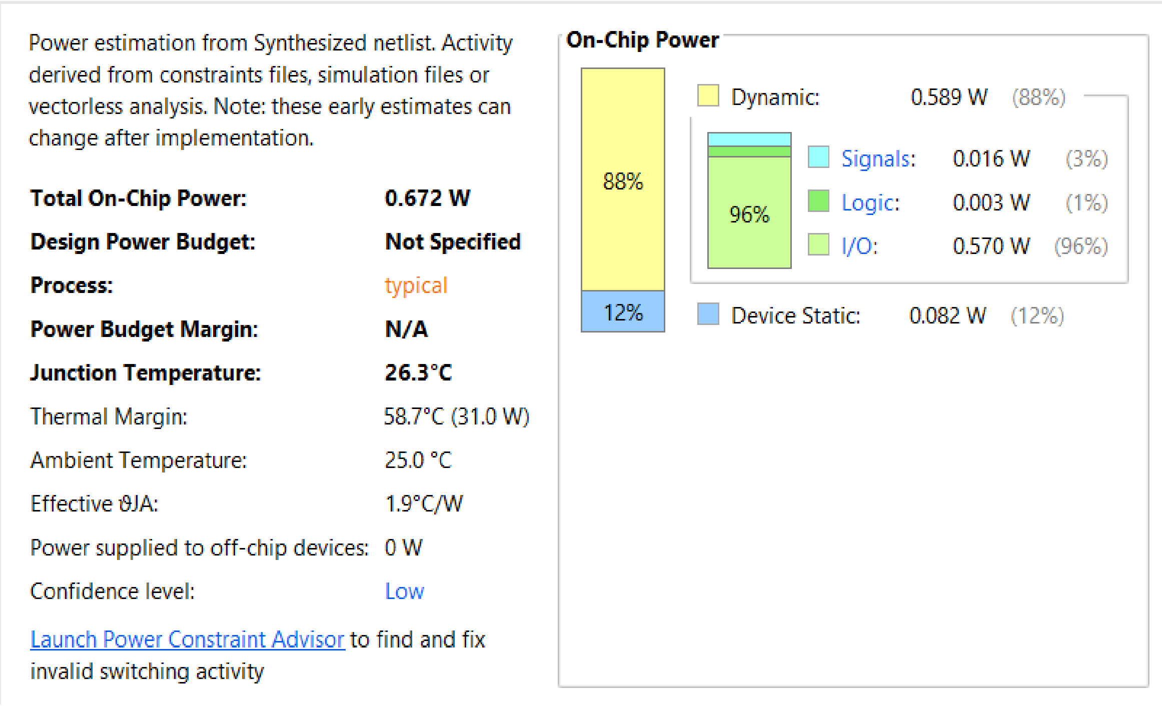
RTL Schematic:



Synthesis Report:

```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     1|
|2     |IBUF |     3|
|3     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     5|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:17 ; elapsed = 00:00:27
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.672 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**26.3°C**
Thermal Margin:	58.7°C (31.0 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

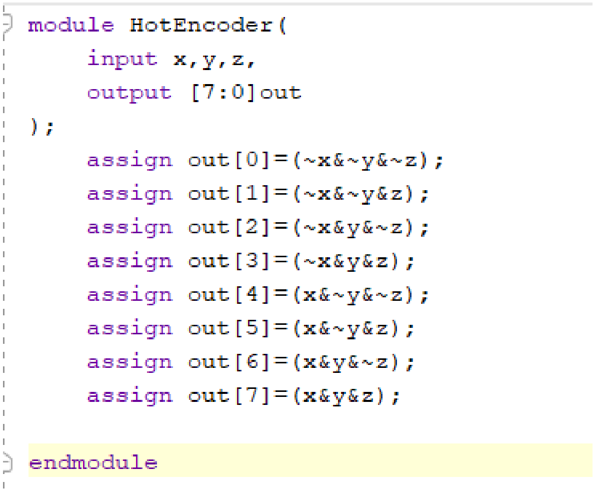
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨 Dynamic:	0.589 W	(88%)
🟦 Signals:	0.016 W	(3%)
🟩 Logic:	0.003 W	(1%)
🟩 I/O:	0.570 W	(96%)
🟦 Device Static:	0.082 W	(12%)

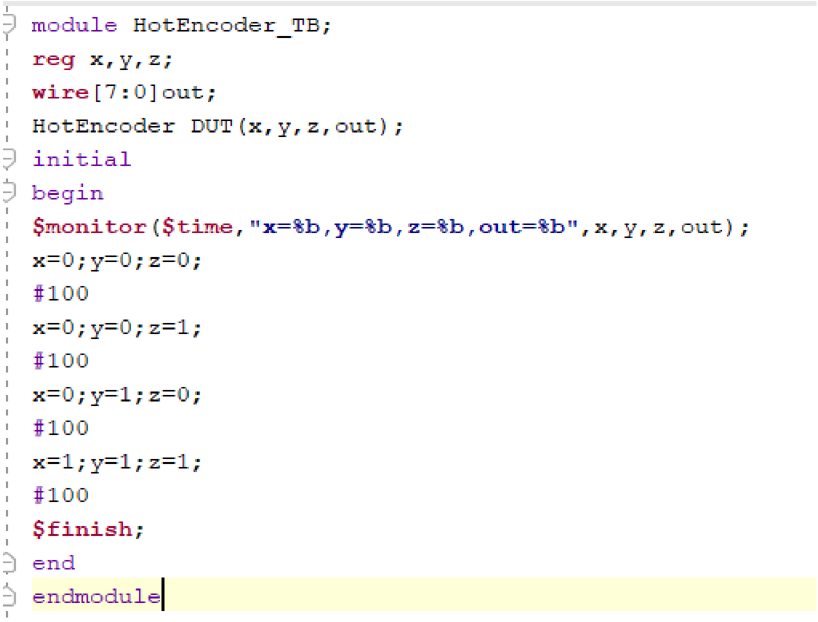
6. Binary To One Hot Encoder :-

Verilog Code:



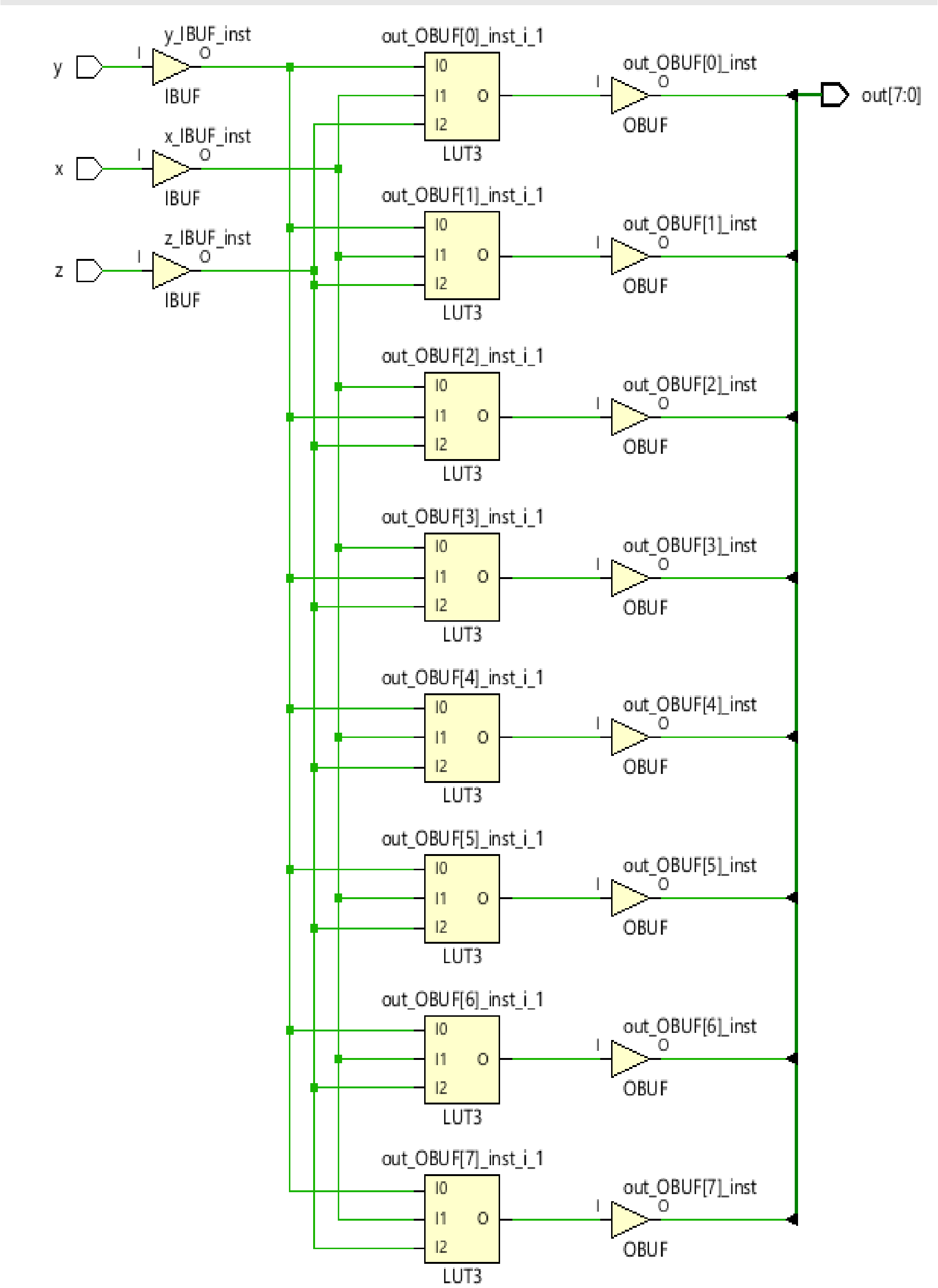
```
module HotEncoder(
     input x,y,z,
     output [7:0]out
);
     assign out[0]=(~x&~y&~z);
     assign out[1]=(~x&~y&z);
     assign out[2]=(~x&y&~z);
     assign out[3]=(~x&y&z);
     assign out[4]=(x&~y&~z);
     assign out[5]=(x&~y&z);
     assign out[6]=(x&y&~z);
     assign out[7]=(x&y&z);

endmodule
```

Test Bench:



```
module HotEncoder_TB;
reg x,y,z;
wire[7:0]out;
HotEncoder DUT(x,y,z,out);
initial
begin
$monitor($time,"x=%b,y=%b,z=%b,out=%b",x,y,z,out);
x=0;y=0;z=0;
#100
x=0;y=0;z=1;
#100
x=0;y=1;z=0;
#100
x=1;y=1;z=1;
#100
$finish;
end
endmodule
```

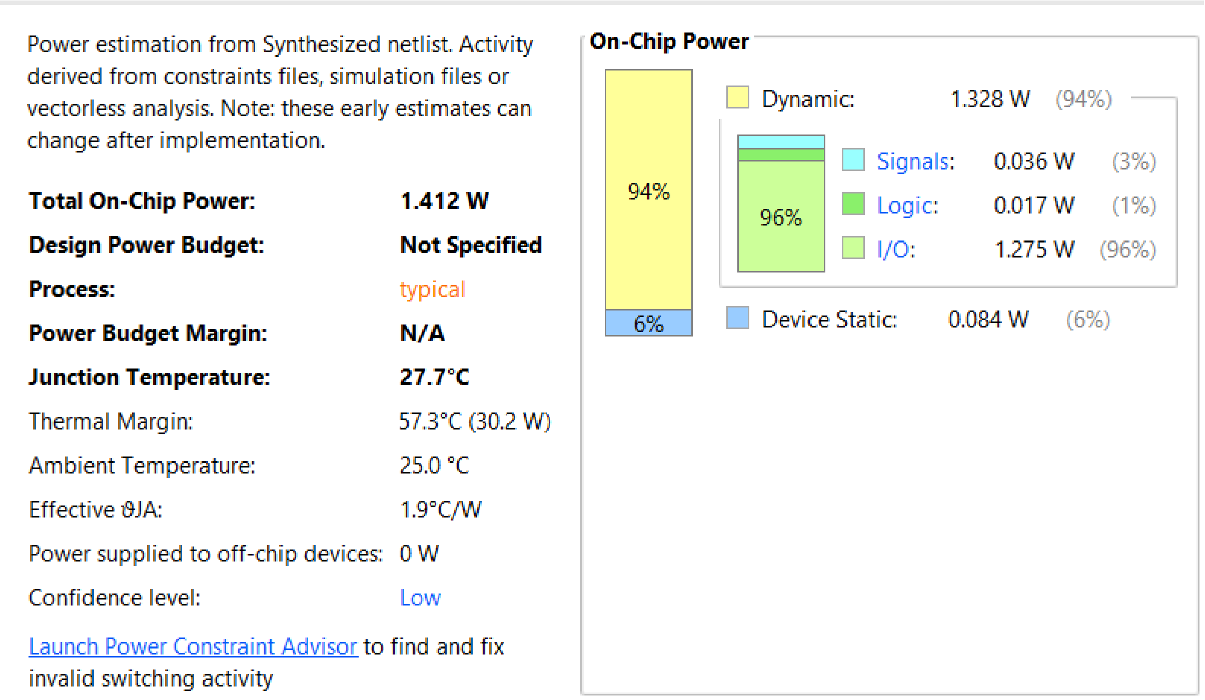
RTL Schematic:



Synthesis Report:

```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     8|
|2     |IBUF |     3|
|3     |OBUF |     8|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    19|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:16 ; elapsed = 00:00:26
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.412 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**27.7°C**
Thermal Margin:	57.3°C (30.2 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

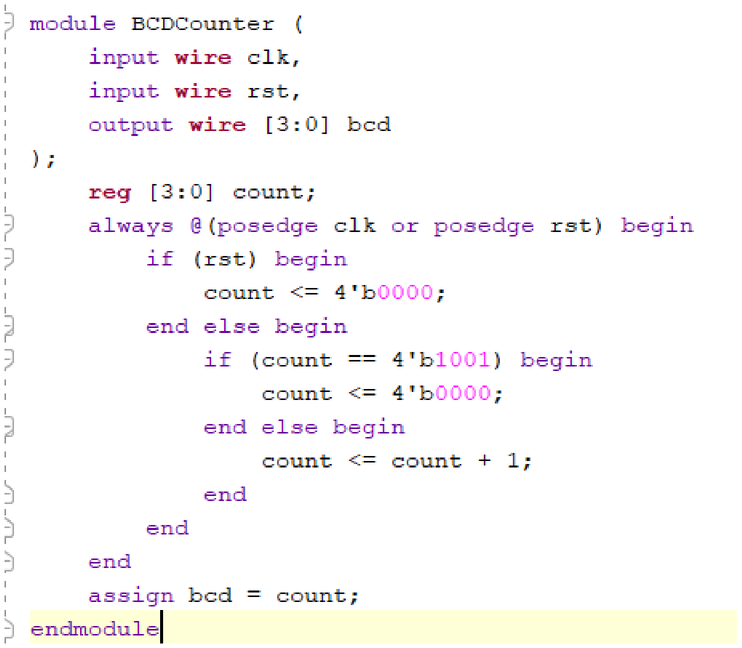
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨	Dynamic:	1.328 W	(94%)
🟦	Signals:	0.036 W	(3%)
🟩	Logic:	0.017 W	(1%)
🟩	I/O:	1.275 W	(96%)
🟦	Device Static:	0.084 W	(6%)

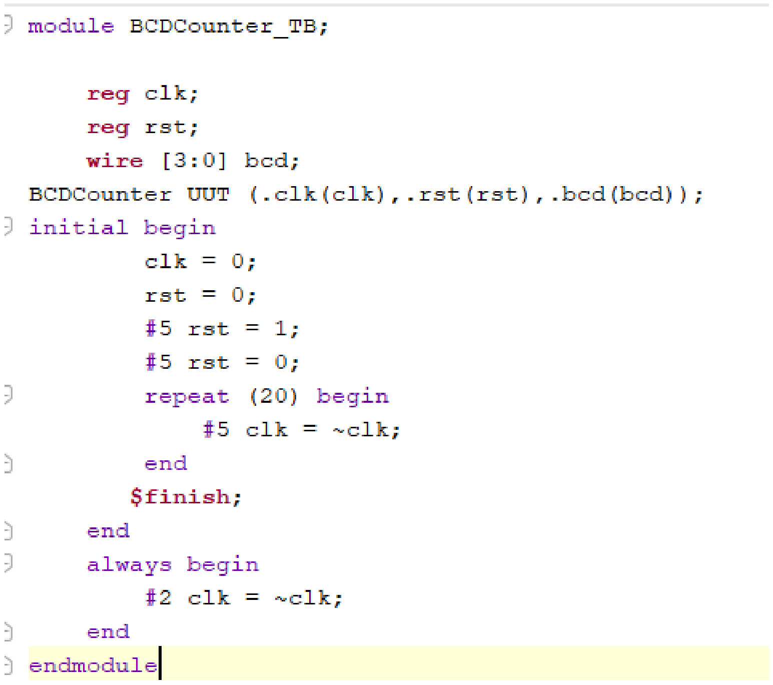
7. 4 Bit BCD Synchronous Counter :-

Verilog Code:



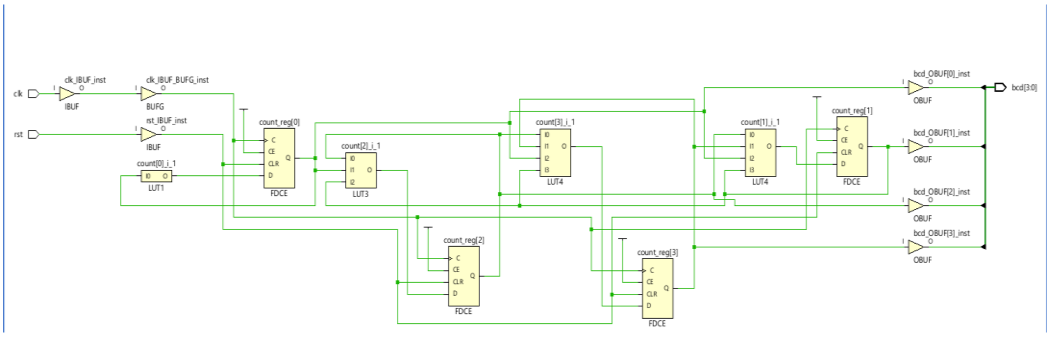
```
module BCDCounter (
    input wire clk,
    input wire rst,
    output wire [3:0] bcd
);
    reg [3:0] count;
    always @(posedge clk or posedge rst) begin
        if (rst) begin
            count <= 4'b0000;
        end else begin
            if (count == 4'b1001) begin
                count <= 4'b0000;
            end else begin
                count <= count + 1;
            end
        end
    end
    assign bcd = count;
endmodule
```

Test Bench:



```
module BCDCounter_TB;

    reg clk;
    reg rst;
    wire [3:0] bcd;
BCDCounter UUT (.clk(clk),.rst(rst),.bcd(bcd));
initial begin
        clk = 0;
        rst = 0;
        #5 rst = 1;
        #5 rst = 0;
        repeat (20) begin
            #5 clk = ~clk;
        end
       $finish;
    end
    always begin
        #2 clk = ~clk;
    end
endmodule
```

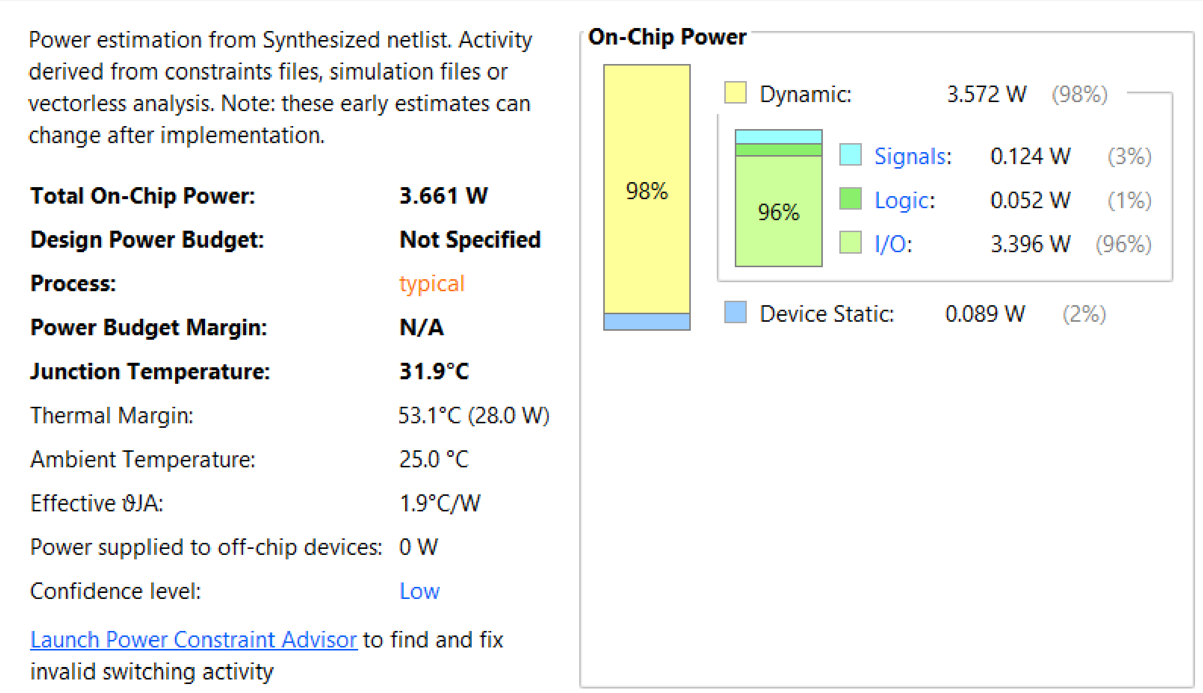
RTL Schematic:



Synthesis Report:

```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT1 |     1|
|3     |LUT3 |     1|
|4     |LUT4 |     2|
|5     |FDCE |     4|
|6     |IBUF |     2|
|7     |OBUF |     4|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    15|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:14 ; elapsed = 00:00:26
---------------------------------------------------------------------------------
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**3.661 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**31.9°C**
Thermal Margin:	53.1°C (28.0 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

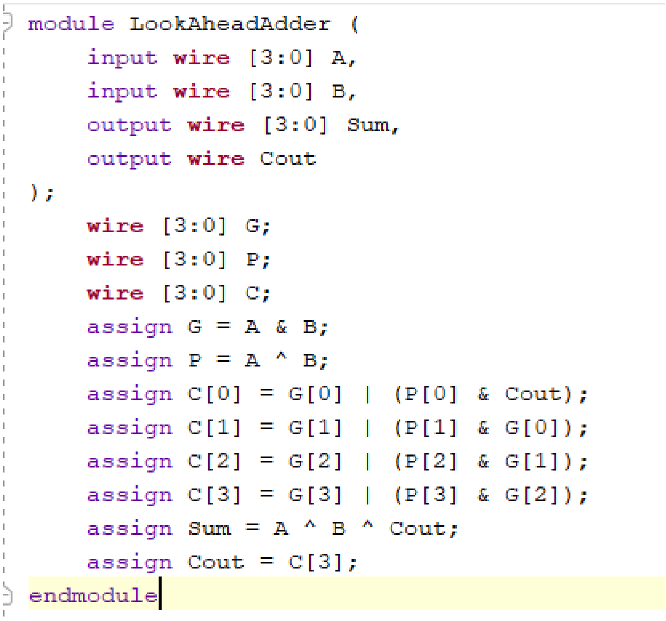
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨 Dynamic:	3.572 W	(98%)
🟦 Signals:	0.124 W	(3%)
🟩 Logic:	0.052 W	(1%)
🟩 I/O:	3.396 W	(96%)
🟦 Device Static:	0.089 W	(2%)

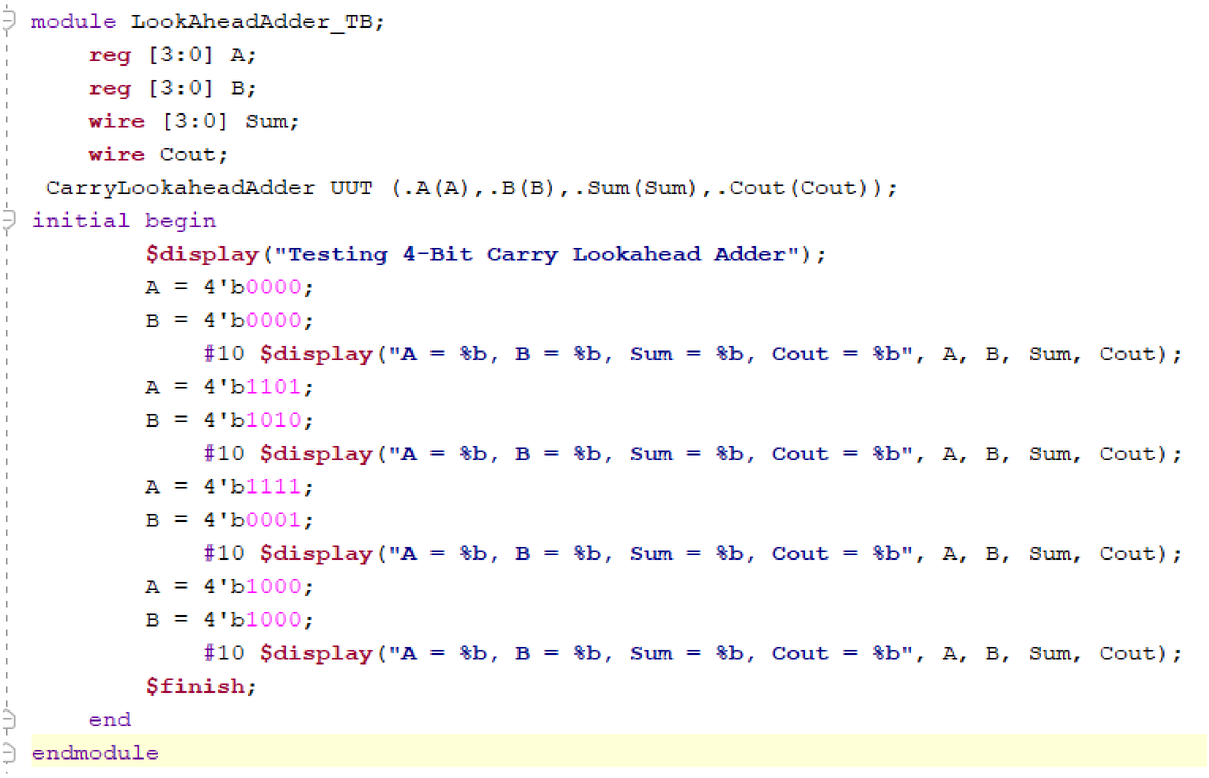
8. 4-Bit Carry Look Ahead Adder :-

Verilog Code:



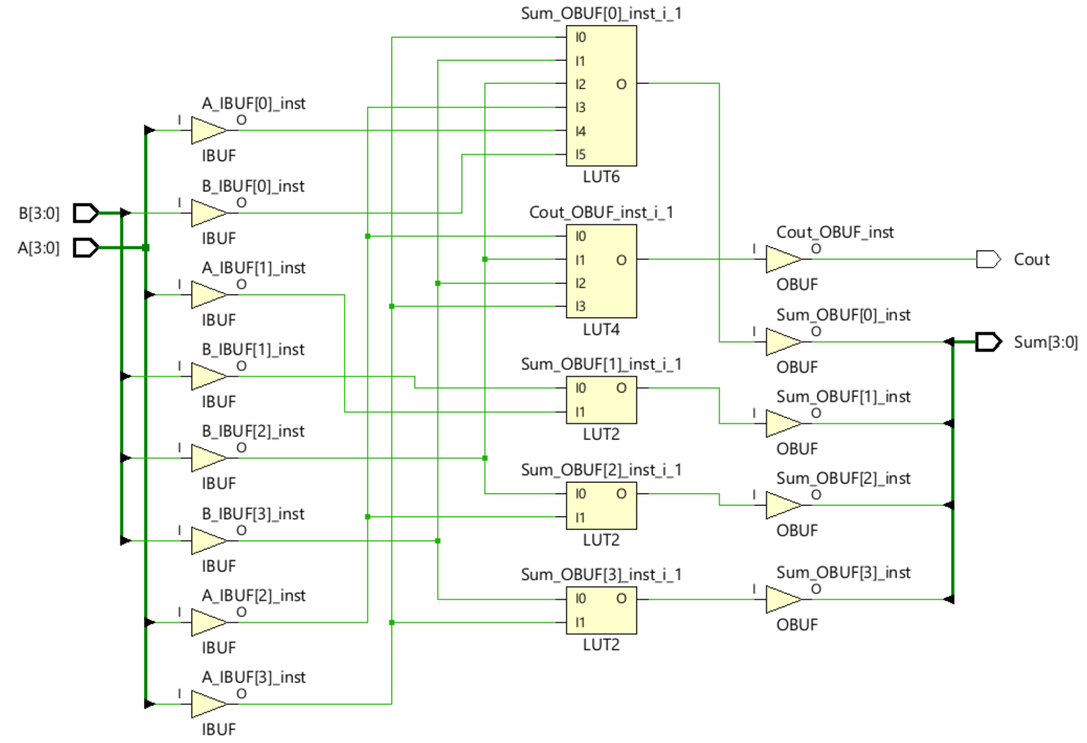
```verilog
module LookAheadAdder (
    input wire [3:0] A,
    input wire [3:0] B,
    output wire [3:0] Sum,
    output wire Cout
);
    wire [3:0] G;
    wire [3:0] P;
    wire [3:0] C;
    assign G = A & B;
    assign P = A ^ B;
    assign C[0] = G[0] | (P[0] & Cout);
    assign C[1] = G[1] | (P[1] & G[0]);
    assign C[2] = G[2] | (P[2] & G[1]);
    assign C[3] = G[3] | (P[3] & G[2]);
    assign Sum = A ^ B ^ Cout;
    assign Cout = C[3];
endmodule
```

Test Bench:

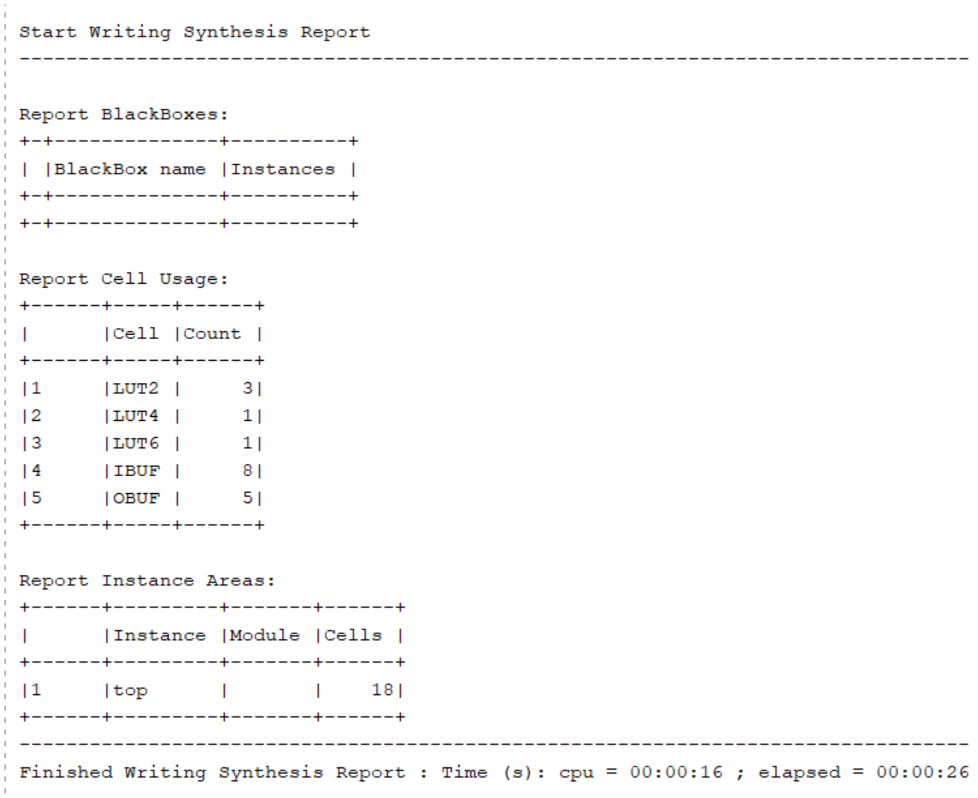


```verilog
module LookAheadAdder_TB;
    reg [3:0] A;
    reg [3:0] B;
    wire [3:0] Sum;
    wire Cout;
 CarryLookaheadAdder UUT (.A(A),.B(B),.Sum(Sum),.Cout(Cout));
initial begin
        $display("Testing 4-Bit Carry Lookahead Adder");
        A = 4'b0000;
        B = 4'b0000;
            #10 $display("A = %b, B = %b, Sum = %b, Cout = %b", A, B, Sum, Cout);
        A = 4'b1101;
        B = 4'b1010;
            #10 $display("A = %b, B = %b, Sum = %b, Cout = %b", A, B, Sum, Cout);
        A = 4'b1111;
        B = 4'b0001;
            #10 $display("A = %b, B = %b, Sum = %b, Cout = %b", A, B, Sum, Cout);
        A = 4'b1000;
        B = 4'b1000;
            #10 $display("A = %b, B = %b, Sum = %b, Cout = %b", A, B, Sum, Cout);
        $finish;
    end
endmodule
```

RTL Schematic:

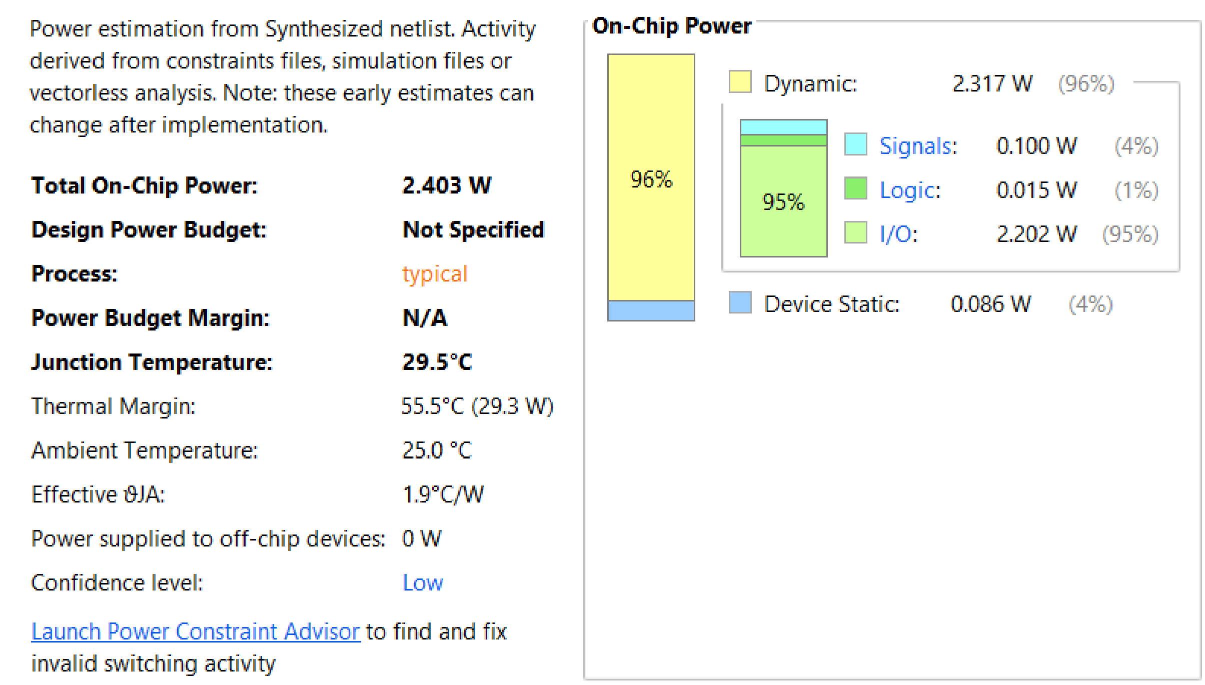


Synthesis Report:



```
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT2 |     3|
|2     |LUT4 |     1|
|3     |LUT6 |     1|
|4     |IBUF |     8|
|5     |OBUF |     5|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    18|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:16 ; elapsed = 00:00:26
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**2.403 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**29.5°C**
Thermal Margin:	55.5°C (29.3 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

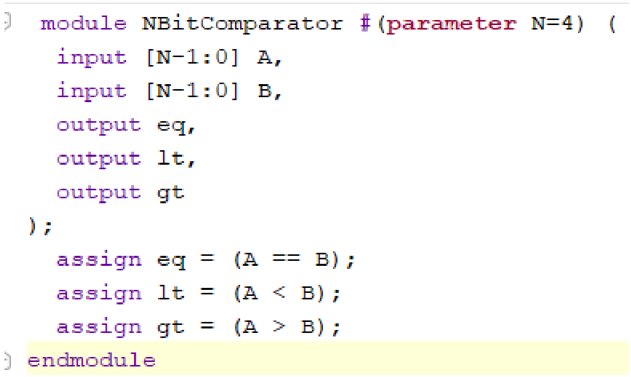
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨 Dynamic:	2.317 W	(96%)
🟦 Signals:	0.100 W	(4%)
🟩 Logic:	0.015 W	(1%)
🟩 I/O:	2.202 W	(95%)
🟦 Device Static:	0.086 W	(4%)

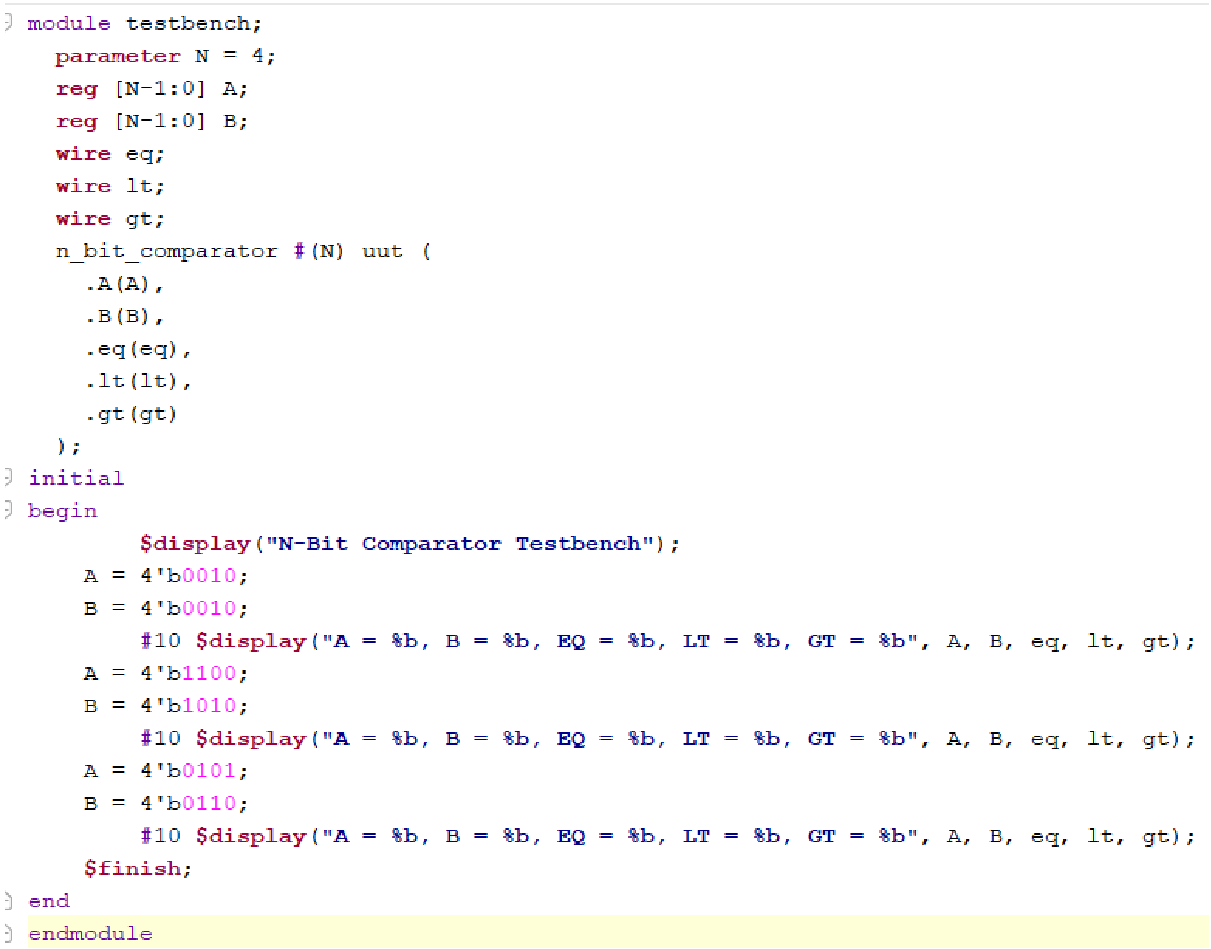
9. N-Bit Comparator :-

Verilog Code:



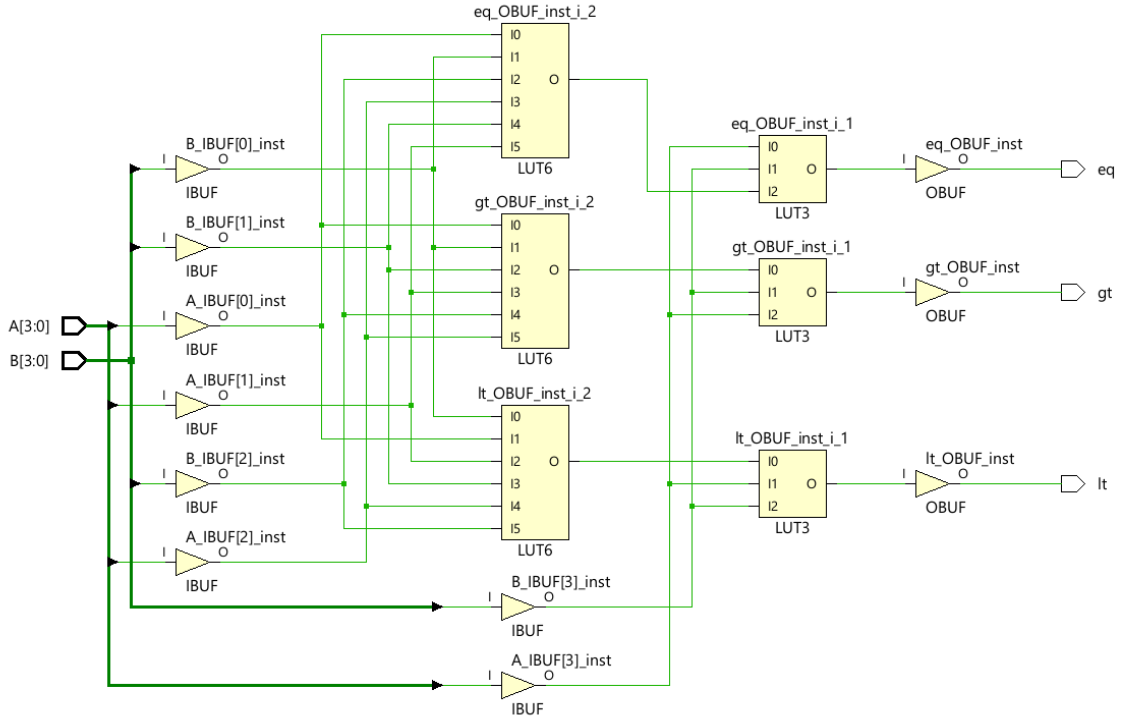
```
 module NBitComparator #(parameter N=4) (
  input [N-1:0] A,
  input [N-1:0] B,
  output eq,
  output lt,
  output gt
);
  assign eq = (A == B);
  assign lt = (A < B);
  assign gt = (A > B);
endmodule
```

Test Bench:



```
module testbench;
  parameter N = 4;
  reg [N-1:0] A;
  reg [N-1:0] B;
  wire eq;
  wire lt;
  wire gt;
  n_bit_comparator #(N) uut (
    .A(A),
    .B(B),
    .eq(eq),
    .lt(lt),
    .gt(gt)
  );
initial
begin
        $display("N-Bit Comparator Testbench");
    A = 4'b0010;
    B = 4'b0010;
        #10 $display("A = %b, B = %b, EQ = %b, LT = %b, GT = %b", A, B, eq, lt, gt);
    A = 4'b1100;
    B = 4'b1010;
        #10 $display("A = %b, B = %b, EQ = %b, LT = %b, GT = %b", A, B, eq, lt, gt);
    A = 4'b0101;
    B = 4'b0110;
        #10 $display("A = %b, B = %b, EQ = %b, LT = %b, GT = %b", A, B, eq, lt, gt);
    $finish;
end
endmodule
```

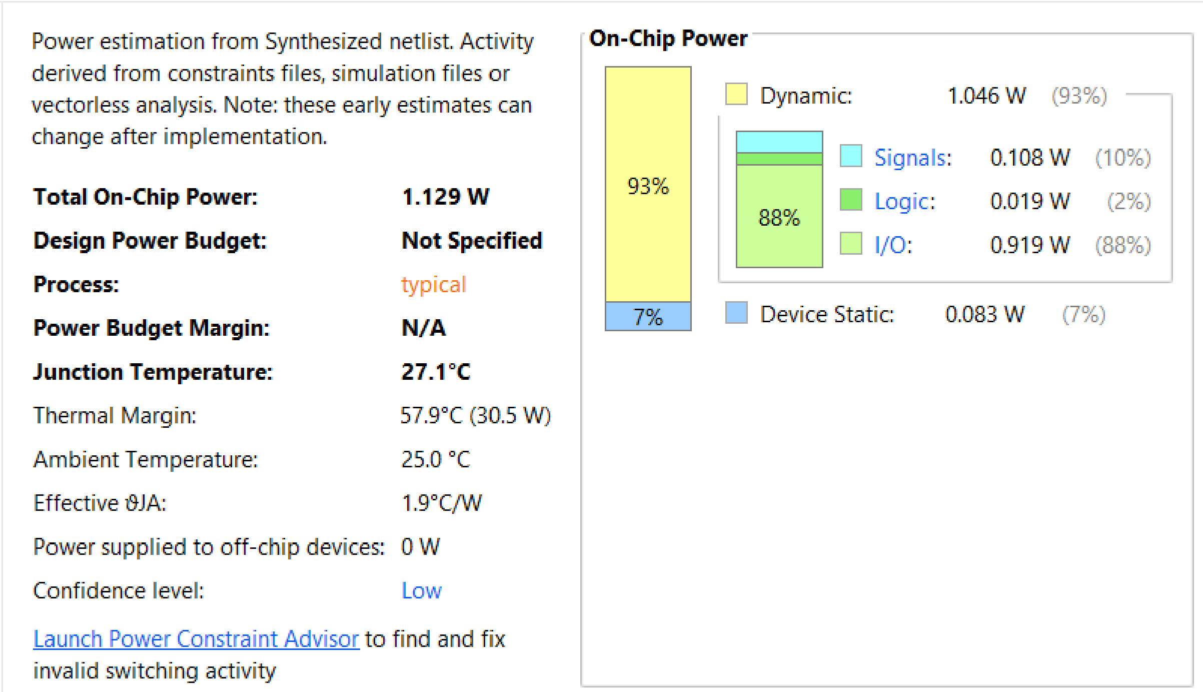
RTL Schematic:



Synthesis Report:

```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT3 |     3|
|2     |LUT6 |     3|
|3     |IBUF |     8|
|4     |OBUF |     3|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    17|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:16 ; elapsed = 00:00:26
---------------------------------------------------------------------------------
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.129 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**27.1°C**
Thermal Margin:	57.9°C (30.5 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

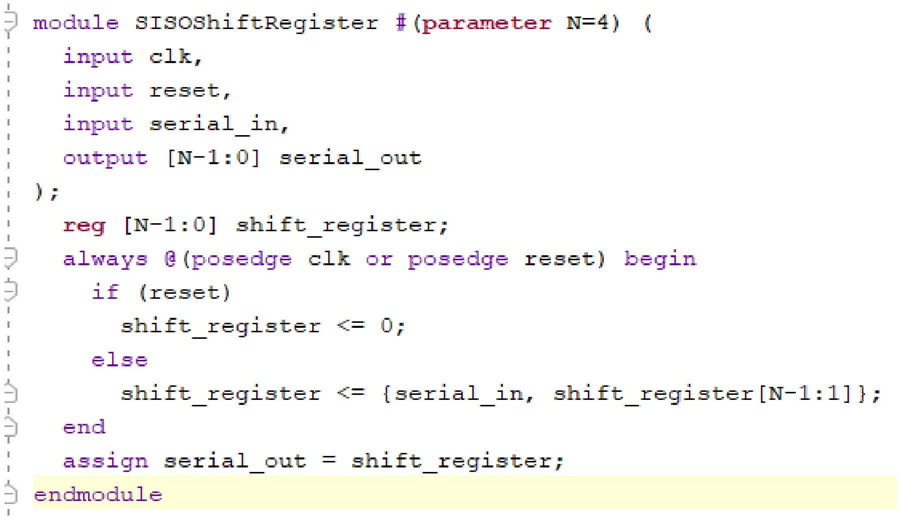
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	1.046 W	(93%)
Signals:	0.108 W	(10%)
Logic:	0.019 W	(2%)
I/O:	0.919 W	(88%)
Device Static:	0.083 W	(7%)

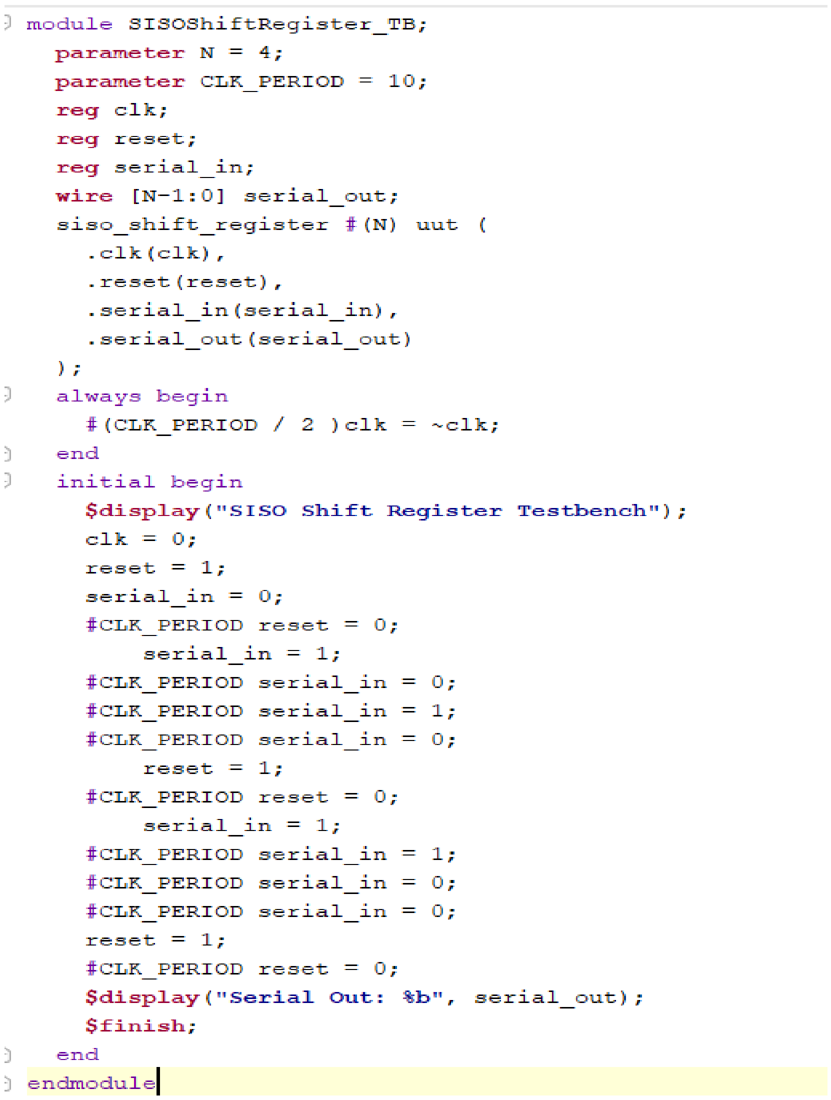
10. Serial In Serial Out Shift Register :-

Verilog Code:



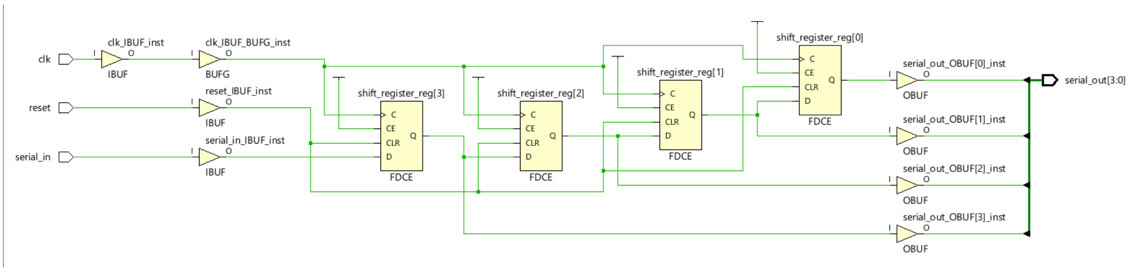
```
module SISOShiftRegister #(parameter N=4) (
  input clk,
  input reset,
  input serial_in,
  output [N-1:0] serial_out
);
  reg [N-1:0] shift_register;
  always @(posedge clk or posedge reset) begin
    if (reset)
      shift_register <= 0;
    else
      shift_register <= {serial_in, shift_register[N-1:1]};
  end
  assign serial_out = shift_register;
endmodule
```

Test Bench:



```
module SISOShiftRegister_TB;
  parameter N = 4;
  parameter CLK_PERIOD = 10;
  reg clk;
  reg reset;
  reg serial_in;
  wire [N-1:0] serial_out;
  siso_shift_register #(N) uut (
    .clk(clk),
    .reset(reset),
    .serial_in(serial_in),
    .serial_out(serial_out)
  );
  always begin
    #(CLK_PERIOD / 2 )clk = ~clk;
  end
  initial begin
    $display("SISO Shift Register Testbench");
    clk = 0;
    reset = 1;
    serial_in = 0;
    #CLK_PERIOD reset = 0;
        serial_in = 1;
    #CLK_PERIOD serial_in = 0;
    #CLK_PERIOD serial_in = 1;
    #CLK_PERIOD serial_in = 0;
        reset = 1;
    #CLK_PERIOD reset = 0;
        serial_in = 1;
    #CLK_PERIOD serial_in = 1;
    #CLK_PERIOD serial_in = 0;
    #CLK_PERIOD serial_in = 0;
    reset = 1;
    #CLK_PERIOD reset = 0;
    $display("Serial Out: %b", serial_out);
    $finish;
  end
endmodule
```

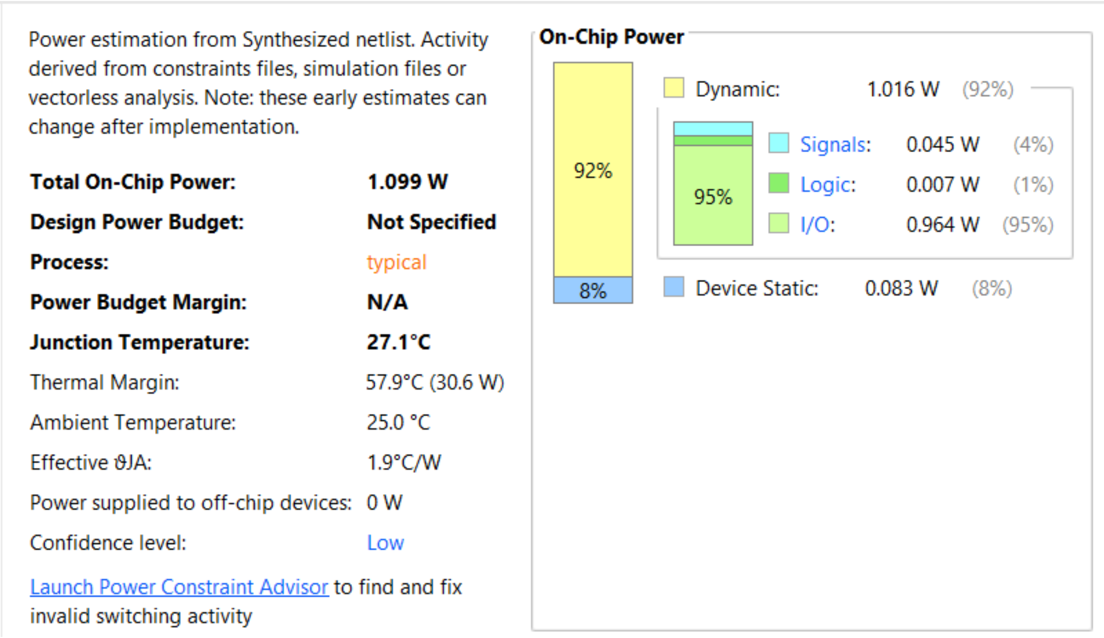
RTL Schematic:



Synthesis Report:

```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |FDCE |     4|
|3     |IBUF |     3|
|4     |OBUF |     4|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    12|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:16 ; elapsed = 00:00:26
---------------------------------------------------------------------------------
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.099 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**27.1°C**
Thermal Margin:	57.9°C (30.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

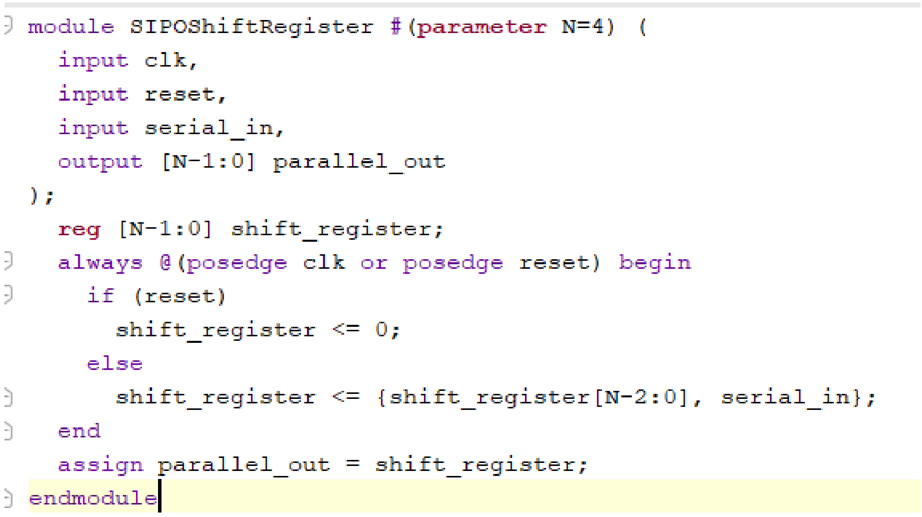
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨	Dynamic:	1.016 W	(92%)
🟦	Signals:	0.045 W	(4%)
🟩	Logic:	0.007 W	(1%)
🟩	I/O:	0.964 W	(95%)
🟦	Device Static:	0.083 W	(8%)

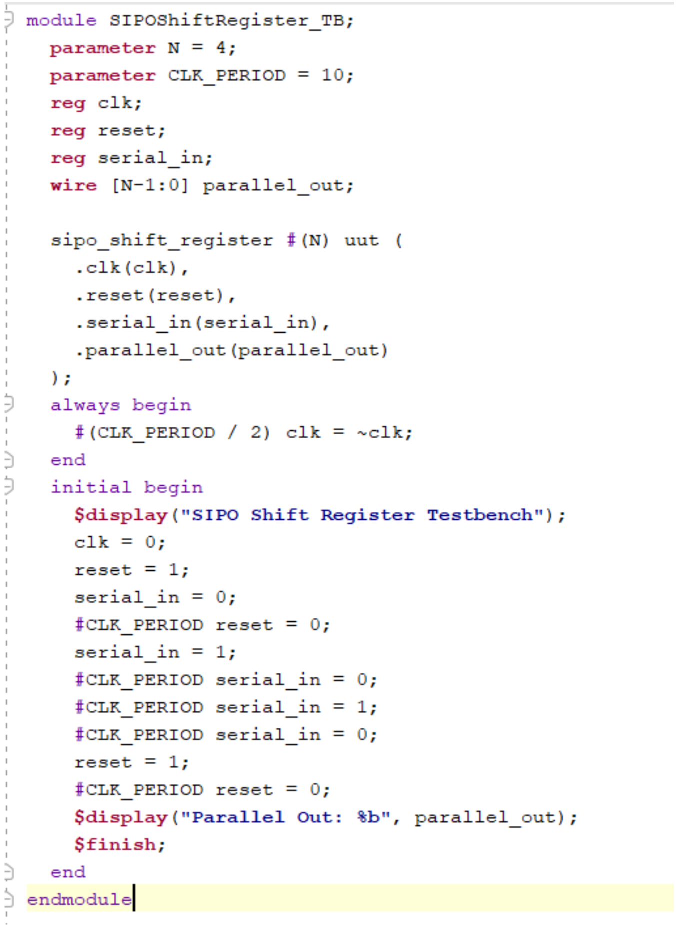
11. Serial In Parallel Out Shift Register :-

Verilog Code:



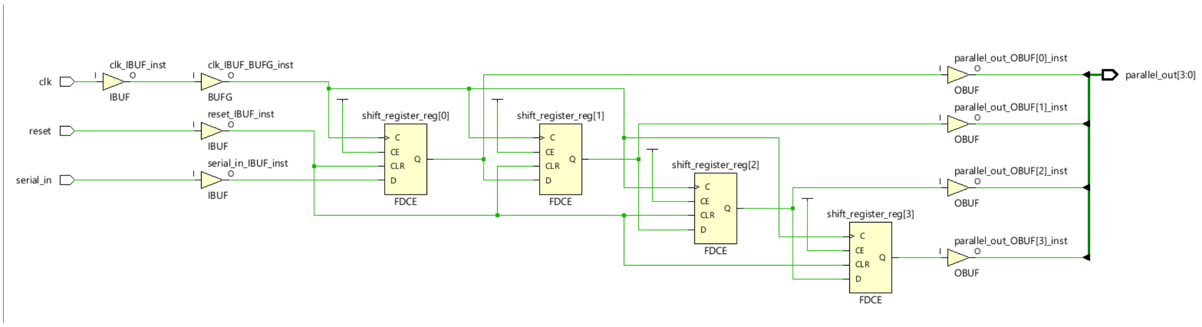
```
module SIPOShiftRegister #(parameter N=4) (
    input clk,
    input reset,
    input serial_in,
    output [N-1:0] parallel_out
);
    reg [N-1:0] shift_register;
    always @(posedge clk or posedge reset) begin
      if (reset)
        shift_register <= 0;
      else
        shift_register <= {shift_register[N-2:0], serial_in};
    end
    assign parallel_out = shift_register;
endmodule
```

Test Bench:



```
module SIPOShiftRegister_TB;
  parameter N = 4;
  parameter CLK_PERIOD = 10;
  reg clk;
  reg reset;
  reg serial_in;
  wire [N-1:0] parallel_out;

  sipo_shift_register #(N) uut (
    .clk(clk),
    .reset(reset),
    .serial_in(serial_in),
    .parallel_out(parallel_out)
  );
  always begin
    #(CLK_PERIOD / 2) clk = ~clk;
  end
  initial begin
    $display("SIPO Shift Register Testbench");
    clk = 0;
    reset = 1;
    serial_in = 0;
    #CLK_PERIOD reset = 0;
    serial_in = 1;
    #CLK_PERIOD serial_in = 0;
    #CLK_PERIOD serial_in = 1;
    #CLK_PERIOD serial_in = 0;
    reset = 1;
    #CLK_PERIOD reset = 0;
    $display("Parallel Out: %b", parallel_out);
    $finish;
  end
endmodule
```

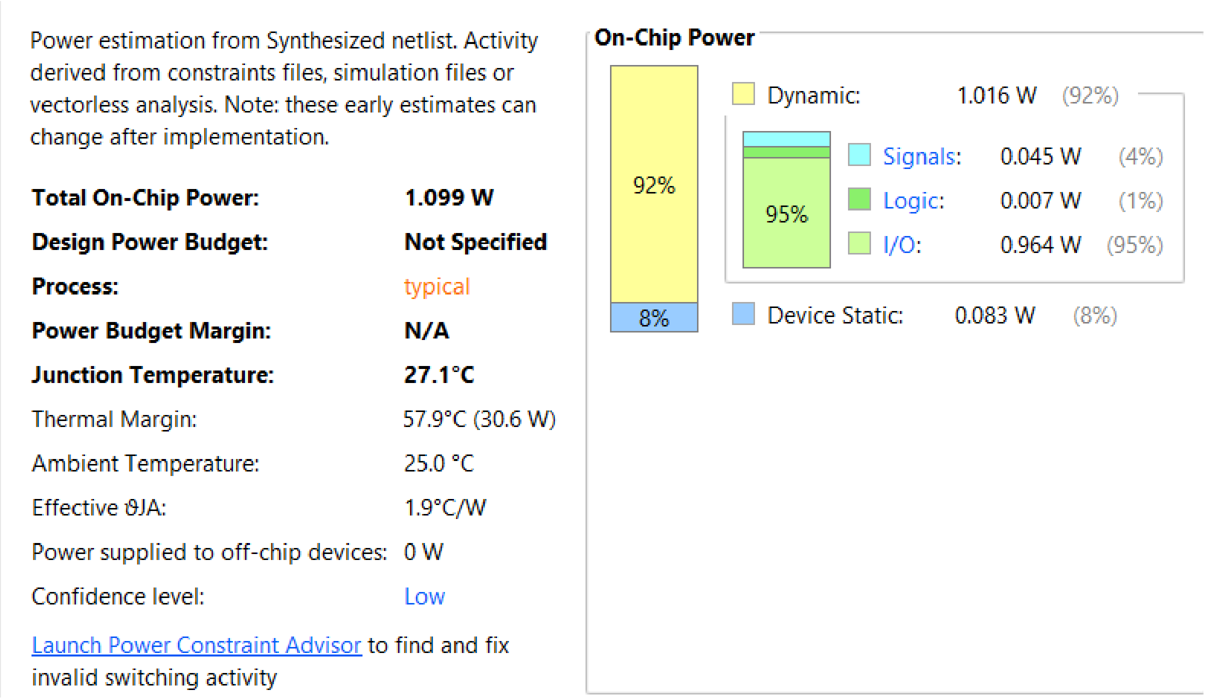
RTL Schematic:



Synthesis Report:

```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |FDCE |     4|
|3     |IBUF |     3|
|4     |OBUF |     4|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    12|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:15 ; elapsed = 00:00:24
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.099 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**27.1°C**
Thermal Margin:	57.9°C (30.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

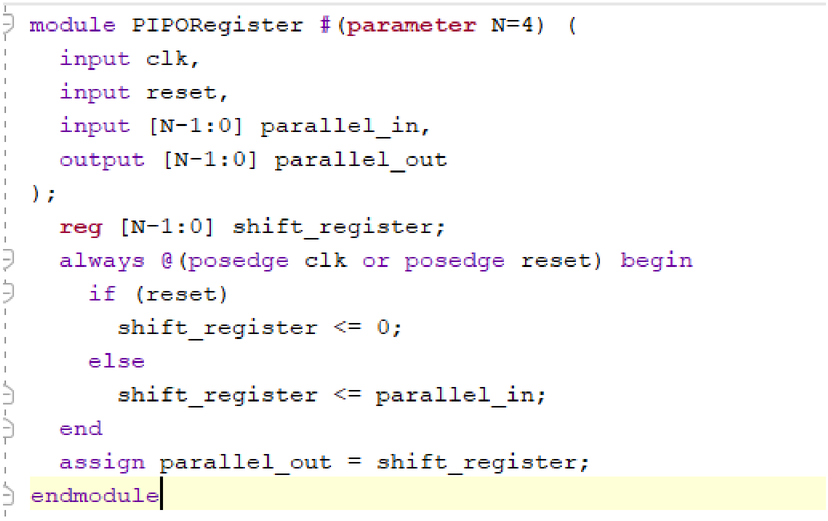
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨	Dynamic:	1.016 W	(92%)
🟦	Signals:	0.045 W	(4%)
🟩	Logic:	0.007 W	(1%)
🟩	I/O:	0.964 W	(95%)
🟦	Device Static:	0.083 W	(8%)

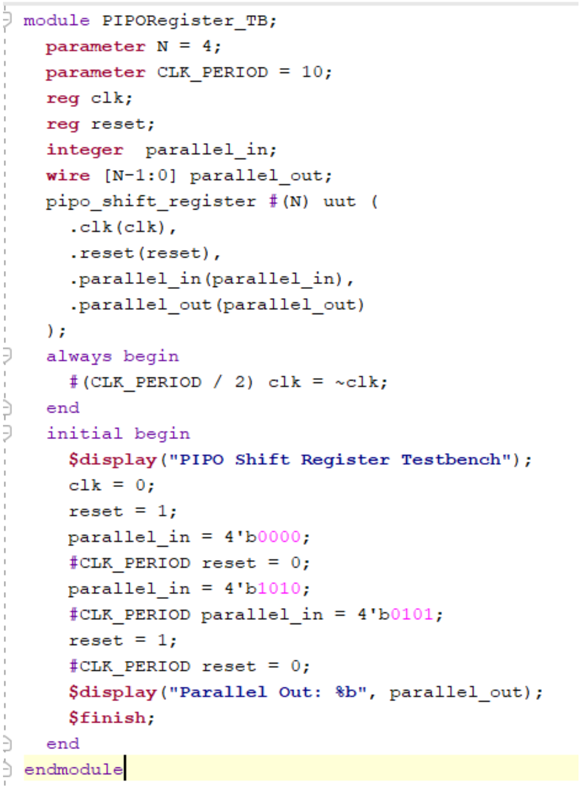
12. Parallel In Parallel Out Register :-

Verilog Code:



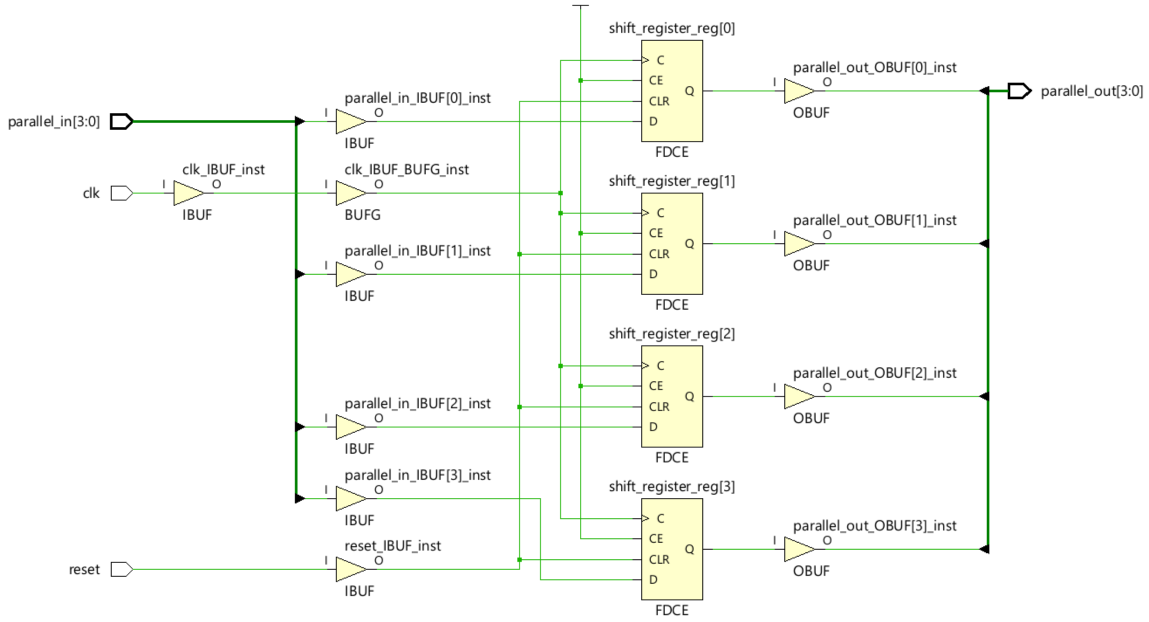
```
module PIPORegister #(parameter N=4) (
  input clk,
  input reset,
  input [N-1:0] parallel_in,
  output [N-1:0] parallel_out
);
  reg [N-1:0] shift_register;
  always @(posedge clk or posedge reset) begin
    if (reset)
      shift_register <= 0;
    else
      shift_register <= parallel_in;
  end
  assign parallel_out = shift_register;
endmodule
```

Test Bench:

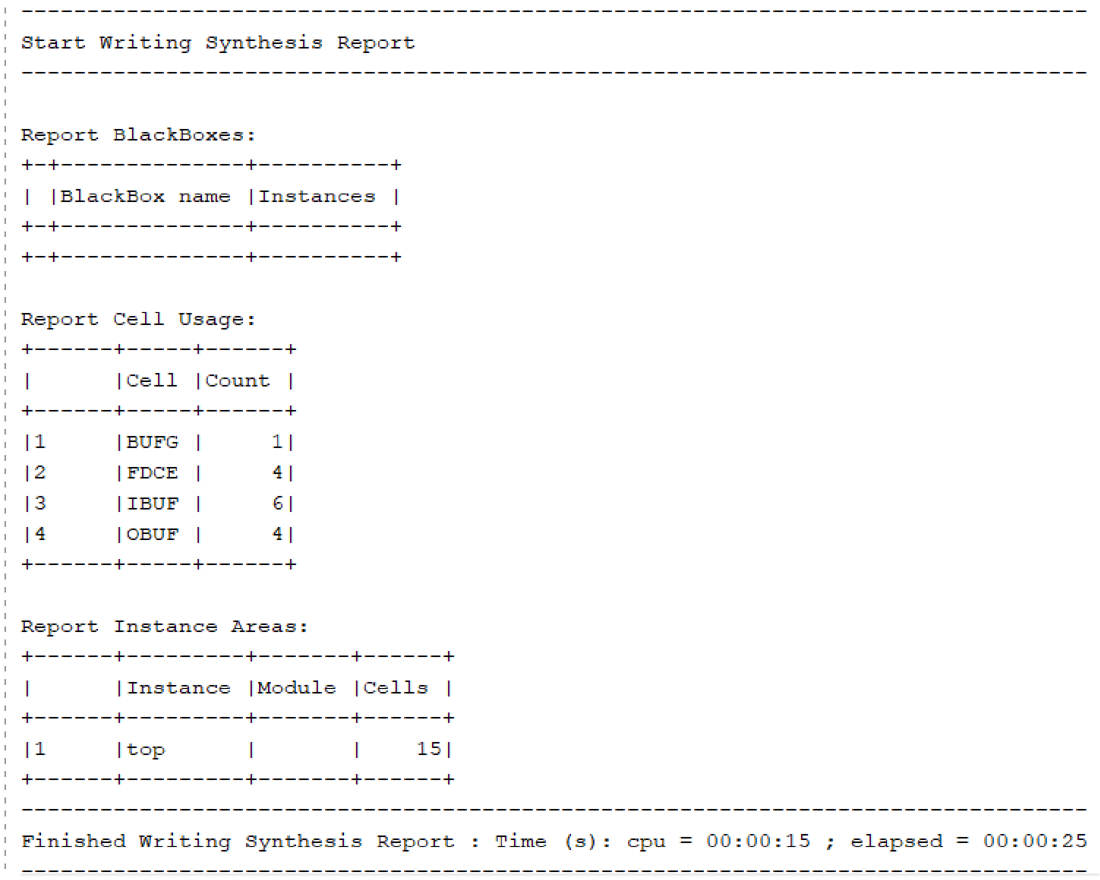


```
module PIPORegister_TB;
  parameter N = 4;
  parameter CLK_PERIOD = 10;
  reg clk;
  reg reset;
  integer  parallel_in;
  wire [N-1:0] parallel_out;
  pipo_shift_register #(N) uut (
    .clk(clk),
    .reset(reset),
    .parallel_in(parallel_in),
    .parallel_out(parallel_out)
  );
  always begin
    #(CLK_PERIOD / 2) clk = ~clk;
  end
  initial begin
    $display("PIPO Shift Register Testbench");
    clk = 0;
    reset = 1;
    parallel_in = 4'b0000;
    #CLK_PERIOD reset = 0;
    parallel_in = 4'b1010;
    #CLK_PERIOD parallel_in = 4'b0101;
    reset = 1;
    #CLK_PERIOD reset = 0;
    $display("Parallel Out: %b", parallel_out);
    $finish;
  end
endmodule
```

RTL Schematic:

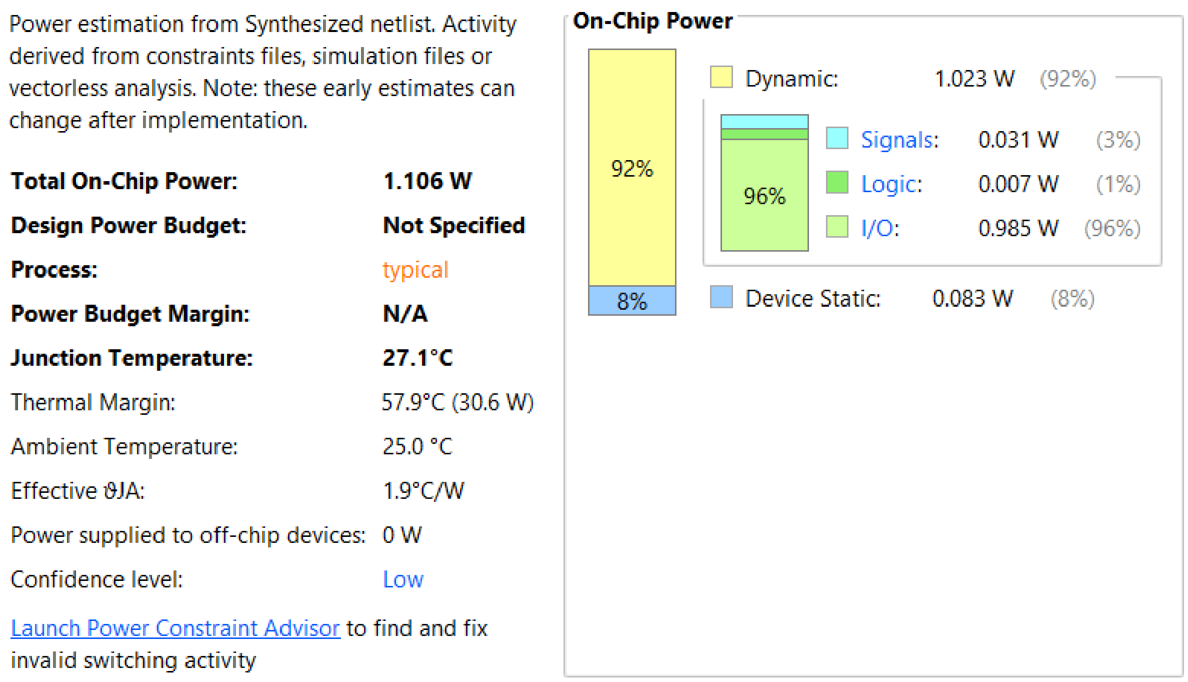


Synthesis Report:



```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |FDCE |     4|
|3     |IBUF |     6|
|4     |OBUF |     4|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    15|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:15 ; elapsed = 00:00:25
---------------------------------------------------------------------------------
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.106 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**27.1°C**
Thermal Margin:	57.9°C (30.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

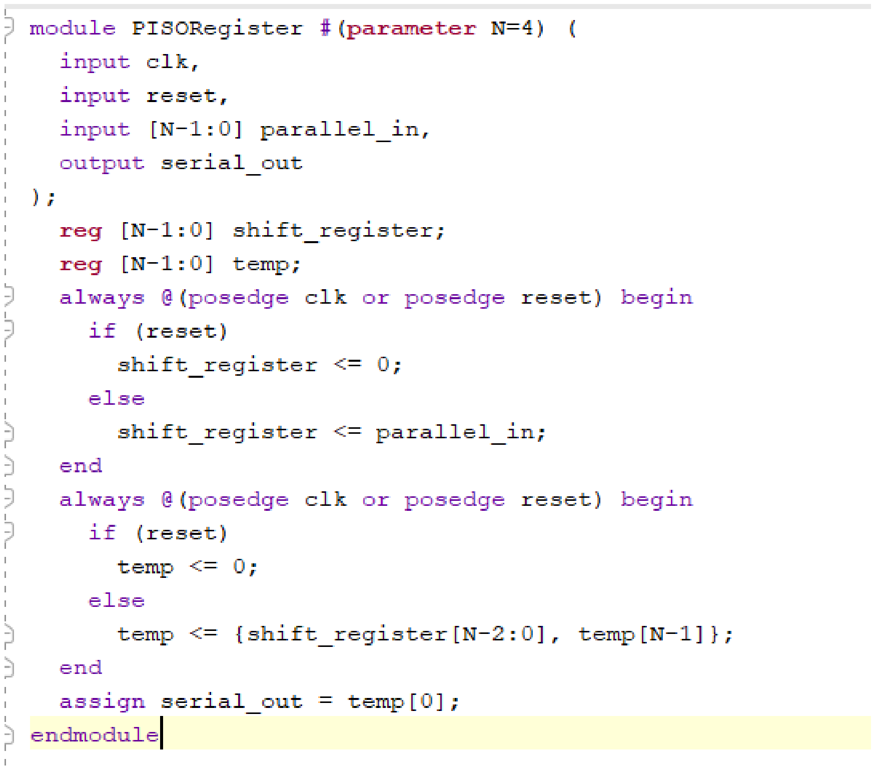
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨	Dynamic:	1.023 W	(92%)
🟦	Signals:	0.031 W	(3%)
🟩	Logic:	0.007 W	(1%)
🟩	I/O:	0.985 W	(96%)
🟦	Device Static:	0.083 W	(8%)

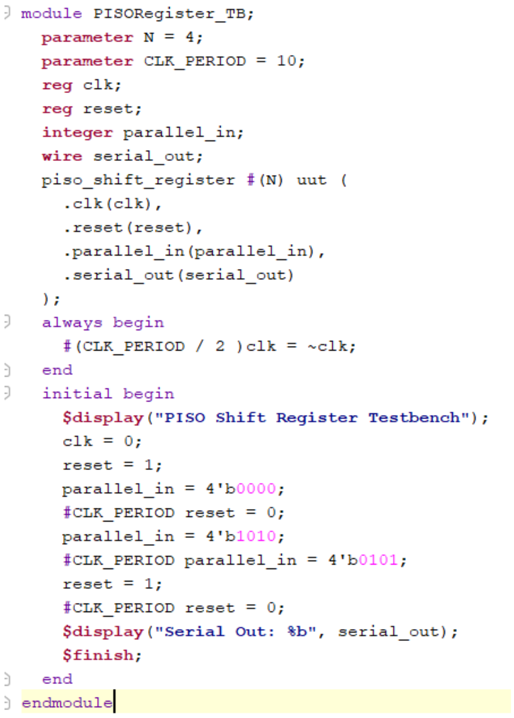
13. Parallel In Serial Out Register :-

Verilog Code:



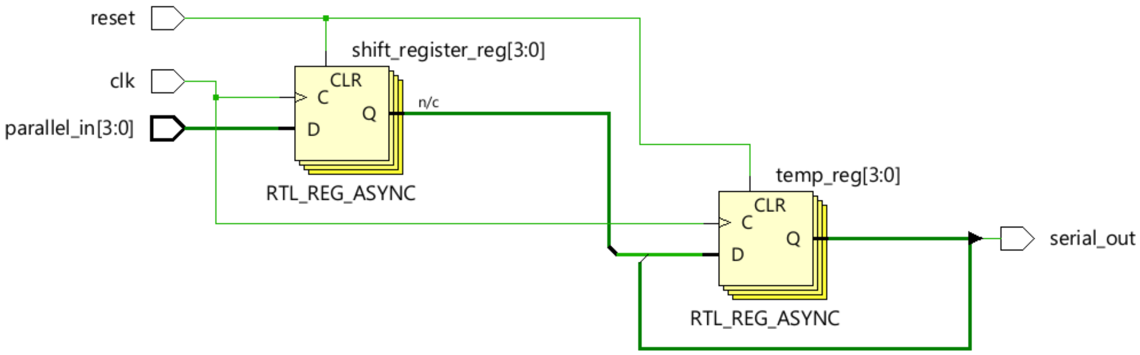
```
module PISORegister #(parameter N=4) (
  input clk,
  input reset,
  input [N-1:0] parallel_in,
  output serial_out
);
  reg [N-1:0] shift_register;
  reg [N-1:0] temp;
  always @(posedge clk or posedge reset) begin
    if (reset)
      shift_register <= 0;
    else
      shift_register <= parallel_in;
  end
  always @(posedge clk or posedge reset) begin
    if (reset)
      temp <= 0;
    else
      temp <= {shift_register[N-2:0], temp[N-1]};
  end
  assign serial_out = temp[0];
endmodule
```

Test Bench:



```
module PISORegister_TB;
  parameter N = 4;
  parameter CLK_PERIOD = 10;
  reg clk;
  reg reset;
  integer parallel_in;
  wire serial_out;
  piso_shift_register #(N) uut (
    .clk(clk),
    .reset(reset),
    .parallel_in(parallel_in),
    .serial_out(serial_out)
  );
  always begin
    #(CLK_PERIOD / 2 )clk = ~clk;
  end
  initial begin
    $display("PISO Shift Register Testbench");
    clk = 0;
    reset = 1;
    parallel_in = 4'b0000;
    #CLK_PERIOD reset = 0;
    parallel_in = 4'b1010;
    #CLK_PERIOD parallel_in = 4'b0101;
    reset = 1;
    #CLK_PERIOD reset = 0;
    $display("Serial Out: %b", serial_out);
    $finish;
  end
endmodule
```

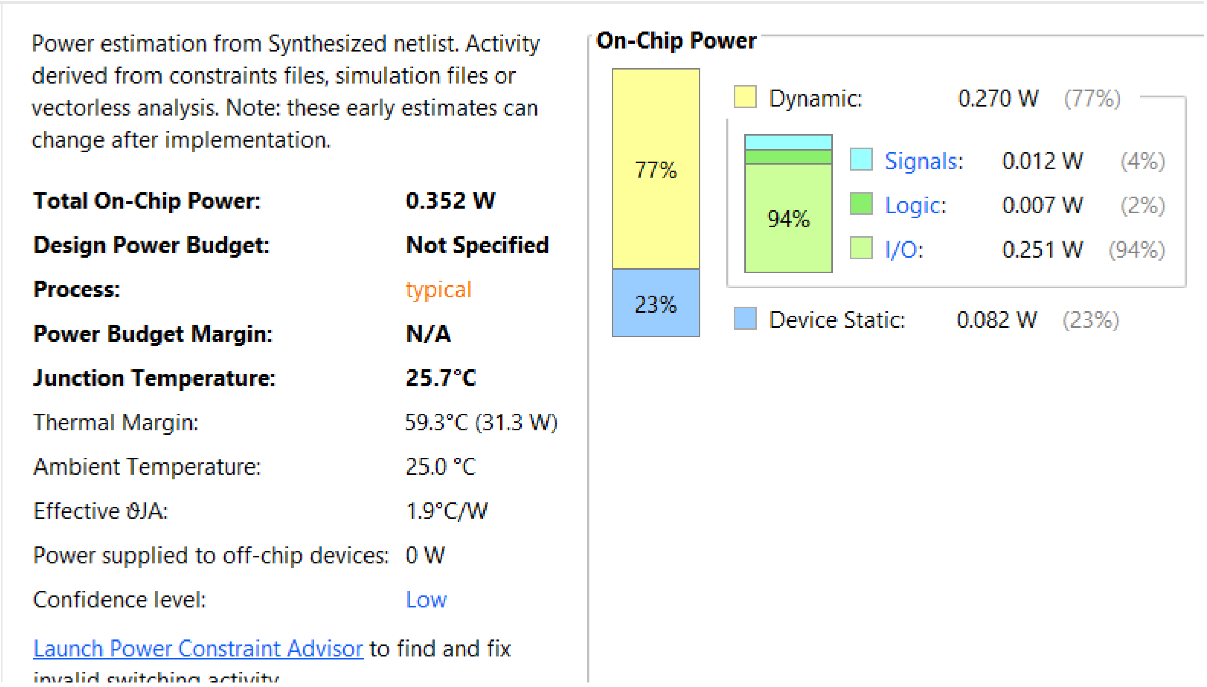
RTL Schematic:



Synthesis Report:

```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |FDCE |     3|
|3     |IBUF |     3|
|4     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     8|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:14 ; elapsed = 00:00:25
---------------------------------------------------------------------------------
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.352 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.7°C**
Thermal Margin:	59.3°C (31.3 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

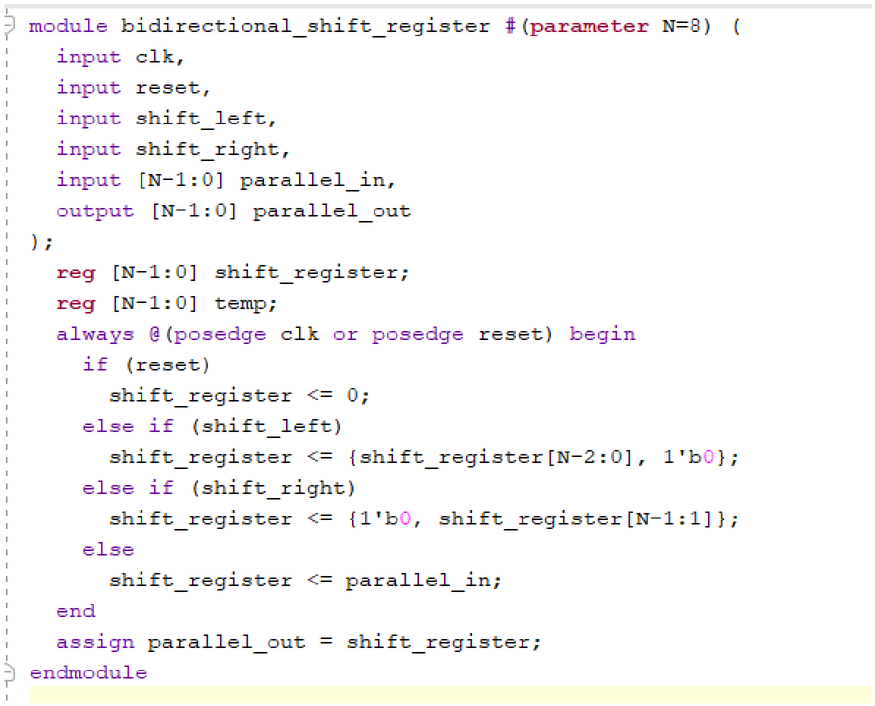
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	0.270 W	(77%)
Signals:	0.012 W	(4%)
Logic:	0.007 W	(2%)
I/O:	0.251 W	(94%)
Device Static:	0.082 W	(23%)

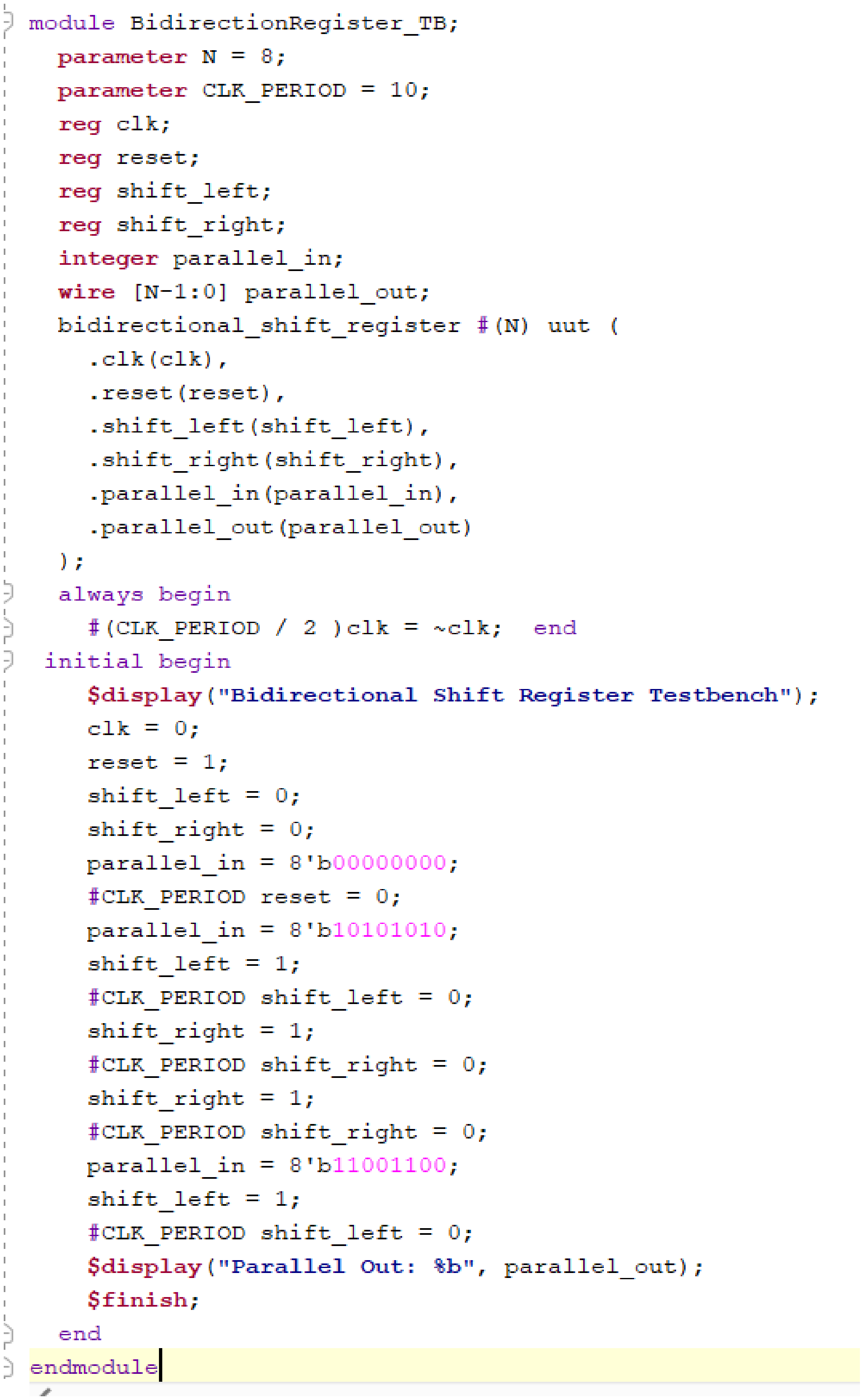
14. Bi-Direction Shift Register :-

Verilog Code:



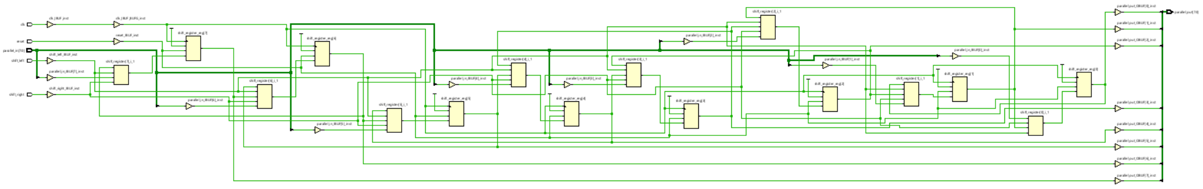
```
module bidirectional_shift_register #(parameter N=8) (
  input clk,
  input reset,
  input shift_left,
  input shift_right,
  input [N-1:0] parallel_in,
  output [N-1:0] parallel_out
);
  reg [N-1:0] shift_register;
  reg [N-1:0] temp;
  always @(posedge clk or posedge reset) begin
    if (reset)
      shift_register <= 0;
    else if (shift_left)
      shift_register <= {shift_register[N-2:0], 1'b0};
    else if (shift_right)
      shift_register <= {1'b0, shift_register[N-1:1]};
    else
      shift_register <= parallel_in;
  end
  assign parallel_out = shift_register;
endmodule
```

Test Bench:



```
module BidirectionRegister_TB;
  parameter N = 8;
  parameter CLK_PERIOD = 10;
  reg clk;
  reg reset;
  reg shift_left;
  reg shift_right;
  integer parallel_in;
  wire [N-1:0] parallel_out;
  bidirectional_shift_register #(N) uut (
    .clk(clk),
    .reset(reset),
    .shift_left(shift_left),
    .shift_right(shift_right),
    .parallel_in(parallel_in),
    .parallel_out(parallel_out)
  );
  always begin
    #(CLK_PERIOD / 2 )clk = ~clk;  end
 initial begin
    $display("Bidirectional Shift Register Testbench");
    clk = 0;
    reset = 1;
    shift_left = 0;
    shift_right = 0;
    parallel_in = 8'b00000000;
    #CLK_PERIOD reset = 0;
    parallel_in = 8'b10101010;
    shift_left = 1;
    #CLK_PERIOD shift_left = 0;
    shift_right = 1;
    #CLK_PERIOD shift_right = 0;
    shift_right = 1;
    #CLK_PERIOD shift_right = 0;
    parallel_in = 8'b11001100;
    shift_left = 1;
    #CLK_PERIOD shift_left = 0;
    $display("Parallel Out: %b", parallel_out);
    $finish;
  end
endmodule
```

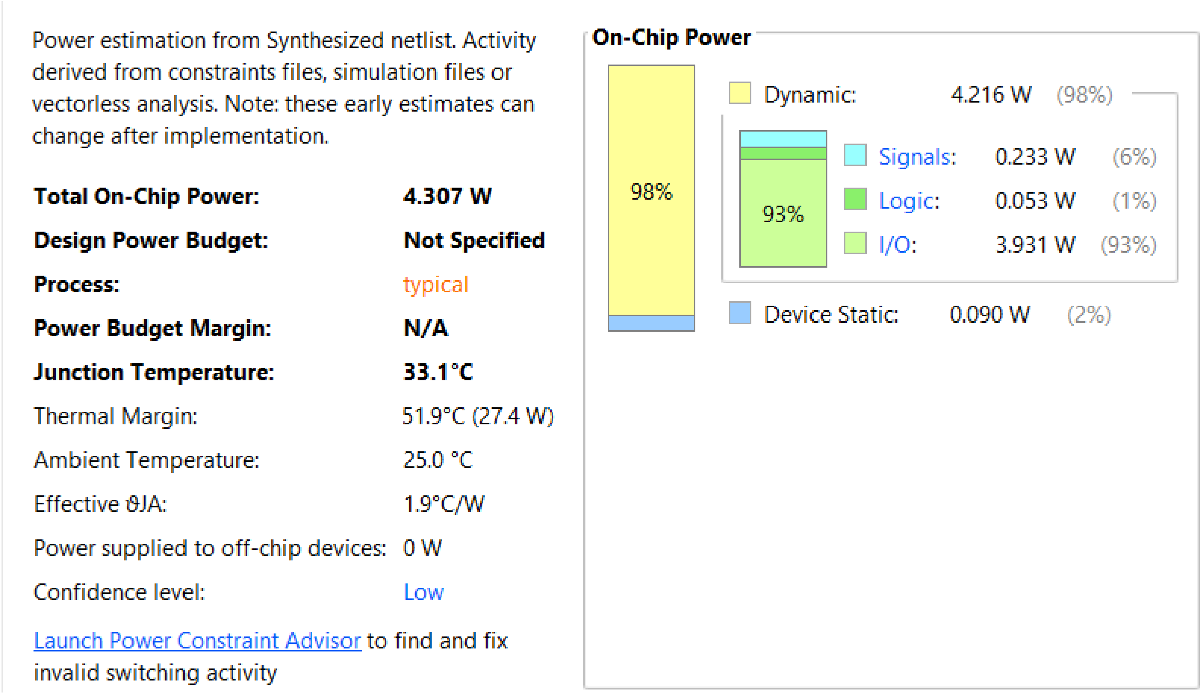
RTL Schematic:



Synthesis Report:

```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT4 |     2|
|3     |LUT5 |     6|
|4     |FDCE |     8|
|5     |IBUF |    12|
|6     |OBUF |     8|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    37|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:17 ; elapsed = 00:00:27
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**4.307 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**33.1°C**
Thermal Margin:	51.9°C (27.4 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

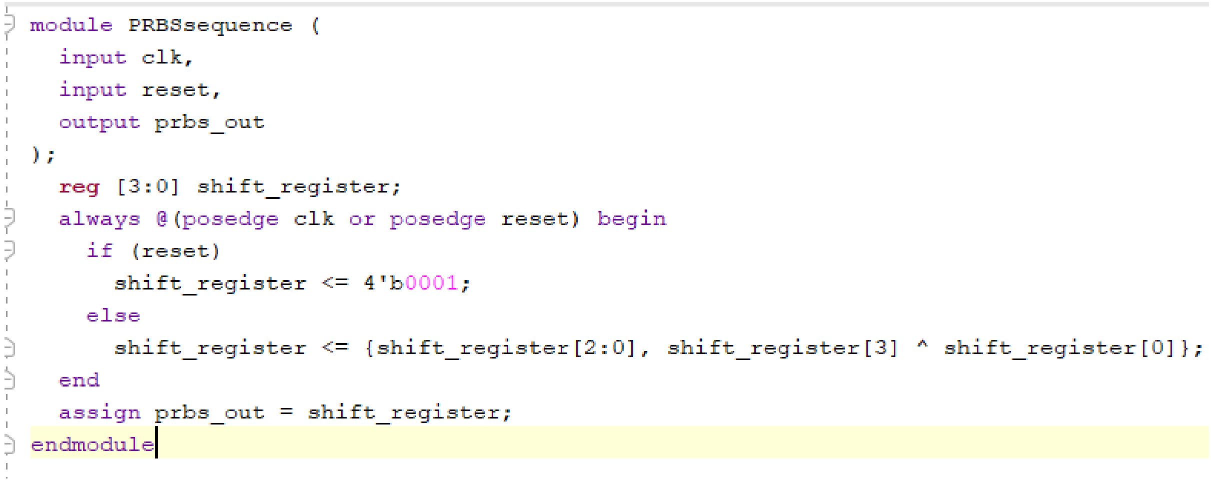
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨	Dynamic:	4.216 W	(98%)
🟦	Signals:	0.233 W	(6%)
🟩	Logic:	0.053 W	(1%)
🟩	I/O:	3.931 W	(93%)
🟦	Device Static:	0.090 W	(2%)

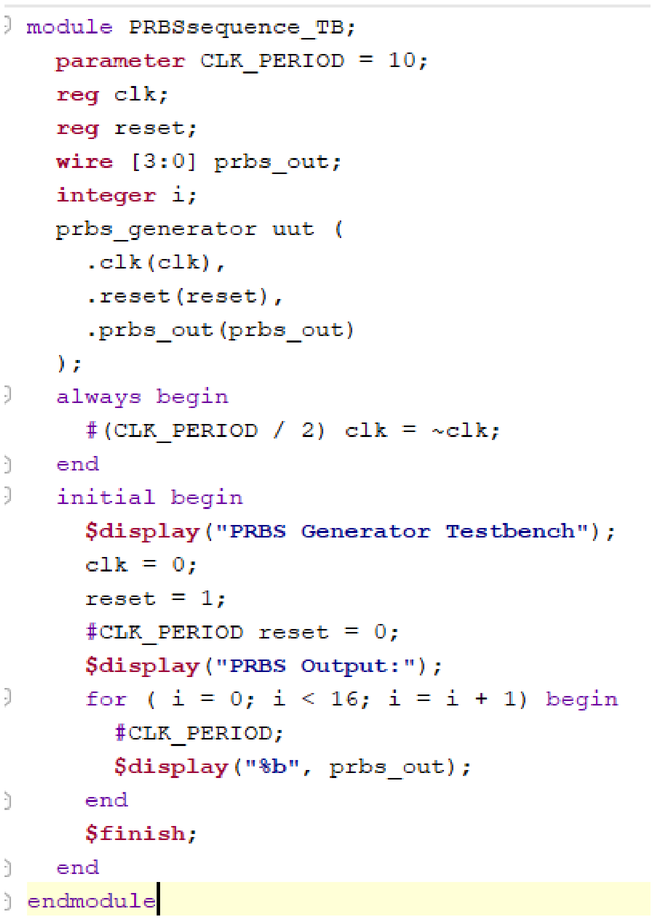
15. PRBS Sequence Generator :-

Verilog Code:



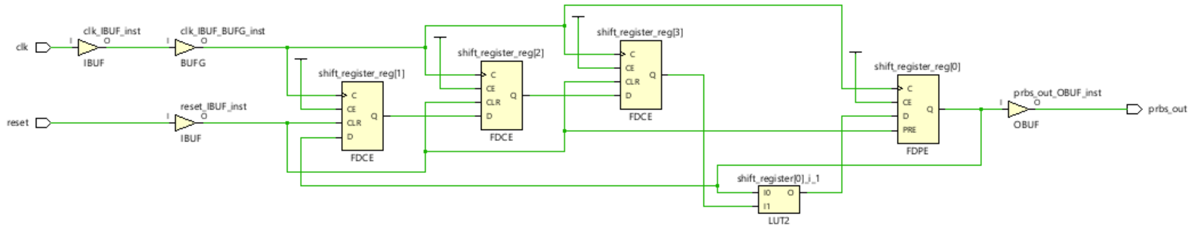
```verilog
module PRBSsequence (
  input clk,
  input reset,
  output prbs_out
);
  reg [3:0] shift_register;
  always @(posedge clk or posedge reset) begin
    if (reset)
      shift_register <= 4'b0001;
    else
      shift_register <= {shift_register[2:0], shift_register[3] ^ shift_register[0]};
  end
  assign prbs_out = shift_register;
endmodule
```

Test Bench:

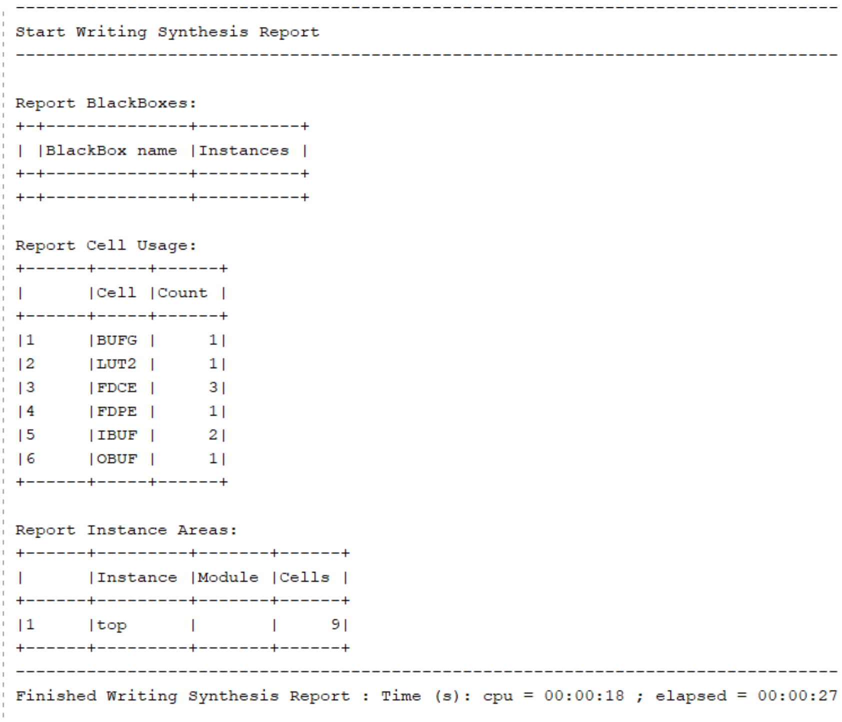


```verilog
module PRBSsequence_TB;
  parameter CLK_PERIOD = 10;
  reg clk;
  reg reset;
  wire [3:0] prbs_out;
  integer i;
  prbs_generator uut (
    .clk(clk),
    .reset(reset),
    .prbs_out(prbs_out)
  );
  always begin
    #(CLK_PERIOD / 2) clk = ~clk;
  end
  initial begin
    $display("PRBS Generator Testbench");
    clk = 0;
    reset = 1;
    #CLK_PERIOD reset = 0;
    $display("PRBS Output:");
    for ( i = 0; i < 16; i = i + 1) begin
      #CLK_PERIOD;
      $display("%b", prbs_out);
    end
    $finish;
  end
endmodule
```

RTL Schematic:

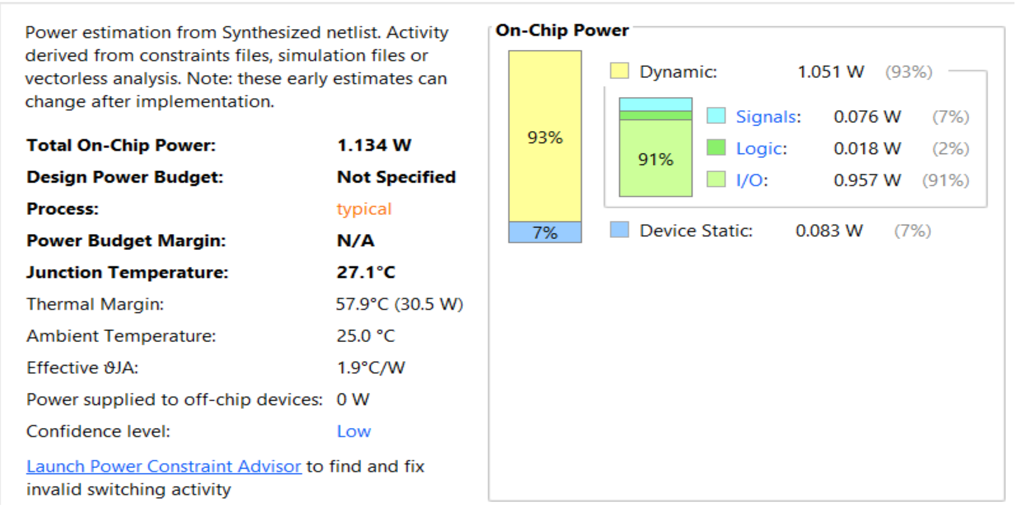


Synthesis Report:



```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT2 |     1|
|3     |FDCE |     3|
|4     |FDPE |     1|
|5     |IBUF |     2|
|6     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     9|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:18 ; elapsed = 00:00:27
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.134 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**27.1°C**
Thermal Margin:	57.9°C (30.5 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

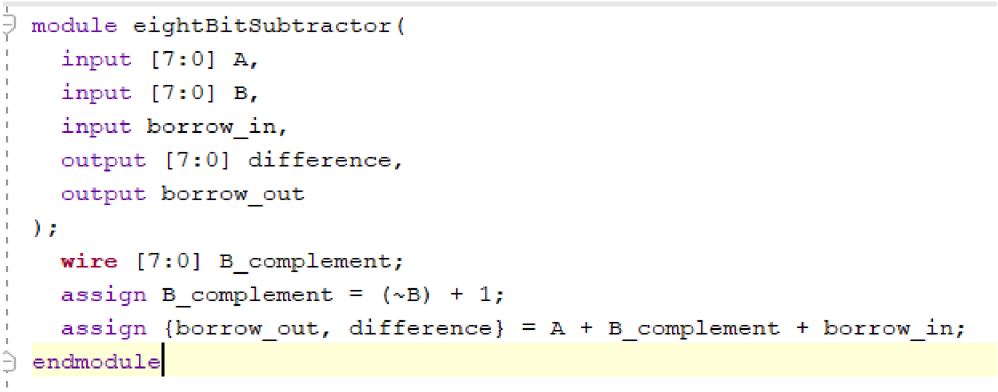
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨	Dynamic:	1.051 W	(93%)
🟦	Signals:	0.076 W	(7%)
🟩	Logic:	0.018 W	(2%)
🟩	I/O:	0.957 W	(91%)
🟦	Device Static:	0.083 W	(7%)

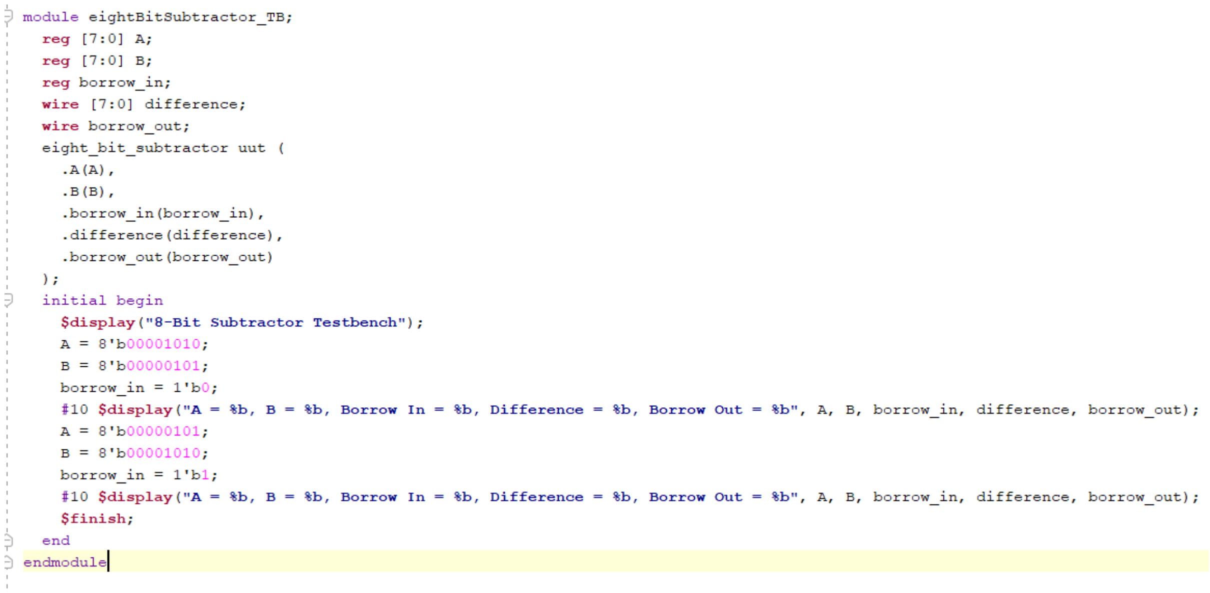
16. 8-Bit Subtractor :-

Verilog Code:



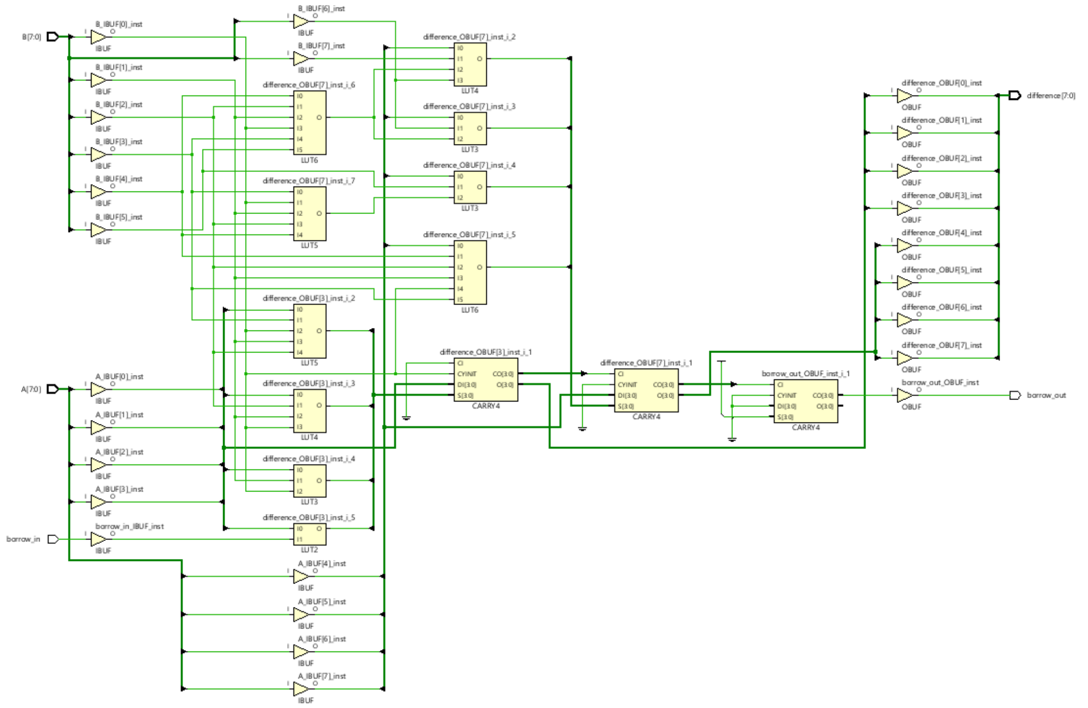
```
module eightBitSubtractor(
  input [7:0] A,
  input [7:0] B,
  input borrow_in,
  output [7:0] difference,
  output borrow_out
);
  wire [7:0] B_complement;
  assign B_complement = (~B) + 1;
  assign {borrow_out, difference} = A + B_complement + borrow_in;
endmodule
```

Test Bench:



```
module eightBitSubtractor_TB;
  reg [7:0] A;
  reg [7:0] B;
  reg borrow_in;
  wire [7:0] difference;
  wire borrow_out;
  eight_bit_subtractor uut (
    .A(A),
    .B(B),
    .borrow_in(borrow_in),
    .difference(difference),
    .borrow_out(borrow_out)
  );
  initial begin
    $display("8-Bit Subtractor Testbench");
    A = 8'b00001010;
    B = 8'b00000101;
    borrow_in = 1'b0;
    #10 $display("A = %b, B = %b, Borrow In = %b, Difference = %b, Borrow Out = %b", A, B, borrow_in, difference, borrow_out);
    A = 8'b00000101;
    B = 8'b00001010;
    borrow_in = 1'b1;
    #10 $display("A = %b, B = %b, Borrow In = %b, Difference = %b, Borrow Out = %b", A, B, borrow_in, difference, borrow_out);
    $finish;
  end
endmodule
```

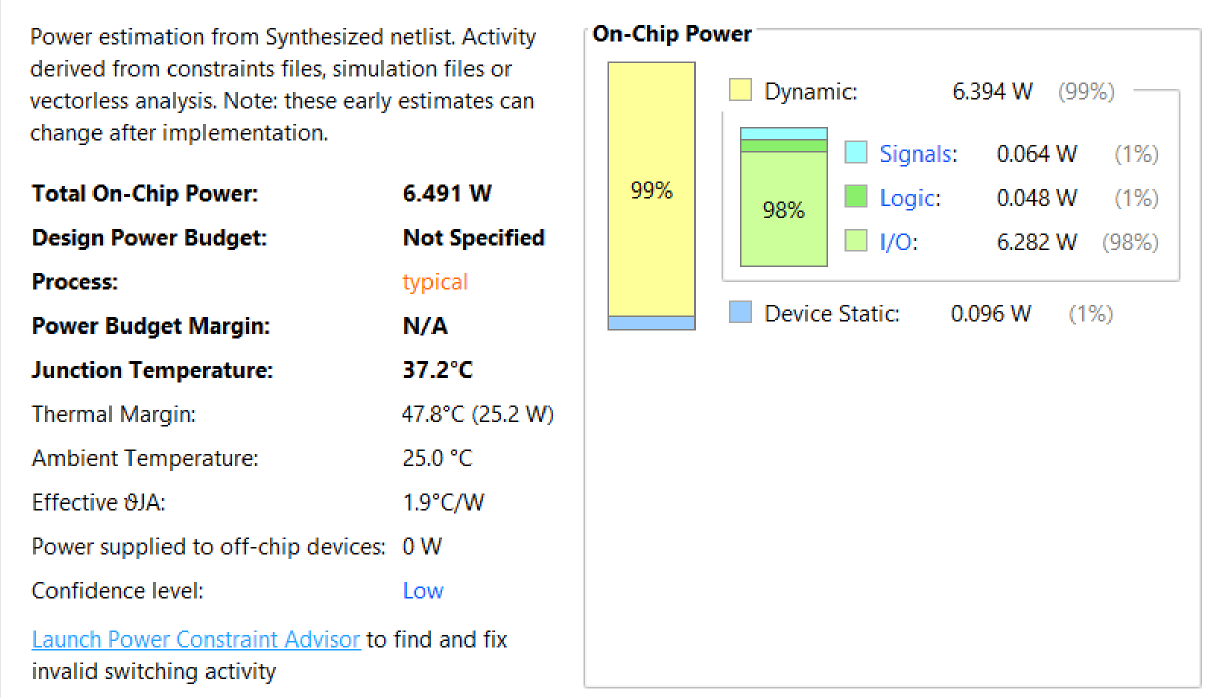
RTL Schematic:



Synthesis Report:

```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |CARRY4 |     3|
|2     |LUT2   |     1|
|3     |LUT3   |     3|
|4     |LUT4   |     2|
|5     |LUT5   |     2|
|6     |LUT6   |     2|
|7     |IBUF   |    17|
|8     |OBUF   |     9|
+------+-------+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    39|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:18 ; elapsed = 00:00:29
---------------------------------------------------------------------------------
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**6.491 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**37.2°C**
Thermal Margin:	47.8°C (25.2 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

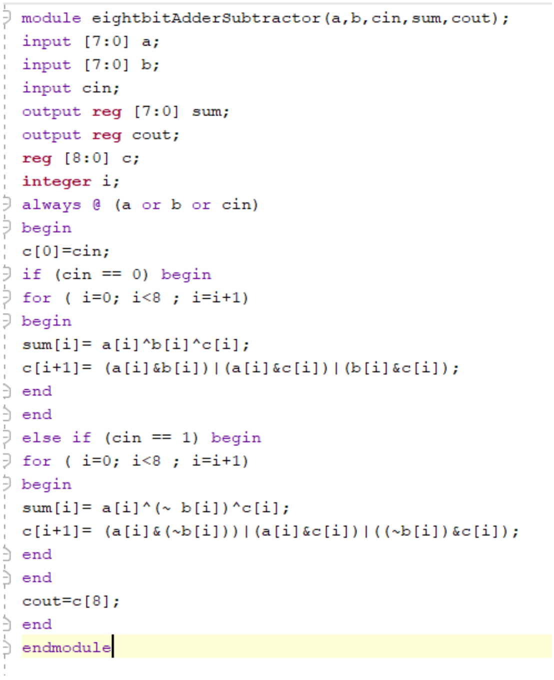
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨 Dynamic:	6.394 W	(99%)
🟦 Signals:	0.064 W	(1%)
🟩 Logic:	0.048 W	(1%)
🟩 I/O:	6.282 W	(98%)
🟦 Device Static:	0.096 W	(1%)

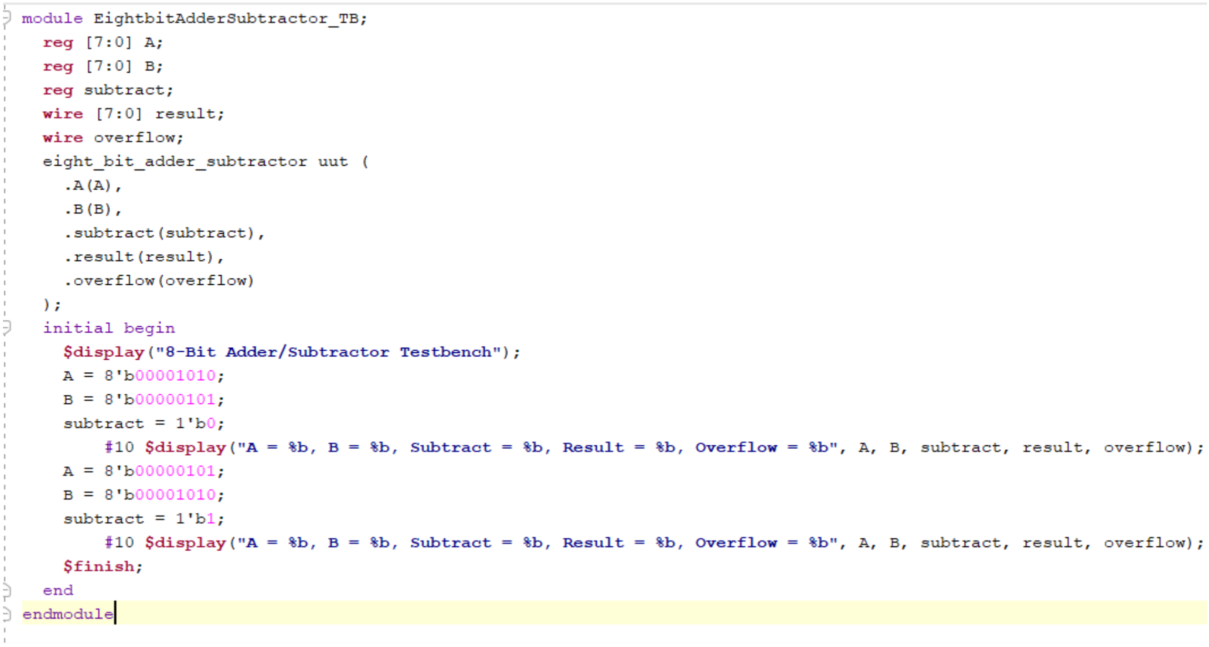
17. 8-Bit Adder/Subtractor :-

Verilog Code:



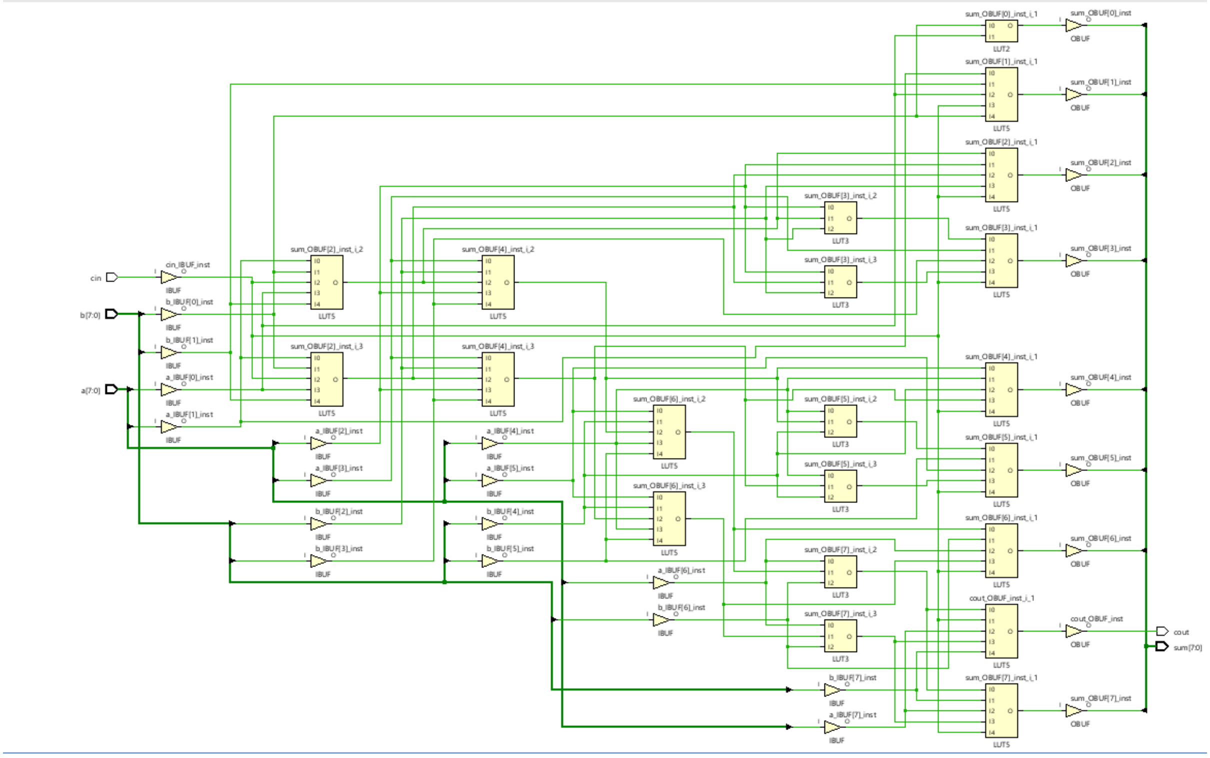
```
module eightbitAdderSubtractor(a,b,cin,sum,cout);
input [7:0] a;
input [7:0] b;
input cin;
output reg [7:0] sum;
output reg cout;
reg [8:0] c;
integer i;
always @ (a or b or cin)
begin
c[0]=cin;
if (cin == 0) begin
for ( i=0; i<8 ; i=i+1)
begin
sum[i]= a[i]^b[i]^c[i];
c[i+1]= (a[i]&b[i])|(a[i]&c[i])|(b[i]&c[i]);
end
end
else if (cin == 1) begin
for ( i=0; i<8 ; i=i+1)
begin
sum[i]= a[i]^(~ b[i])^c[i];
c[i+1]= (a[i]&(~b[i]))|(a[i]&c[i])|((~b[i])&c[i]);
end
end
cout=c[8];
end
endmodule
```

Test Bench:

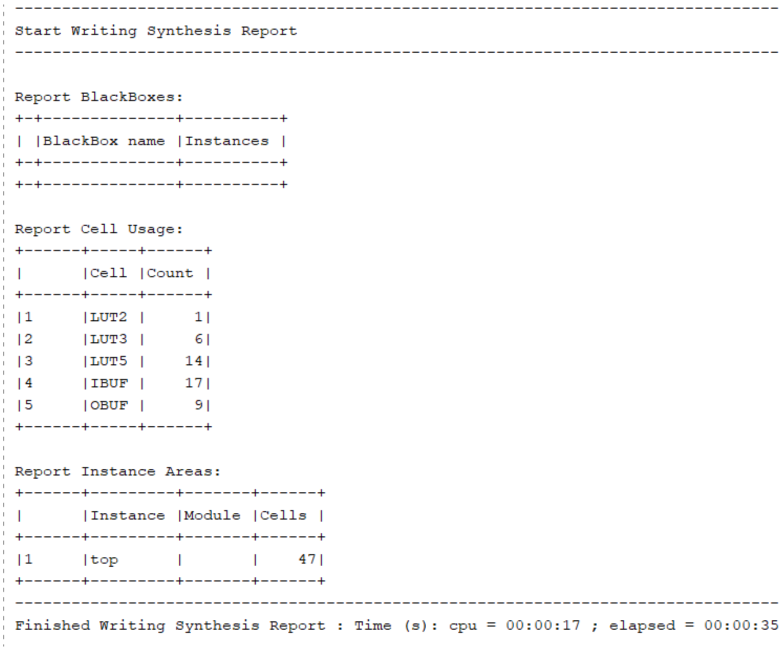


```
module EightbitAdderSubtractor_TB;
  reg [7:0] A;
  reg [7:0] B;
  reg subtract;
  wire [7:0] result;
  wire overflow;
  eight_bit_adder_subtractor uut (
    .A(A),
    .B(B),
    .subtract(subtract),
    .result(result),
    .overflow(overflow)
  );
  initial begin
    $display("8-Bit Adder/Subtractor Testbench");
    A = 8'b00001010;
    B = 8'b00000101;
    subtract = 1'b0;
        #10 $display("A = %b, B = %b, Subtract = %b, Result = %b, Overflow = %b", A, B, subtract, result, overflow);
    A = 8'b00000101;
    B = 8'b00001010;
    subtract = 1'b1;
        #10 $display("A = %b, B = %b, Subtract = %b, Result = %b, Overflow = %b", A, B, subtract, result, overflow);
    $finish;
  end
endmodule
```

RTL Schematic:

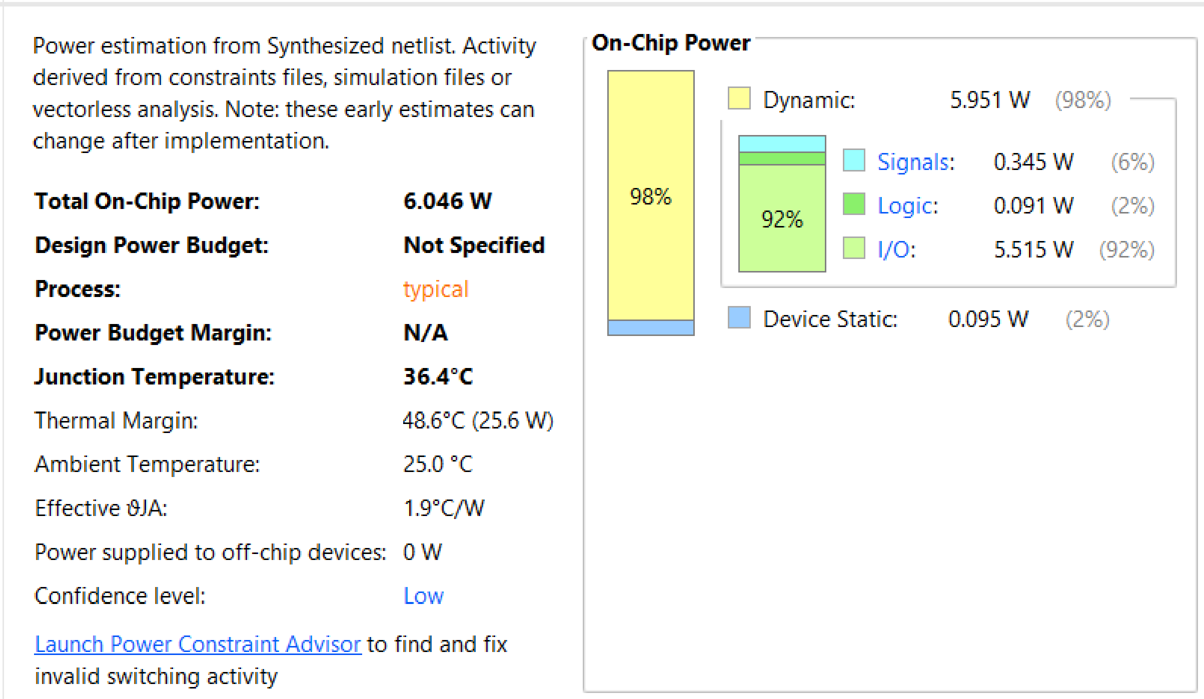


Synthesis Report:



```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT2 |     1|
|2     |LUT3 |     6|
|3     |LUT5 |    14|
|4     |IBUF |    17|
|5     |OBUF |     9|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    47|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:17 ; elapsed = 00:00:35
```

Power report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**6.046 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**36.4°C**
Thermal Margin:	48.6°C (25.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

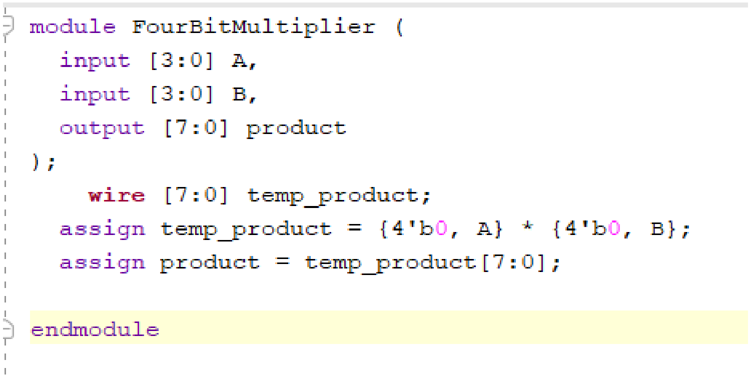
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨	Dynamic:	5.951 W	(98%)
🟦	Signals:	0.345 W	(6%)
🟩	Logic:	0.091 W	(2%)
🟩	I/O:	5.515 W	(92%)
🟦	Device Static:	0.095 W	(2%)

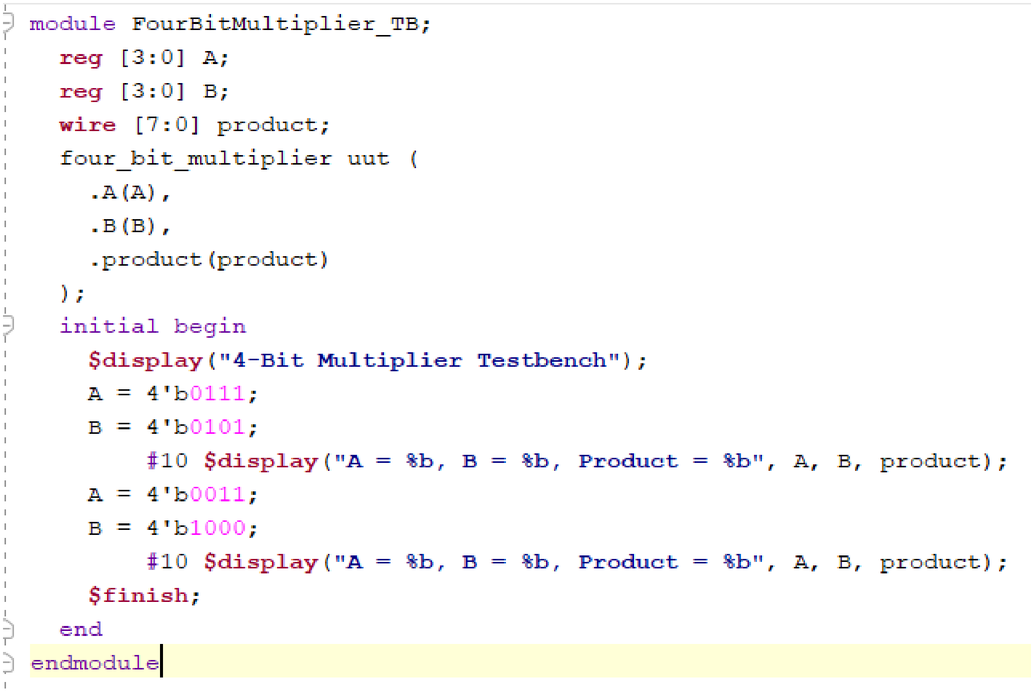
18. 4-Bit Multiplier :-

Verilog Code:



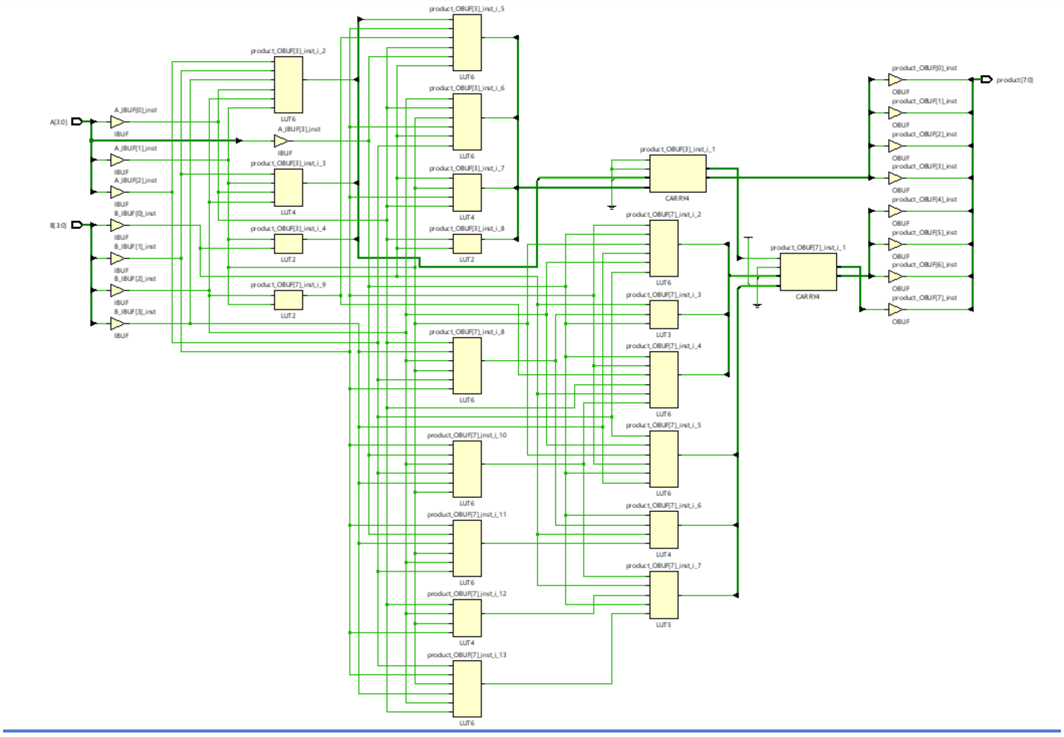
```
module FourBitMultiplier (
  input [3:0] A,
  input [3:0] B,
  output [7:0] product
);
    wire [7:0] temp_product;
  assign temp_product = {4'b0, A} * {4'b0, B};
  assign product = temp_product[7:0];

endmodule
```

Test Bench:

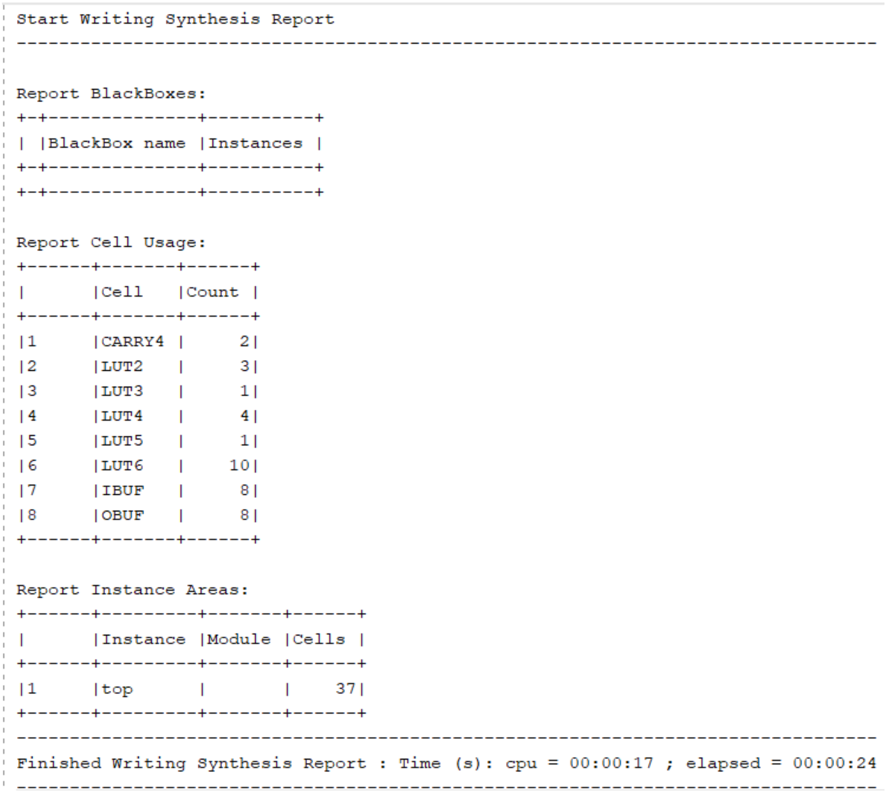


```
module FourBitMultiplier_TB;
  reg [3:0] A;
  reg [3:0] B;
  wire [7:0] product;
  four_bit_multiplier uut (
    .A(A),
    .B(B),
    .product(product)
  );
  initial begin
    $display("4-Bit Multiplier Testbench");
    A = 4'b0111;
    B = 4'b0101;
        #10 $display("A = %b, B = %b, Product = %b", A, B, product);
    A = 4'b0011;
    B = 4'b1000;
        #10 $display("A = %b, B = %b, Product = %b", A, B, product);
    $finish;
  end
endmodule
```

RTL Schematic:

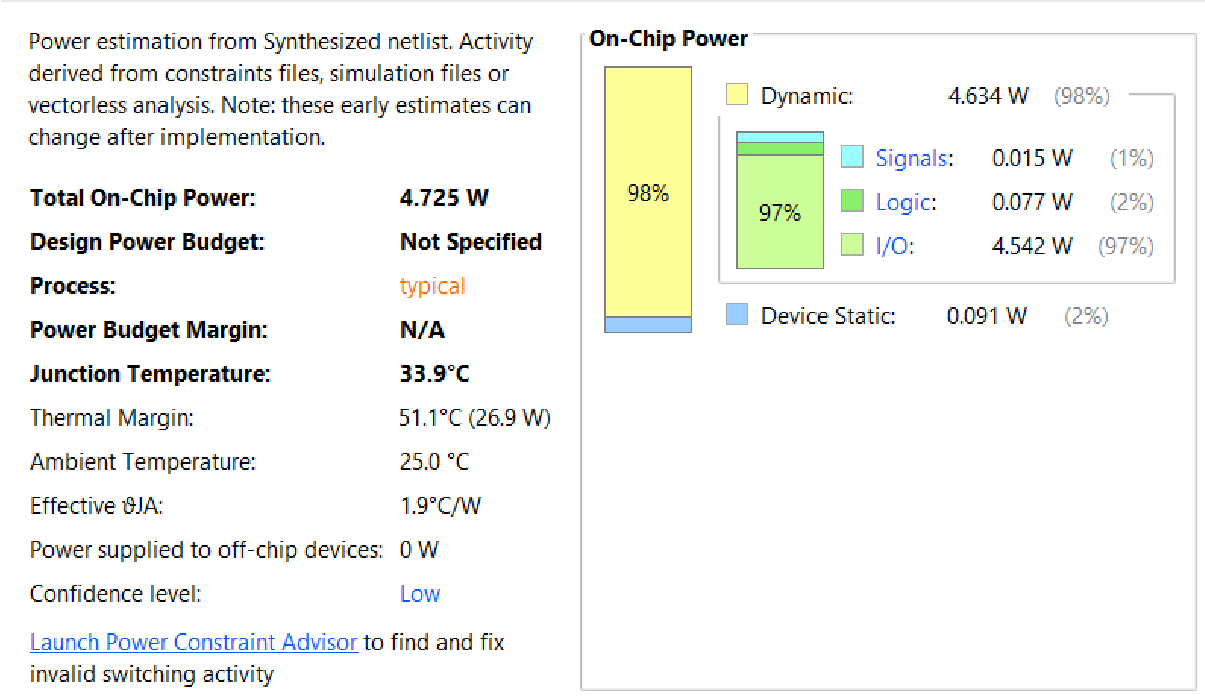


Synthesis Report:



```
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |CARRY4 |     2|
|2     |LUT2   |     3|
|3     |LUT3   |     1|
|4     |LUT4   |     4|
|5     |LUT5   |     1|
|6     |LUT6   |    10|
|7     |IBUF   |     8|
|8     |OBUF   |     8|
+------+-------+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    37|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:17 ; elapsed = 00:00:24
---------------------------------------------------------------------------------
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**4.725 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**33.9°C**
Thermal Margin:	51.1°C (26.9 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

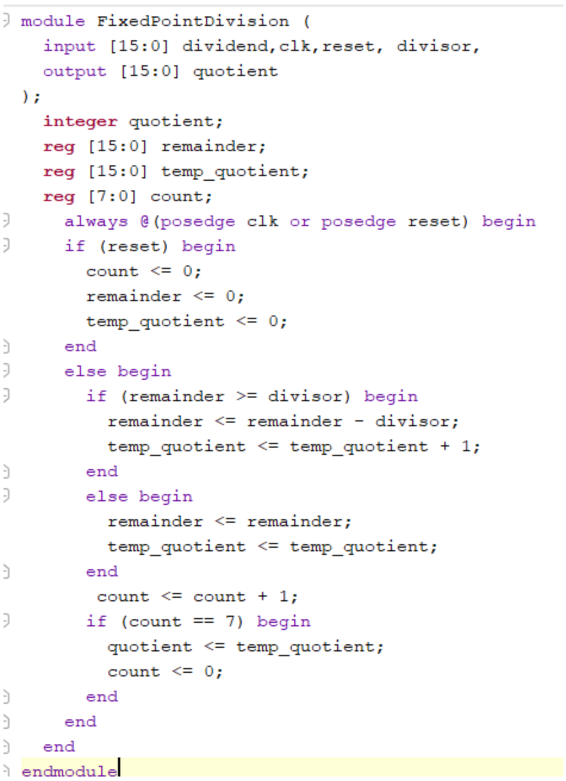
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	4.634 W	(98%)
Signals:	0.015 W	(1%)
Logic:	0.077 W	(2%)
I/O:	4.542 W	(97%)
Device Static:	0.091 W	(2%)

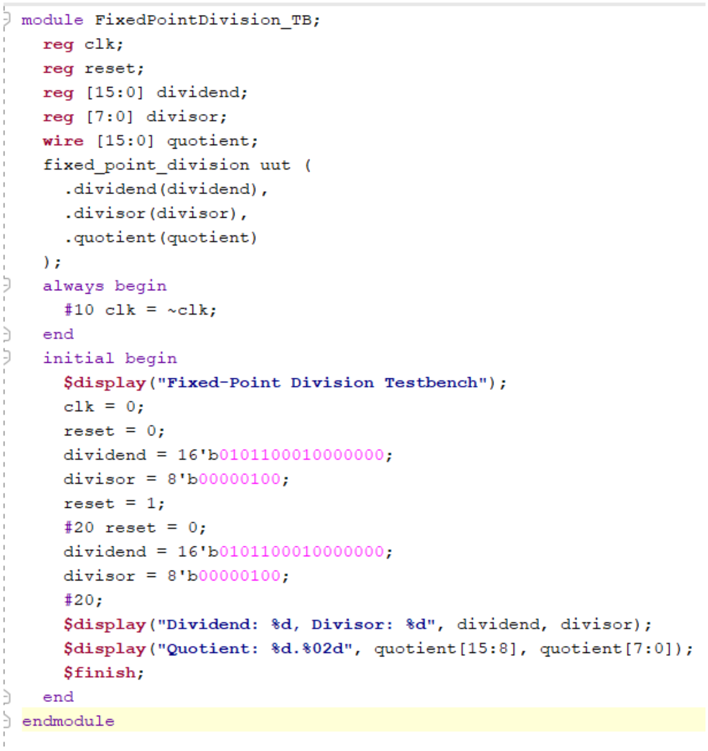
19. Fixed Point Division :-

Verilog Code:



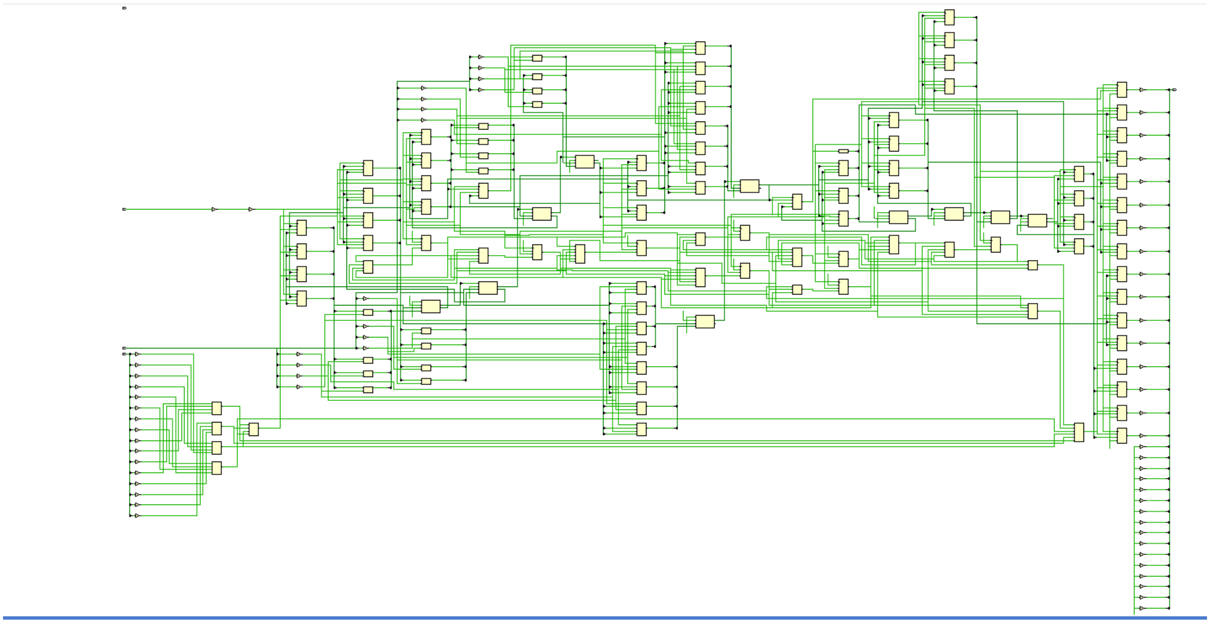
```
module FixedPointDivision (
  input [15:0] dividend,clk,reset, divisor,
  output [15:0] quotient
);
  integer quotient;
  reg [15:0] remainder;
  reg [15:0] temp_quotient;
  reg [7:0] count;
    always @(posedge clk or posedge reset) begin
    if (reset) begin
      count <= 0;
      remainder <= 0;
      temp_quotient <= 0;
    end
    else begin
      if (remainder >= divisor) begin
        remainder <= remainder - divisor;
        temp_quotient <= temp_quotient + 1;
      end
      else begin
        remainder <= remainder;
        temp_quotient <= temp_quotient;
      end
       count <= count + 1;
      if (count == 7) begin
        quotient <= temp_quotient;
        count <= 0;
      end
    end
  end
endmodule
```

Test Bench:

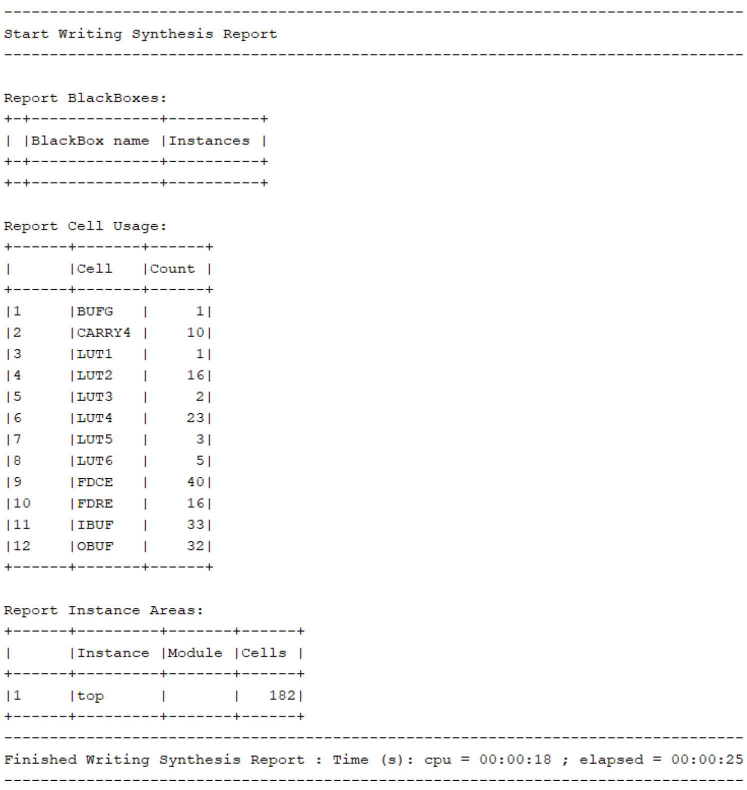


```
module FixedPointDivision_TB;
  reg clk;
  reg reset;
  reg [15:0] dividend;
  reg [7:0] divisor;
  wire [15:0] quotient;
  fixed_point_division uut (
    .dividend(dividend),
    .divisor(divisor),
    .quotient(quotient)
  );
  always begin
    #10 clk = ~clk;
  end
  initial begin
    $display("Fixed-Point Division Testbench");
    clk = 0;
    reset = 0;
    dividend = 16'b0101100010000000;
    divisor = 8'b00000100;
    reset = 1;
    #20 reset = 0;
    dividend = 16'b0101100010000000;
    divisor = 8'b00000100;
    #20;
    $display("Dividend: %d, Divisor: %d", dividend, divisor);
    $display("Quotient: %d.%02d", quotient[15:8], quotient[7:0]);
    $finish;
  end
endmodule
```

RTL Schematic:

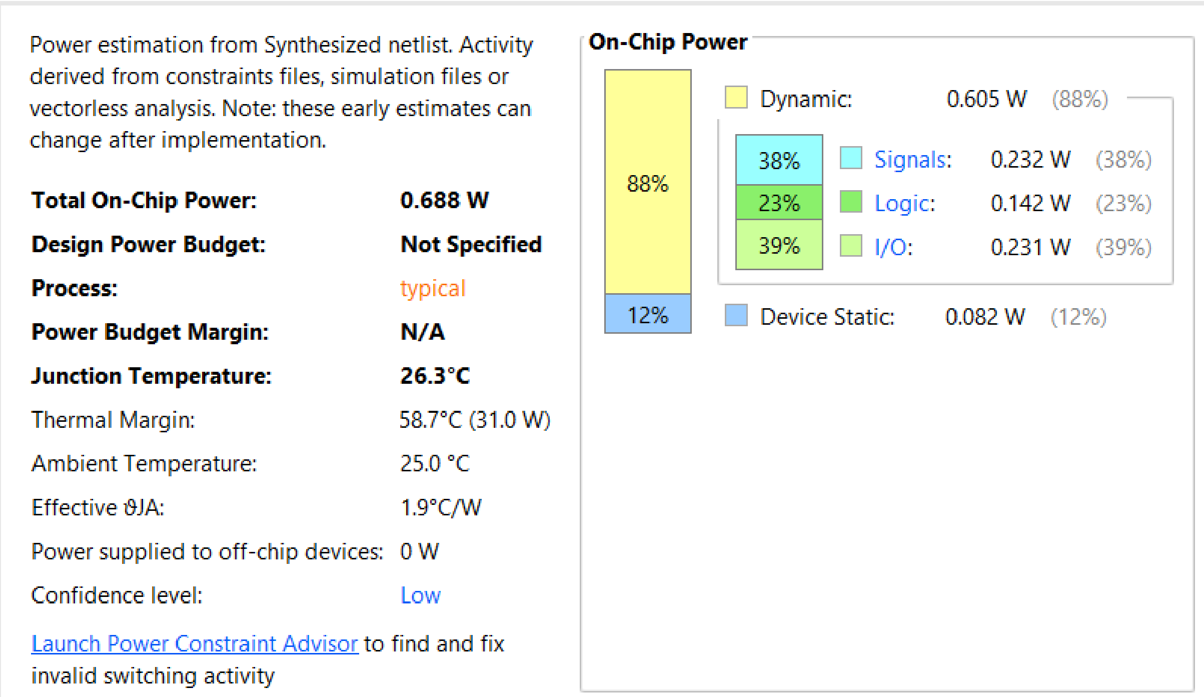


Synthesis Report:



```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     1|
|2     |CARRY4 |    10|
|3     |LUT1   |     1|
|4     |LUT2   |    16|
|5     |LUT3   |     2|
|6     |LUT4   |    23|
|7     |LUT5   |     3|
|8     |LUT6   |     5|
|9     |FDCE   |    40|
|10    |FDRE   |    16|
|11    |IBUF   |    33|
|12    |OBUF   |    32|
+------+-------+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |   182|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:18 ; elapsed = 00:00:25
---------------------------------------------------------------------------------
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.688 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**26.3°C**
Thermal Margin:	58.7°C (31.0 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

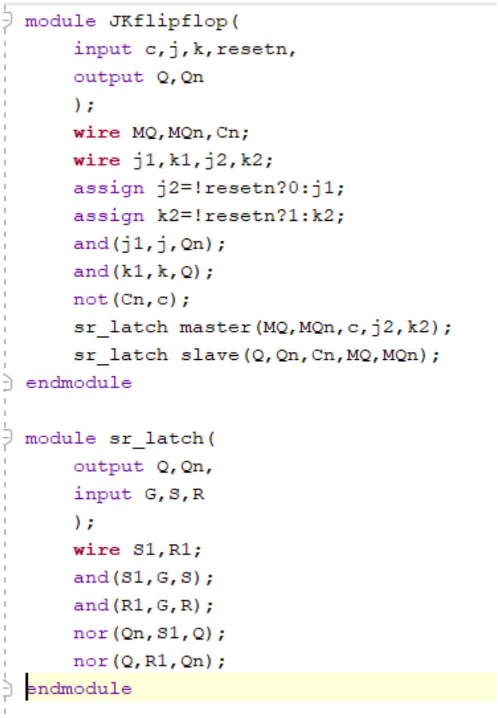
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨	Dynamic:	0.605 W	(88%)
🟦	Signals:	0.232 W	(38%)
🟩	Logic:	0.142 W	(23%)
🟩	I/O:	0.231 W	(39%)
🟦	Device Static:	0.082 W	(12%)

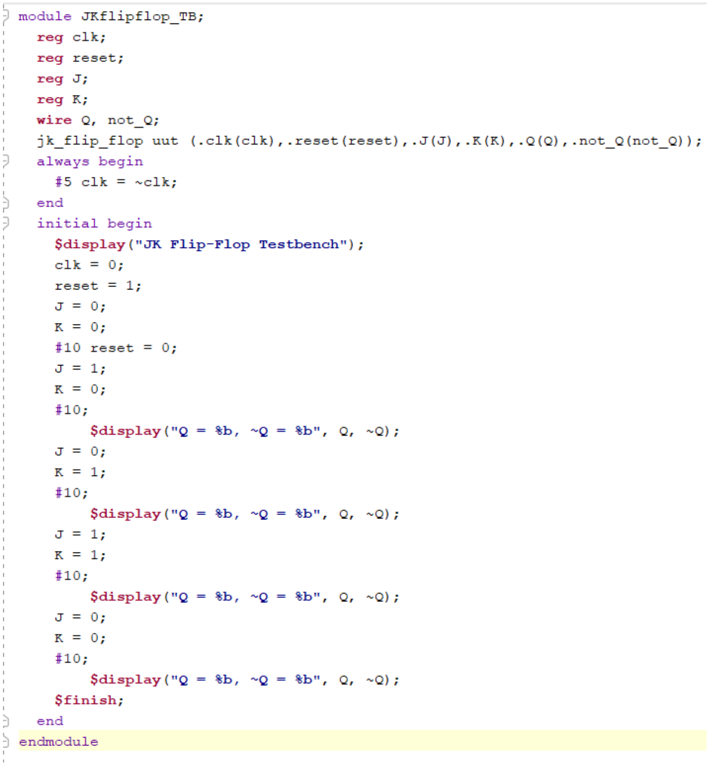
20. Master Slave JK Flip Flop :-

Verilog Code:



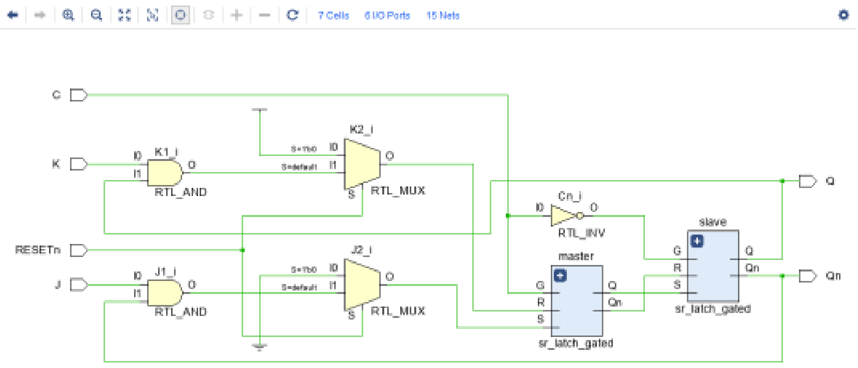
```
module JKflipflop(
    input c,j,k,resetn,
    output Q,Qn
    );
    wire MQ,MQn,Cn;
    wire j1,k1,j2,k2;
    assign j2=!resetn?0:j1;
    assign k2=!resetn?1:k2;
    and(j1,j,Qn);
    and(k1,k,Q);
    not(Cn,c);
    sr_latch master(MQ,MQn,c,j2,k2);
    sr_latch slave(Q,Qn,Cn,MQ,MQn);
endmodule

module sr_latch(
    output Q,Qn,
    input G,S,R
    );
    wire S1,R1;
    and(S1,G,S);
    and(R1,G,R);
    nor(Qn,S1,Q);
    nor(Q,R1,Qn);
endmodule
```

Test Bench:



```
module JKflipflop_TB;
  reg clk;
  reg reset;
  reg J;
  reg K;
  wire Q, not_Q;
  jk_flip_flop uut (.clk(clk),.reset(reset),.J(J),.K(K),.Q(Q),.not_Q(not_Q));
  always begin
    #5 clk = ~clk;
  end
  initial begin
    $display("JK Flip-Flop Testbench");
    clk = 0;
    reset = 1;
    J = 0;
    K = 0;
    #10 reset = 0;
    J = 1;
    K = 0;
    #10;
        $display("Q = %b, ~Q = %b", Q, ~Q);
    J = 0;
    K = 1;
    #10;
        $display("Q = %b, ~Q = %b", Q, ~Q);
    J = 1;
    K = 1;
    #10;
        $display("Q = %b, ~Q = %b", Q, ~Q);
    J = 0;
    K = 0;
    #10;
        $display("Q = %b, ~Q = %b", Q, ~Q);
    $finish;
  end
endmodule
```

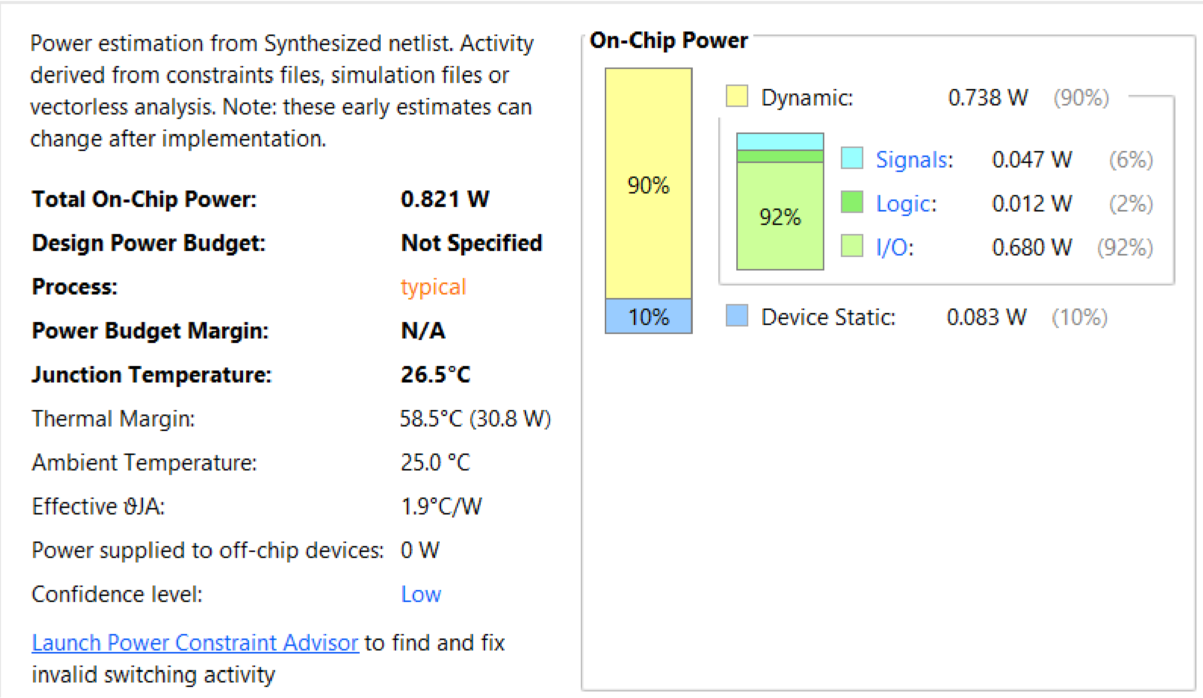
RTL Schematic:



Synthesis Report:

```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT2 |     1|
|2     |LUT3 |     2|
|3     |LUT6 |     1|
|4     |IBUF |     3|
|5     |OBUF |     2|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     9|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:14 ; elapsed = 00:00:16
---------------------------------------------------------------------------------
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.821 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**26.5°C**
Thermal Margin:	58.5°C (30.8 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

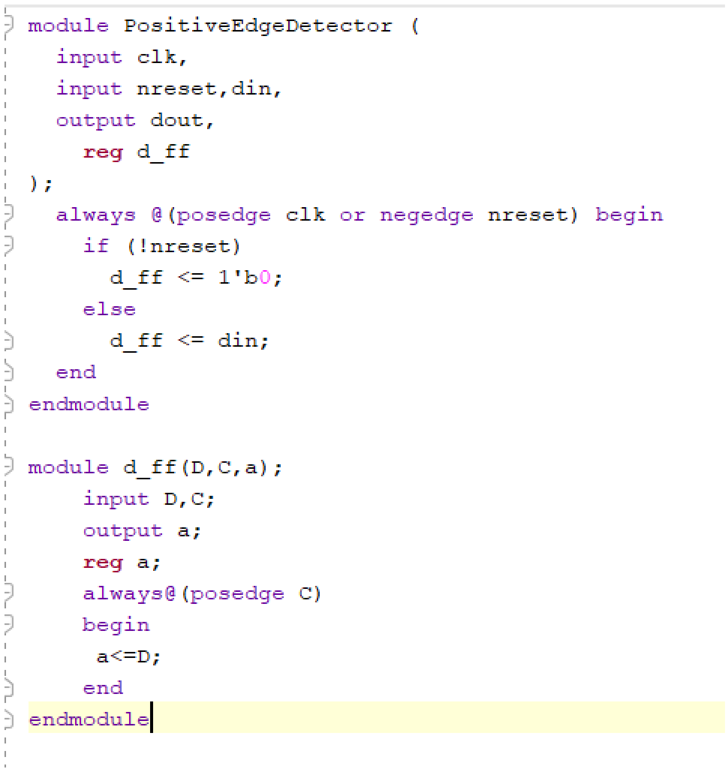
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨 Dynamic:	0.738 W	(90%)
🟦 Signals:	0.047 W	(6%)
🟩 Logic:	0.012 W	(2%)
🟩 I/O:	0.680 W	(92%)
🟦 Device Static:	0.083 W	(10%)

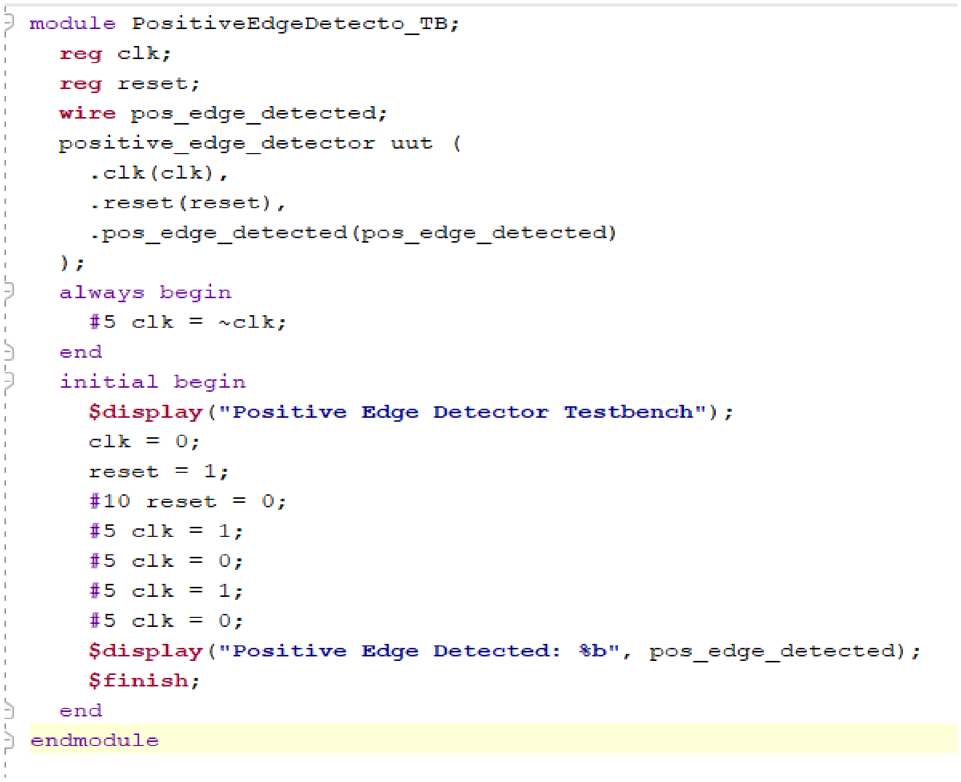
21. Positive Edge Detector :-

Verilog Code:



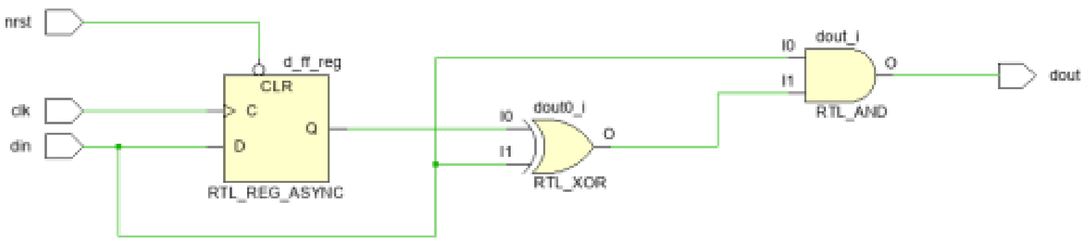
```
module PositiveEdgeDetector (
  input clk,
  input nreset,din,
  output dout,
    reg d_ff
);
  always @(posedge clk or negedge nreset) begin
    if (!nreset)
      d_ff <= 1'b0;
    else
      d_ff <= din;
  end
endmodule

module d_ff(D,C,a);
    input D,C;
    output a;
    reg a;
    always@(posedge C)
    begin
     a<=D;
    end
endmodule
```

Test Bench:



```
module PositiveEdgeDetecto_TB;
  reg clk;
  reg reset;
  wire pos_edge_detected;
  positive_edge_detector uut (
    .clk(clk),
    .reset(reset),
    .pos_edge_detected(pos_edge_detected)
  );
  always begin
    #5 clk = ~clk;
  end
  initial begin
    $display("Positive Edge Detector Testbench");
    clk = 0;
    reset = 1;
    #10 reset = 0;
    #5 clk = 1;
    #5 clk = 0;
    #5 clk = 1;
    #5 clk = 0;
    $display("Positive Edge Detected: %b", pos_edge_detected);
    $finish;
  end
endmodule
```

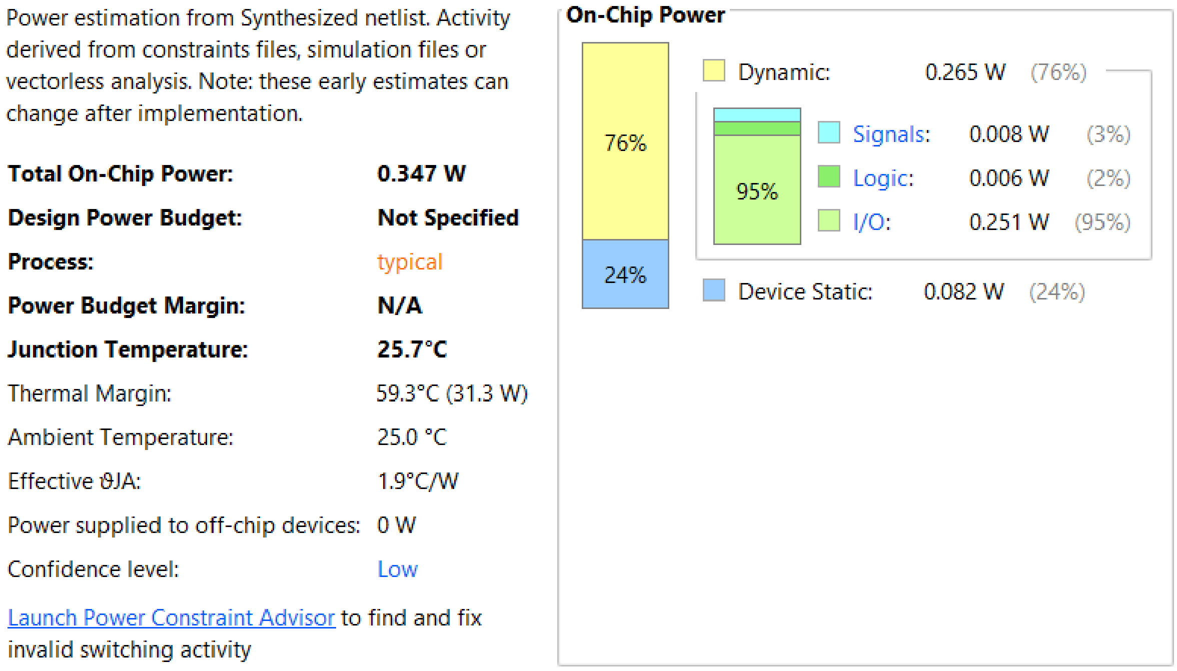
RTL Schematic:



Synthesis Report:

```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+------+------+
|      |Cell  |Count |
+------+------+------+
|1     |BUFG  |     1|
|2     |LUT1  |     1|
|3     |FDCE  |     1|
|4     |IBUF  |     3|
|5     |OBUF  |     1|
|6     |OBUFT |     1|
+------+------+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     8|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:13 ; elapsed = 00:00:15
---------------------------------------------------------------------------------
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.347 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.7°C**
Thermal Margin:	59.3°C (31.3 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

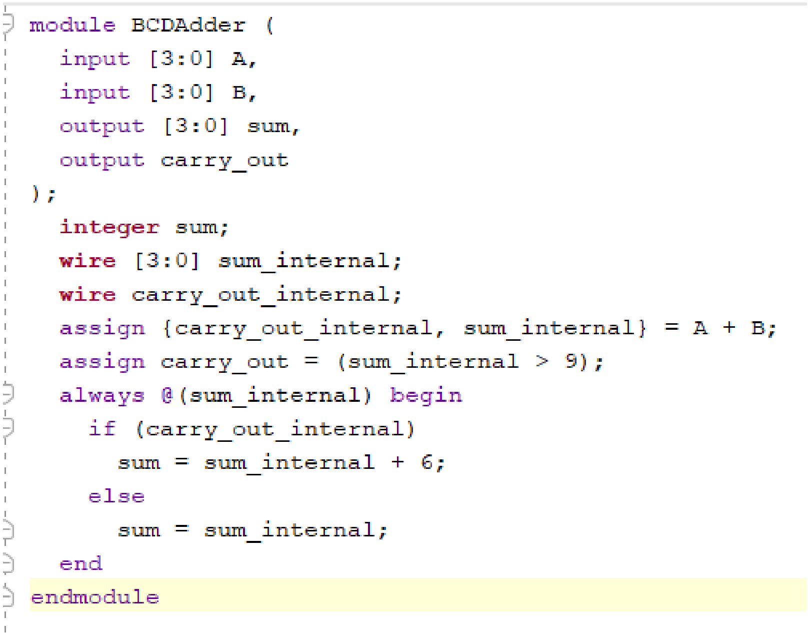
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨 Dynamic:	0.265 W	(76%)
🟦 Signals:	0.008 W	(3%)
🟩 Logic:	0.006 W	(2%)
🟩 I/O:	0.251 W	(95%)
🟦 Device Static:	0.082 W	(24%)

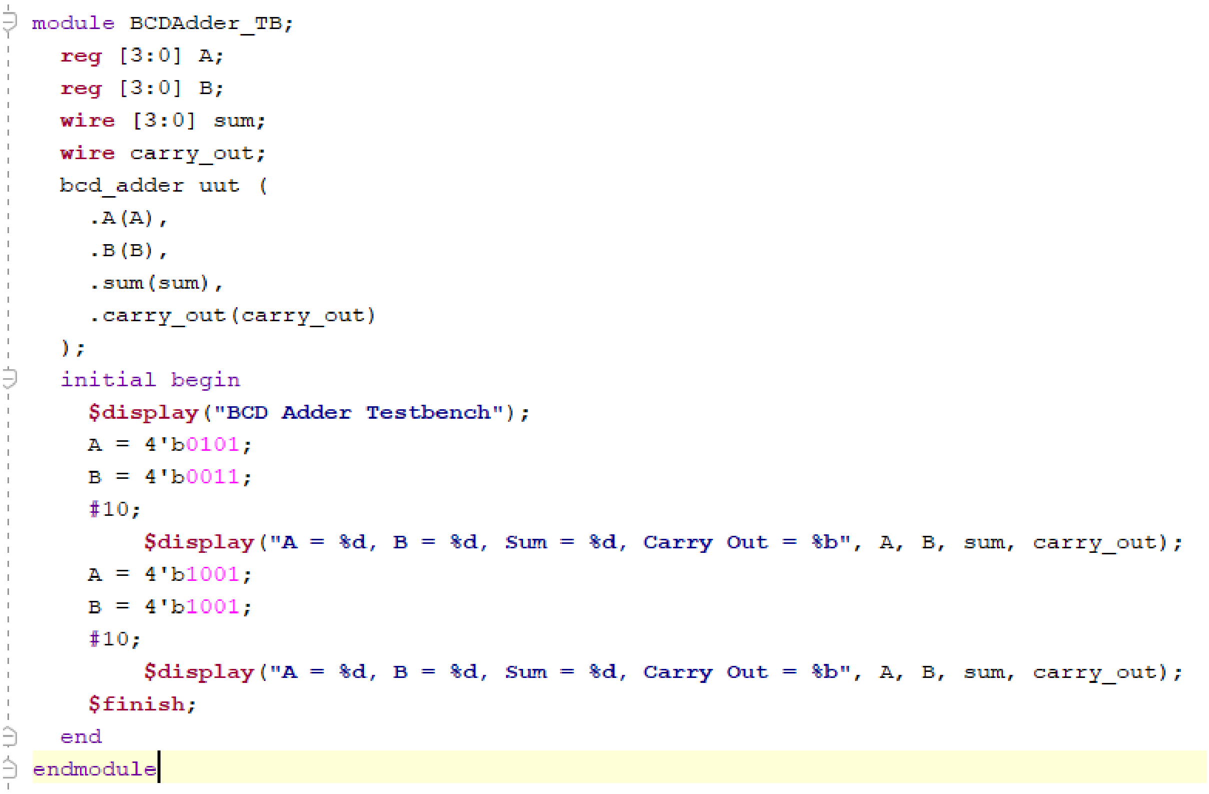
22. BCD Adder :-

Verilog Code:



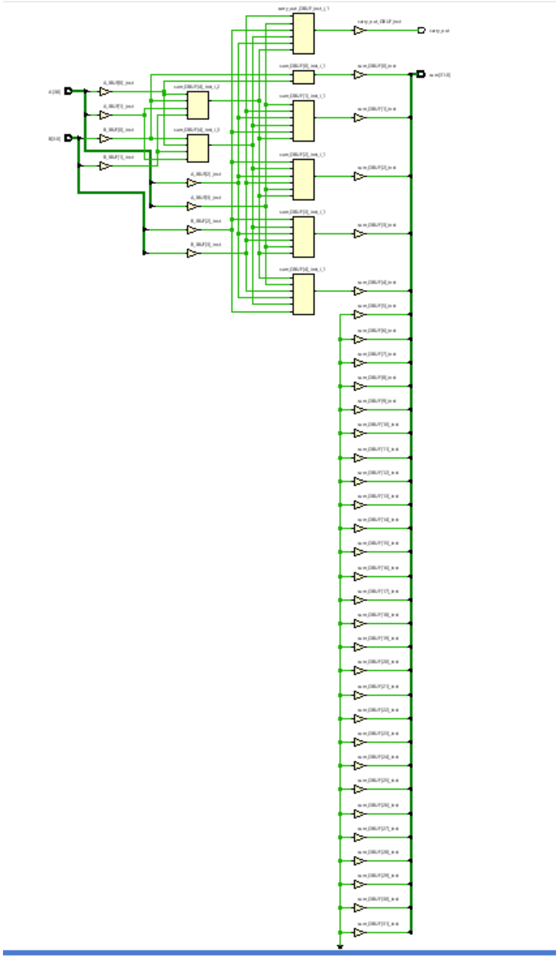
```
module BCDAdder (
  input [3:0] A,
  input [3:0] B,
  output [3:0] sum,
  output carry_out
);
  integer sum;
  wire [3:0] sum_internal;
  wire carry_out_internal;
  assign {carry_out_internal, sum_internal} = A + B;
  assign carry_out = (sum_internal > 9);
  always @(sum_internal) begin
    if (carry_out_internal)
      sum = sum_internal + 6;
    else
      sum = sum_internal;
  end
endmodule
```

Test Bench:

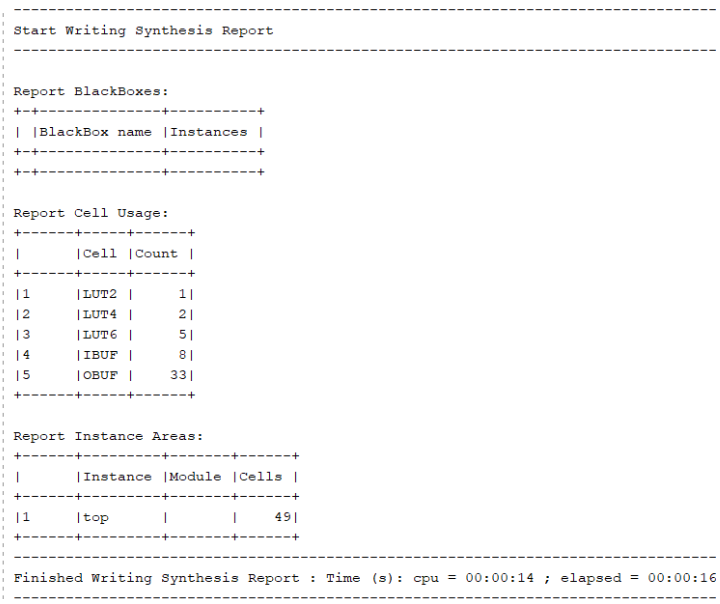


```
module BCDAdder_TB;
  reg [3:0] A;
  reg [3:0] B;
  wire [3:0] sum;
  wire carry_out;
  bcd_adder uut (
    .A(A),
    .B(B),
    .sum(sum),
    .carry_out(carry_out)
  );
  initial begin
    $display("BCD Adder Testbench");
    A = 4'b0101;
    B = 4'b0011;
    #10;
        $display("A = %d, B = %d, Sum = %d, Carry Out = %b", A, B, sum, carry_out);
    A = 4'b1001;
    B = 4'b1001;
    #10;
        $display("A = %d, B = %d, Sum = %d, Carry Out = %b", A, B, sum, carry_out);
    $finish;
  end
endmodule
```

RTL Schematic:

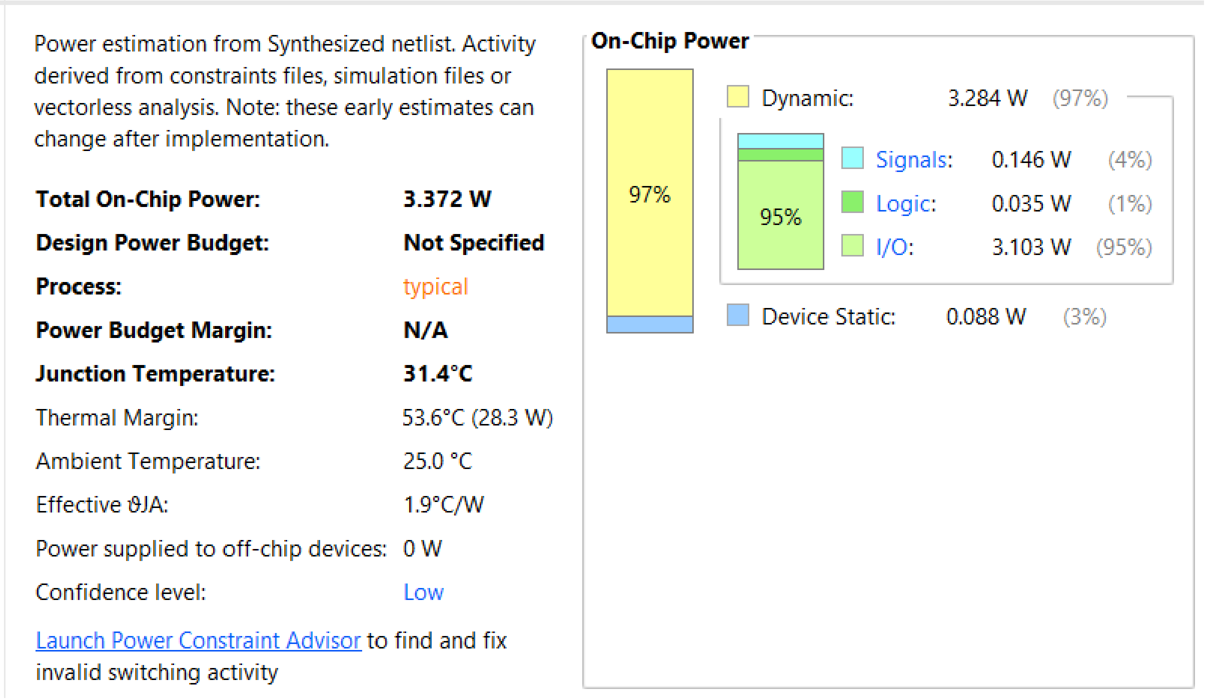


Synthesis Report;



```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT2 |     1|
|2     |LUT4 |     2|
|3     |LUT6 |     5|
|4     |IBUF |     8|
|5     |OBUF |    33|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    49|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:14 ; elapsed = 00:00:16
---------------------------------------------------------------------------------
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**3.372 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**31.4°C**
Thermal Margin:	53.6°C (28.3 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

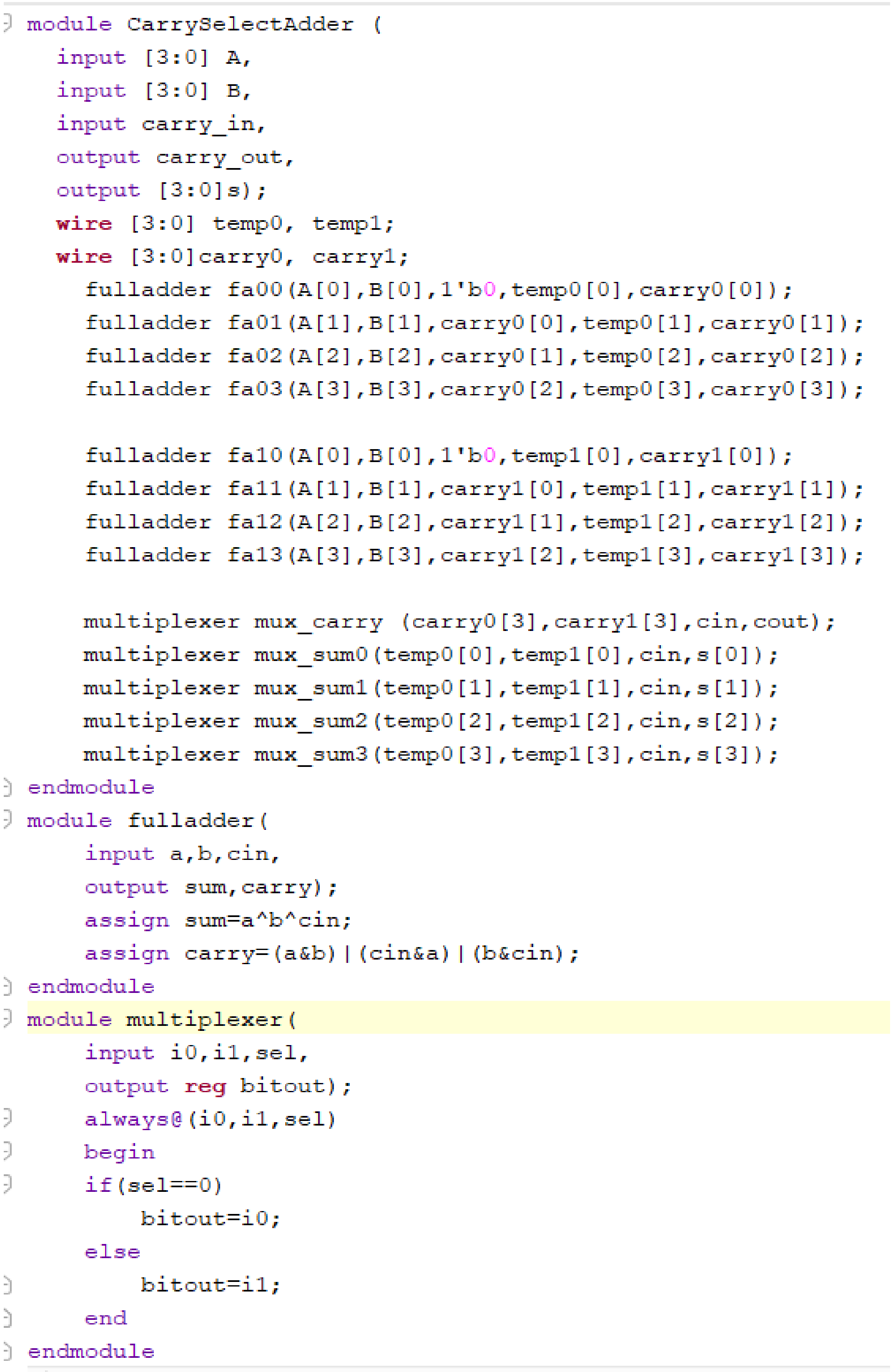
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨 Dynamic:	3.284 W	(97%)
🟦 Signals:	0.146 W	(4%)
🟩 Logic:	0.035 W	(1%)
🟩 I/O:	3.103 W	(95%)
🟦 Device Static:	0.088 W	(3%)

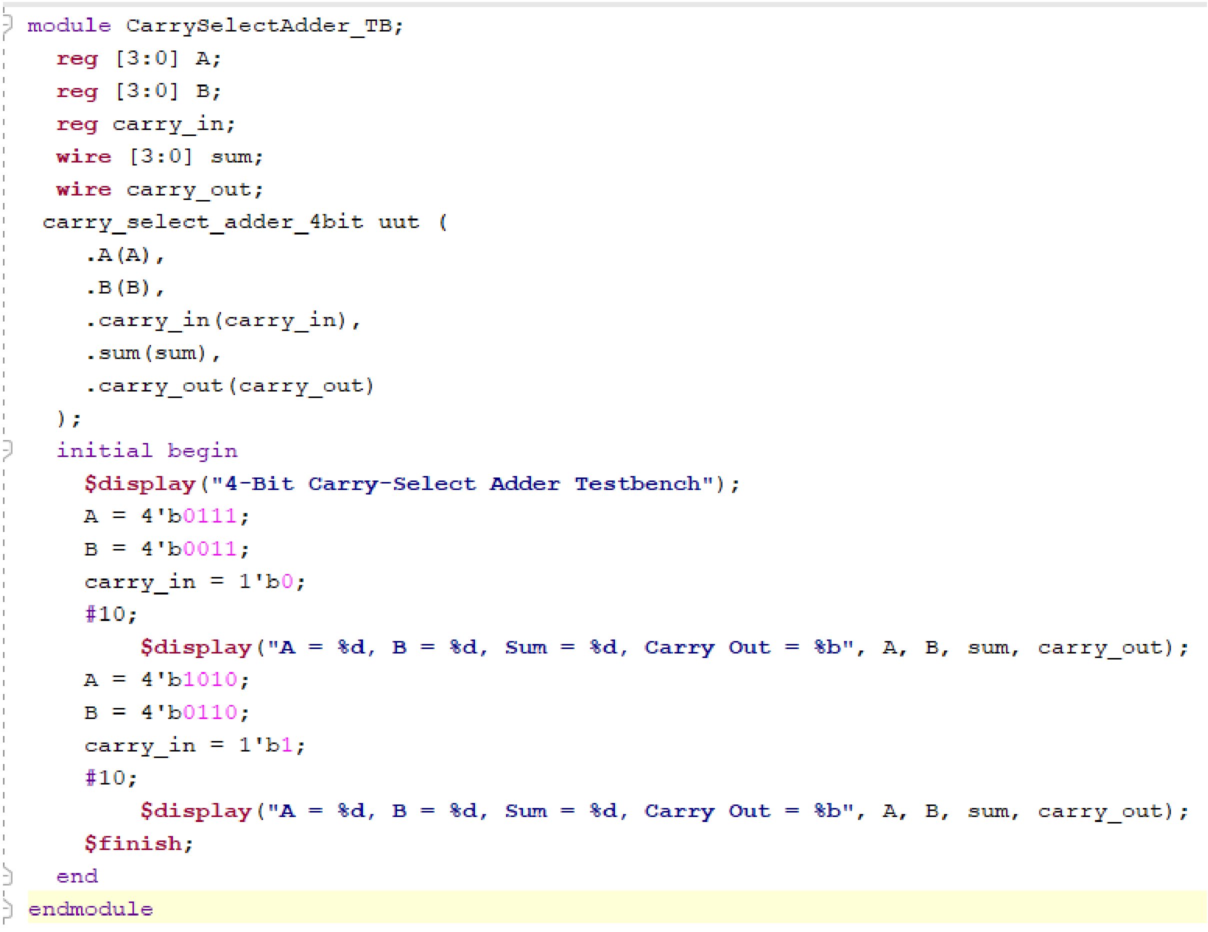
23. 4-Bit Carry Select Adder :-

Verilog Code:



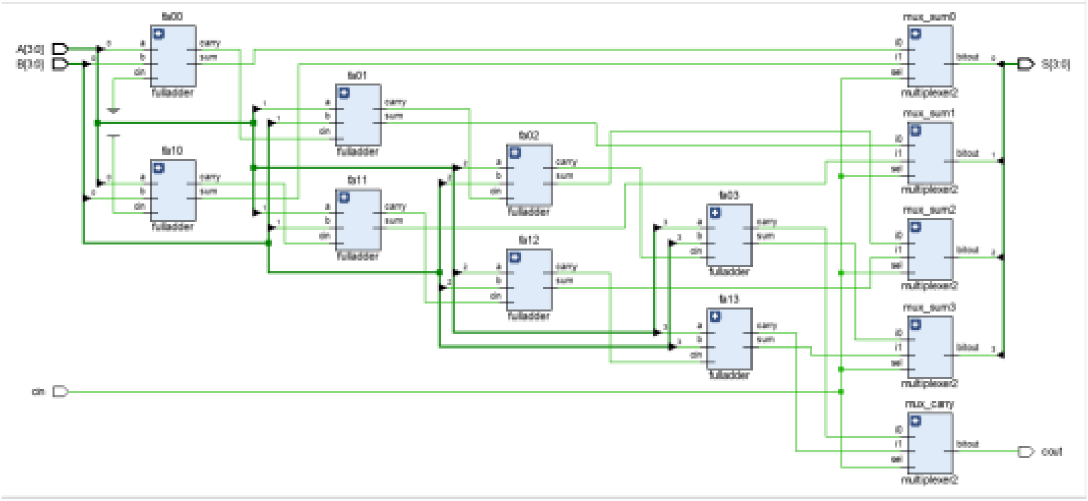
```
module CarrySelectAdder (
   input [3:0] A,
   input [3:0] B,
   input carry_in,
   output carry_out,
   output [3:0]s);
   wire [3:0] temp0, temp1;
   wire [3:0]carry0, carry1;
     fulladder fa00(A[0],B[0],1'b0,temp0[0],carry0[0]);
     fulladder fa01(A[1],B[1],carry0[0],temp0[1],carry0[1]);
     fulladder fa02(A[2],B[2],carry0[1],temp0[2],carry0[2]);
     fulladder fa03(A[3],B[3],carry0[2],temp0[3],carry0[3]);

     fulladder fa10(A[0],B[0],1'b0,temp1[0],carry1[0]);
     fulladder fa11(A[1],B[1],carry1[0],temp1[1],carry1[1]);
     fulladder fa12(A[2],B[2],carry1[1],temp1[2],carry1[2]);
     fulladder fa13(A[3],B[3],carry1[2],temp1[3],carry1[3]);

     multiplexer mux_carry (carry0[3],carry1[3],cin,cout);
     multiplexer mux_sum0(temp0[0],temp1[0],cin,s[0]);
     multiplexer mux_sum1(temp0[1],temp1[1],cin,s[1]);
     multiplexer mux_sum2(temp0[2],temp1[2],cin,s[2]);
     multiplexer mux_sum3(temp0[3],temp1[3],cin,s[3]);
endmodule
module fulladder(
     input a,b,cin,
     output sum,carry);
     assign sum=a^b^cin;
     assign carry=(a&b)|(cin&a)|(b&cin);
endmodule
module multiplexer(
     input i0,i1,sel,
     output reg bitout);
     always@(i0,i1,sel)
     begin
     if(sel==0)
         bitout=i0;
     else
         bitout=i1;
     end
endmodule
```

Test Bench:



```
module CarrySelectAdder_TB;
  reg [3:0] A;
  reg [3:0] B;
  reg carry_in;
  wire [3:0] sum;
  wire carry_out;
 carry_select_adder_4bit uut (
    .A(A),
    .B(B),
    .carry_in(carry_in),
    .sum(sum),
    .carry_out(carry_out)
  );
  initial begin
    $display("4-Bit Carry-Select Adder Testbench");
    A = 4'b0111;
    B = 4'b0011;
    carry_in = 1'b0;
    #10;
        $display("A = %d, B = %d, Sum = %d, Carry Out = %b", A, B, sum, carry_out);
    A = 4'b1010;
    B = 4'b0110;
    carry_in = 1'b1;
    #10;
        $display("A = %d, B = %d, Sum = %d, Carry Out = %b", A, B, sum, carry_out);
    $finish;
  end
endmodule
```

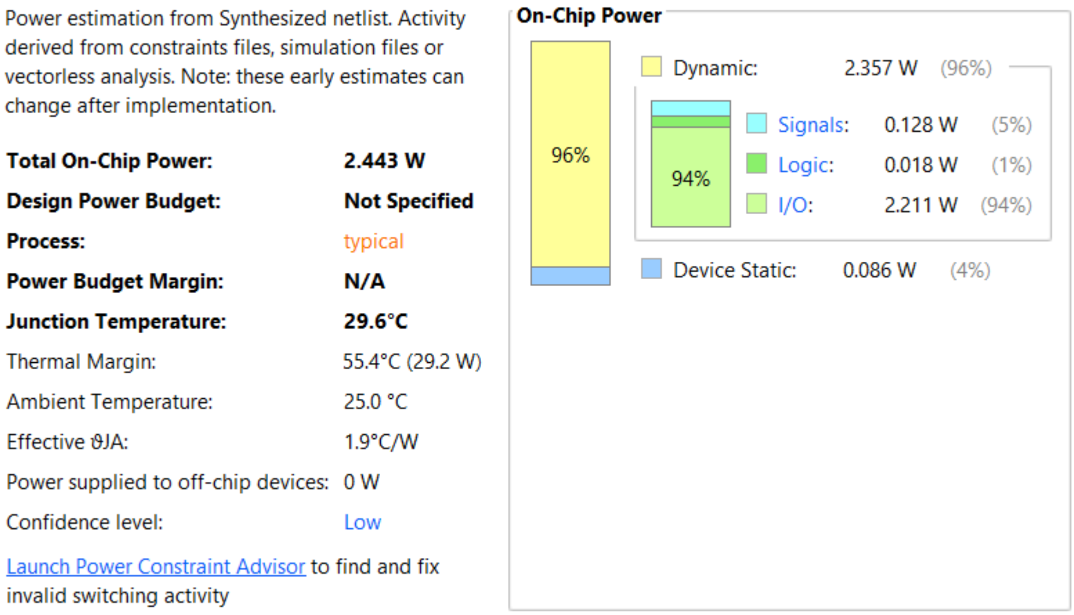
RTL Schematic:



Synthesis Report:

```
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+------+------+
|      |Cell  |Count |
+------+------+------+
|1     |LUT2  |     1|
|2     |LUT4  |     2|
|3     |LUT5  |     1|
|4     |LUT6  |     1|
|5     |IBUF  |     8|
|6     |OBUF  |     4|
|7     |OBUFT |     1|
+------+------+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    18|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:13 ; elapsed = 00:00:20
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**2.443 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**29.6°C**
Thermal Margin:	55.4°C (29.2 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

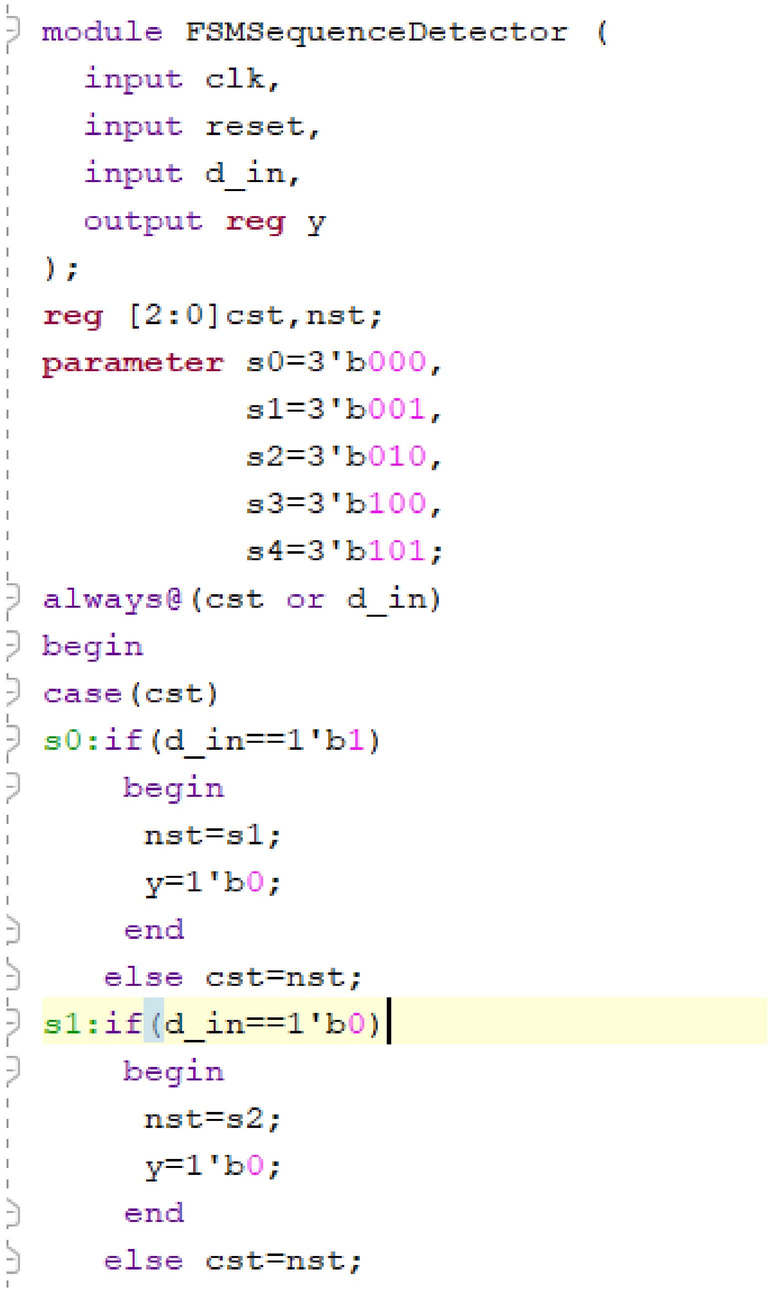
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

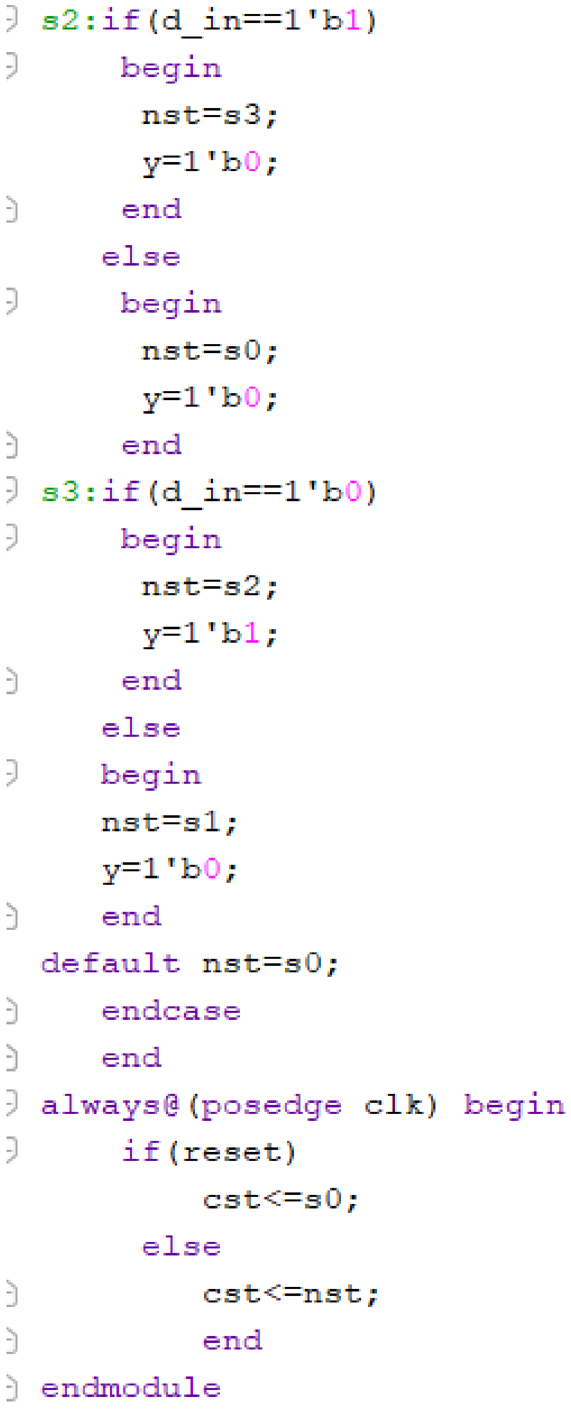
Dynamic:	2.357 W	(96%)
Signals:	0.128 W	(5%)
Logic:	0.018 W	(1%)
I/O:	2.211 W	(94%)
Device Static:	0.086 W	(4%)

24. Moore FSM 1010 Sequence Detector :-

Verilog Code:

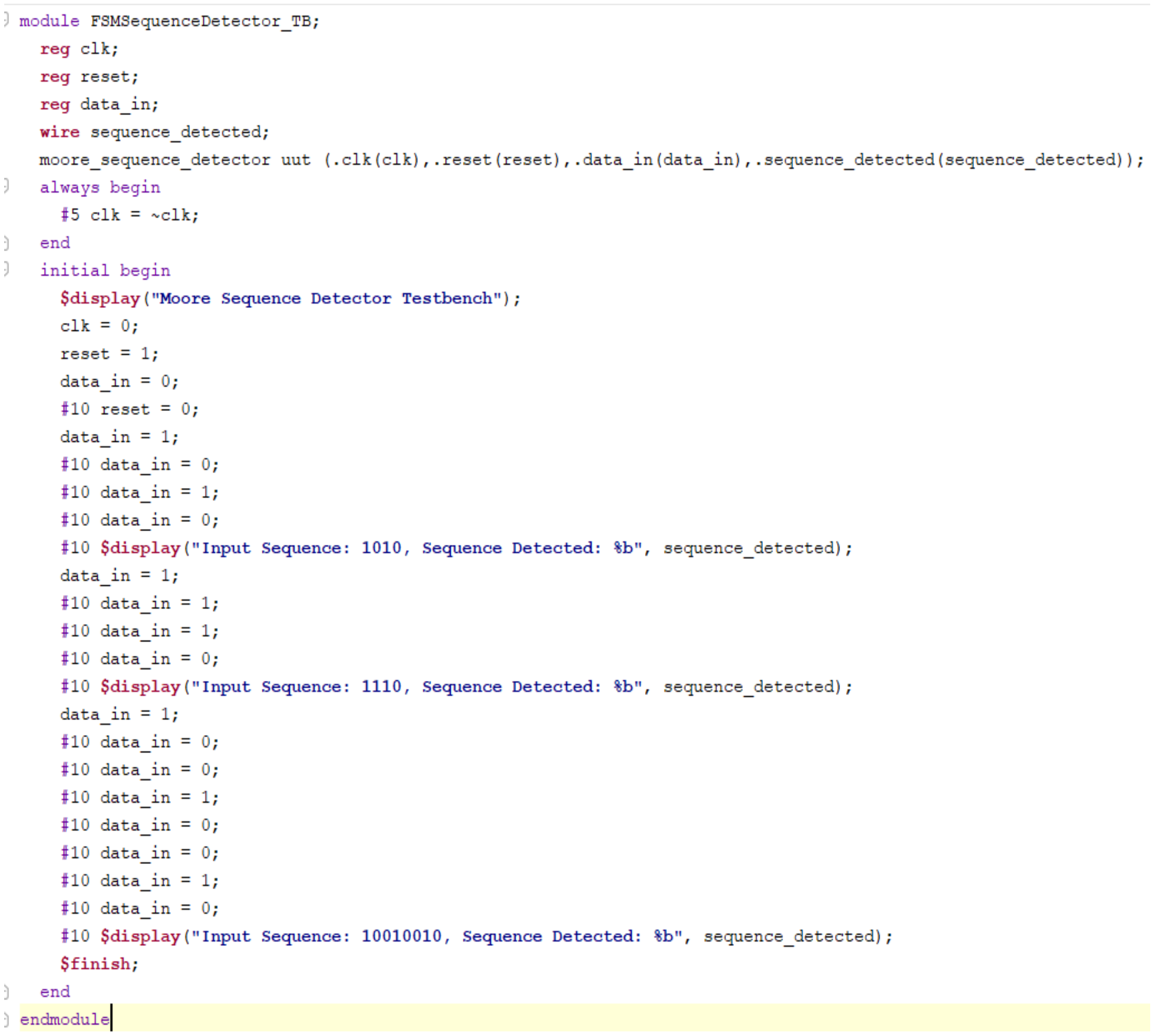


```
module FSMSequenceDetector (
  input clk,
  input reset,
  input d_in,
  output reg y
);
reg [2:0]cst,nst;
parameter s0=3'b000,
          s1=3'b001,
          s2=3'b010,
          s3=3'b100,
          s4=3'b101;
always@(cst or d_in)
begin
case(cst)
s0:if(d_in==1'b1)
    begin
     nst=s1;
     y=1'b0;
    end
   else cst=nst;
s1:if(d_in==1'b0)
    begin
     nst=s2;
     y=1'b0;
    end
   else cst=nst;
```



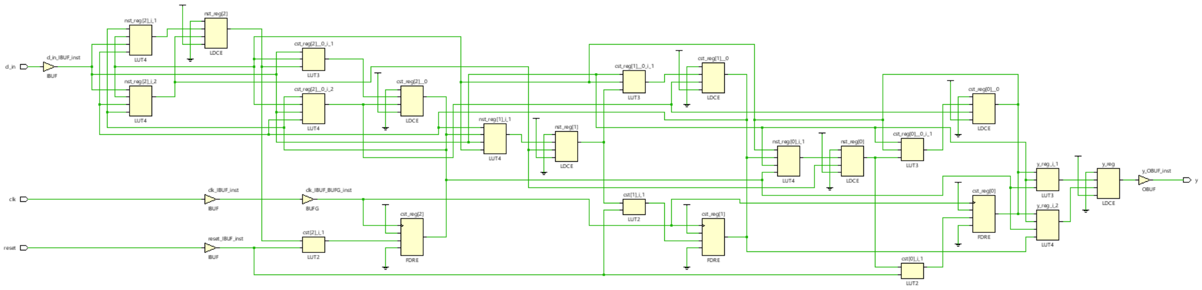
```
s2:if(d_in==1'b1)
    begin
     nst=s3;
     y=1'b0;
    end
   else
    begin
     nst=s0;
     y=1'b0;
    end
s3:if(d_in==1'b0)
    begin
     nst=s2;
     y=1'b1;
    end
   else
   begin
   nst=s1;
   y=1'b0;
   end
default nst=s0;
   endcase
   end
always@(posedge clk) begin
    if(reset)
        cst<=s0;
     else
        cst<=nst;
        end
endmodule
```

Test Bench:

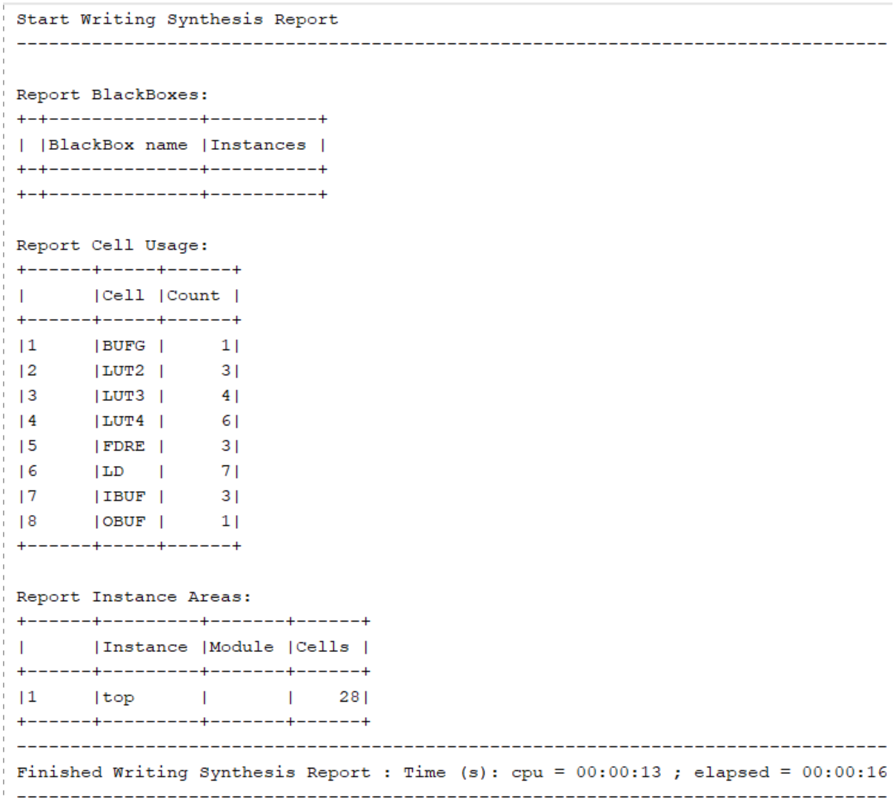


```verilog
module FSMSequenceDetector_TB;
  reg clk;
  reg reset;
  reg data_in;
  wire sequence_detected;
  moore_sequence_detector uut (.clk(clk),.reset(reset),.data_in(data_in),.sequence_detected(sequence_detected));
  always begin
    #5 clk = ~clk;
  end
  initial begin
    $display("Moore Sequence Detector Testbench");
    clk = 0;
    reset = 1;
    data_in = 0;
    #10 reset = 0;
    data_in = 1;
    #10 data_in = 0;
    #10 data_in = 1;
    #10 data_in = 0;
    #10 $display("Input Sequence: 1010, Sequence Detected: %b", sequence_detected);
    data_in = 1;
    #10 data_in = 1;
    #10 data_in = 1;
    #10 data_in = 0;
    #10 $display("Input Sequence: 1110, Sequence Detected: %b", sequence_detected);
    data_in = 1;
    #10 data_in = 0;
    #10 data_in = 0;
    #10 data_in = 1;
    #10 data_in = 0;
    #10 data_in = 0;
    #10 data_in = 1;
    #10 data_in = 0;
    #10 $display("Input Sequence: 10010010, Sequence Detected: %b", sequence_detected);
    $finish;
  end
endmodule
```

RTL Schematic:

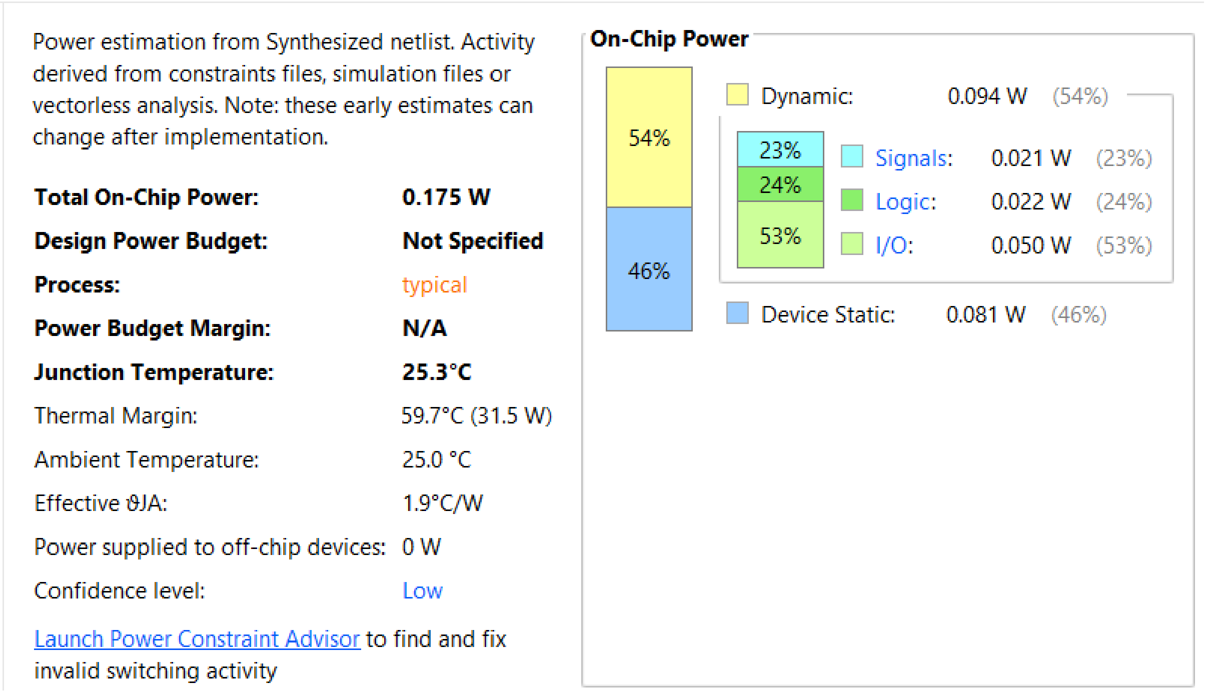


Synthesis Report:



```
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |BUFG |     1|
|2     |LUT2 |     3|
|3     |LUT3 |     4|
|4     |LUT4 |     6|
|5     |FDRE |     3|
|6     |LD   |     7|
|7     |IBUF |     3|
|8     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    28|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:13 ; elapsed = 00:00:16
---------------------------------------------------------------------------------
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.175 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.3°C**
Thermal Margin:	59.7°C (31.5 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

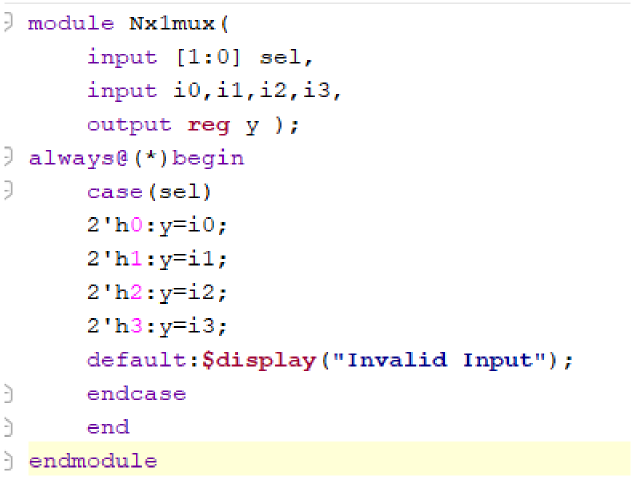
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	0.094 W	(54%)
Signals:	0.021 W	(23%)
Logic:	0.022 W	(24%)
I/O:	0.050 W	(53%)
Device Static:	0.081 W	(46%)

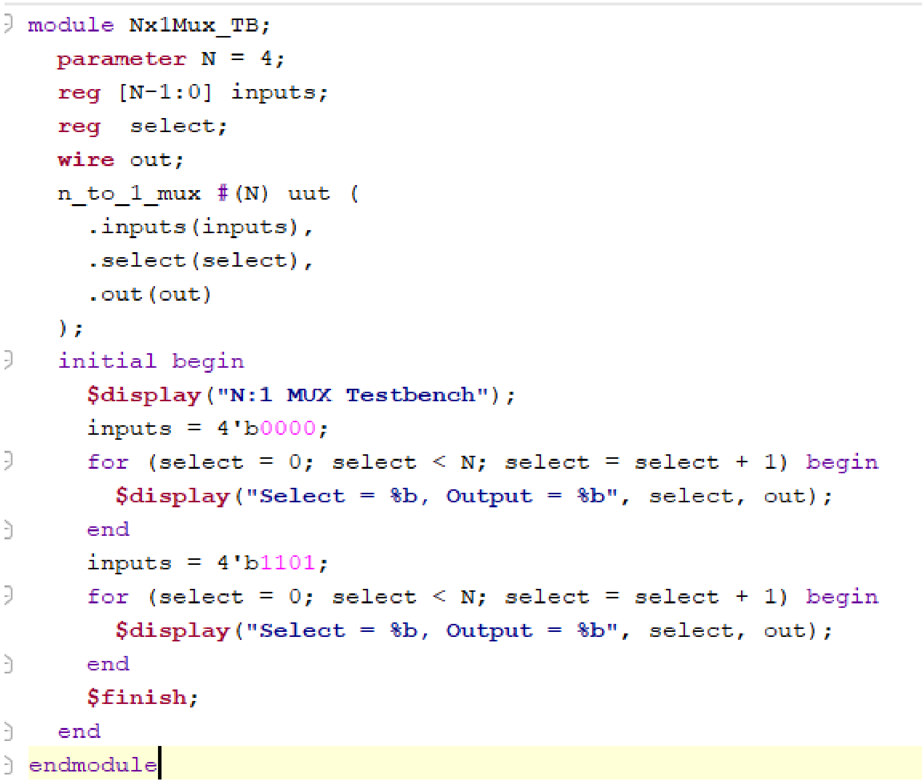
25. N:1 Mux :-

Verilog Code:



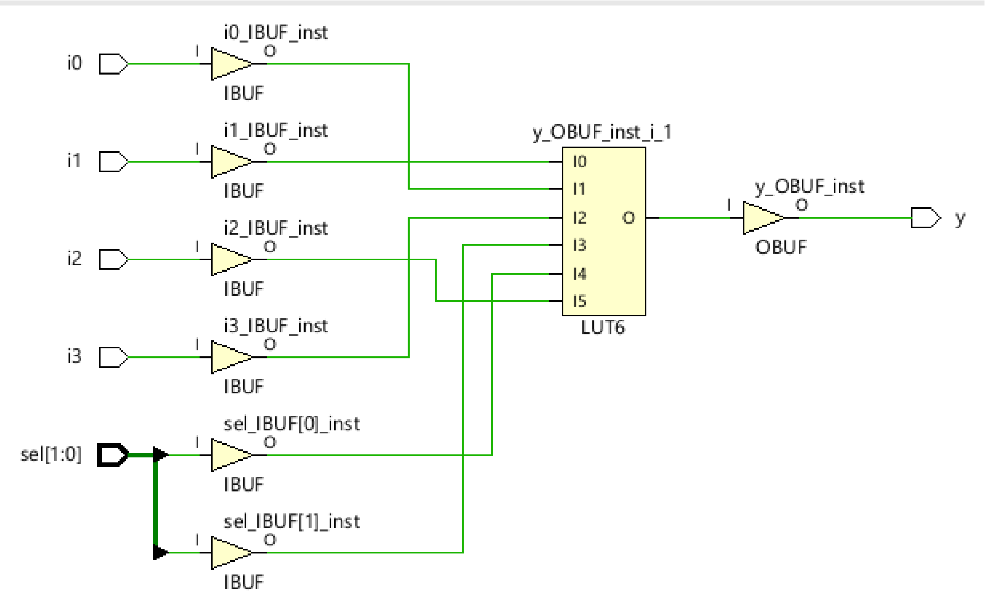
```
module Nx1mux(
    input [1:0] sel,
    input i0,i1,i2,i3,
    output reg y );
always@(*)begin
    case(sel)
    2'h0:y=i0;
    2'h1:y=i1;
    2'h2:y=i2;
    2'h3:y=i3;
    default:$display("Invalid Input");
    endcase
    end
endmodule
```

Test Bench:



```
module Nx1Mux_TB;
  parameter N = 4;
  reg [N-1:0] inputs;
  reg  select;
  wire out;
  n_to_1_mux #(N) uut (
    .inputs(inputs),
    .select(select),
    .out(out)
  );
  initial begin
    $display("N:1 MUX Testbench");
    inputs = 4'b0000;
    for (select = 0; select < N; select = select + 1) begin
      $display("Select = %b, Output = %b", select, out);
    end
    inputs = 4'b1101;
    for (select = 0; select < N; select = select + 1) begin
      $display("Select = %b, Output = %b", select, out);
    end
    $finish;
  end
endmodule
```

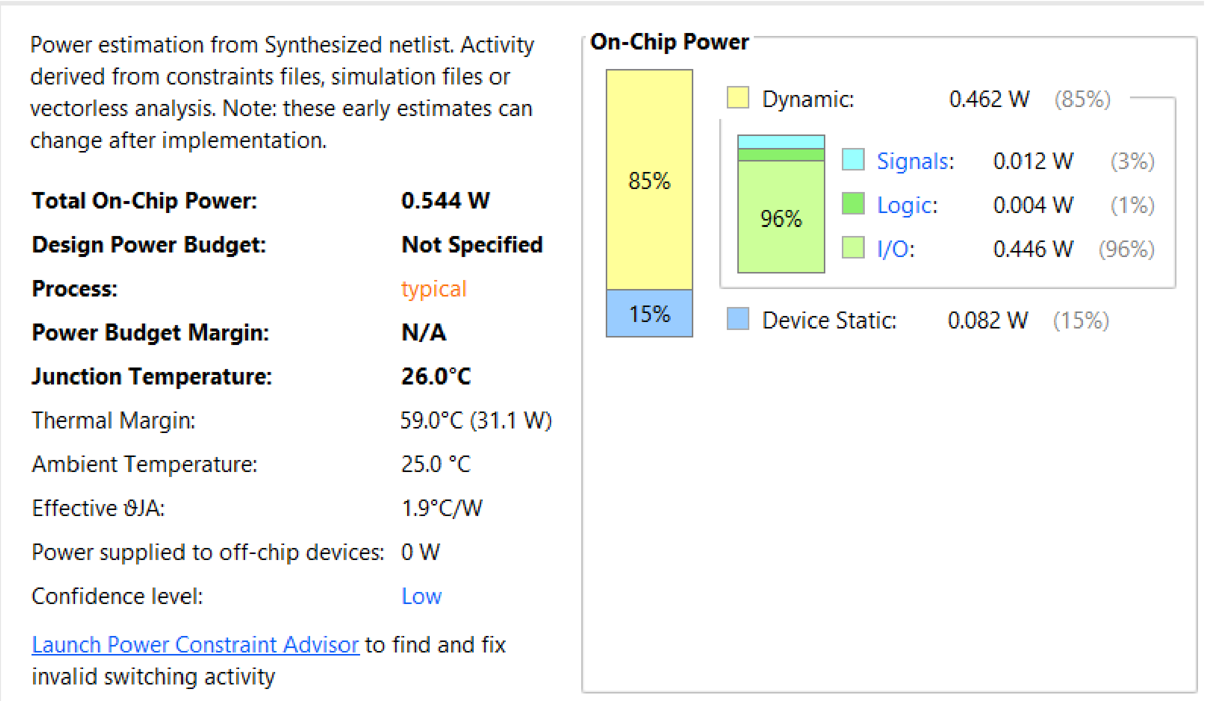
RTL Schematic:



Synthesis Report:

```
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-----+------+
|      |Cell |Count |
+------+-----+------+
|1     |LUT6 |     1|
|2     |IBUF |     6|
|3     |OBUF |     1|
+------+-----+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |     8|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:13 ; elapsed = 00:00:16
```

Power Report:



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.544 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**26.0°C**
Thermal Margin:	59.0°C (31.1 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

🟨 Dynamic:	0.462 W	(85%)
🟦 Signals:	0.012 W	(3%)
🟩 Logic:	0.004 W	(1%)
🟩 I/O:	0.446 W	(96%)
🟦 Device Static:	0.082 W	(15%)