Edited by Foxit Reader Introduction @cynchight(@edynchicalcoloried) iterative @ellore@010 For Evaluation Only.

than for other possible realizations, however. When realizing combinational circuits, for which the speed of operation is not crucial and which can be composed of identical cells, iterative networks prove to be very useful and economical.

Notes and references

The finite-state model described in this chapter was proposed by Mealy [7] in 1955, on the basis of earlier models by Huffman [3] and Moore [8]. The applicability of the model to iterative combinational circuits was pointed out by McCluskey [6]. Recently, there have been several texts devoted to finite-state machines, among which are Hill and Peterson [2], Katz [4], Mano and Ciletti [5], and Wakerly [10]. A collection of original basic papers dealing with various aspects of finite automata is available in a book edited by Moore [9]. A comprehensive presentation of iterative networks is available in Hennie [1].

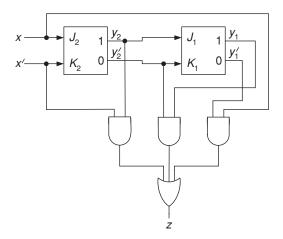
- [1] Hennie, F. C.: *Iterative Arrays of Logical Circuits*, MIT Press, Cambridge MA, 1961.
- [2] Hill, F. J., and G. R. Peterson: *Computer Aided Logical Design With Emphasis on VLSI*, fourth edition, John Wiley & Sons, New York, 1993.
- [3] Huffman, D. A.: "The synthesis of sequential switching circuits," *J. Franklin Inst.*, vol. 257, pp. 161–190, March 1954; pp. 275–303, April 1954. Reprinted in Moore [9].
- [4] Katz, R. H., and G. Borriello: *Contemporary Logic Design*, second edition, Pearson Prentice Hall, Upper Saddle River NJ, 2005.
- [5] Mano, M. M., and M. D. Ciletti: *Digital Design*, fourth edition, Prentice Hall, Upper Saddle River, NJ, 2007.
- [6] McCluskey, E. J.: "Iterative combinational switching networks: general design considerations," *IRE Trans. Electron. Computers*, vol. EC-7, pp. 285–291, December 1958.
- [7] Mealy, G. H.: "A method for synthesizing sequential circuits," *Bell System Tech. J.*, vol. 34, pp. 1045–1079, September 1955.
- [8] Moore, E. F.: Gedanken-experiments on sequential machines, pp. 129–153, *Automata Studies*, Princeton University Press, 1956.
- [9] Moore, E. F. (ed.): Sequential Machines: Selected Papers, Addison Wesley, Reading, Mass., 1964.
- [10] Wakerly, J. F.: Digital Design Principles and Practices, Prentice Hall, Englewood Cliffs NJ, 1990.

Problems

Problem 9.1. Analyze the synchronous circuit of Fig. P9.1 (the clock is not shown, but is implicit).

- (a) Write down the excitation and output functions.
- (b) Form the excitation and state tables.
- (c) Give a word description of the circuit operation.

Fig. P9.1



Problem 9.2. A long input sequence enters a one-input one-output synchronous sequential circuit, that is required to produce an output symbol z=1 whenever the sequence 1111 occurs. Overlapping sequences are accepted; for example, if the input sequence is $010111111\cdots$, the required output sequence is $00000011\cdots$.

- (a) Draw a state diagram.
- (b) Select an assignment and show the excitation and output tables.
- (c) Write down the excitation functions for SR flip-flops, and draw the corresponding logic diagram.

Problem 9.3. Repeat Problem 9.2 for the sequence 01101, and implement the circuit with T flip-flops as memory elements.

Problem 9.4. Construct the state diagram for a one-input eight-state machine that is to produce an output symbol z=1 whenever the last string of five input symbols contains exactly three 1's and starts with two 1's. After each string that starts with two 1's, analysis of the next string does not start until the end of this string of five symbols, whether it produces an output value 1 or not. For example, if the input sequence is 11011010 then the output sequence is 000000000, while an input sequence 10011010 produces an output sequence 000000001.

Problem 9.5. For each of the following cases, show the state table that describes a one-input one-output machine having the following specifications.

- (a) An output symbol z = 1 is to be produced to coincide with every occurrence of the input symbol 1 following a string of two or three consecutive 0's at the input. At all other times, the output symbol is to be 0.
- (b) Regardless of the input symbols, the first two output symbols are 0's. Thereafter, output symbol z is a replica of input symbol x but delayed by two time units, that is, z(t) = x(t-2) for $t \ge 3$.
- (c) The output z(t) is 1 if and only if x(t) = x(t-2). At all other times, z is to be 0.

(d) The output z has the value 1 whenever the last four input symbols correspond to a BCD number that is a multiple of 3, i.e., 0, 3, 6,

Problem 9.6. Design a one-input one-output synchronous sequential circuit that produces an output symbol z=1 whenever any of the following input sequences occurs: 1100, 1010, or 1001. The circuit resets to its initial state after an output symbol 1 has been generated.

- (a) Form the state diagram or table. (Seven states are sufficient.)
- (b) Choose an assignment, and show the excitation functions for JK flip-flops.

Problem 9.7. Design a one-input one-output synchronous sequential circuit that examines the input sequence in nonoverlapping strings having three input symbols each and produces an output symbol 1 that is coincident with the last input symbol of the string if and only if the string consisted of either two or three 1's. For example, if the input sequence is 010101110, the required output sequence is 000001001. Use *SR* flip-flops in your realization.

Problem 9.8. Design a modulo-8 counter that counts in the way specified in Table P9.8. Use JK flip-flops in your realization.

Table P9.8

Decimal	Gr	Gray code				
0	0	0	0			
1	0	0	1			
2	0	1	1			
3	0	1	0			
4	1	1	0			
5	1	1	1			
6	1	0	1			
7	1	0	0			

Problem 9.9. Construct the state diagram for a synchronous sequential machine that can be used to detect faults in coded messages of the 2-out-of-5 type. That is, the machine examines the messages serially and produces an output symbol 1 whenever an illegal message of five binary digits is detected.

Problem 9.10. When a certain serial binary communication channel is operating correctly, all blocks of 0's are of even length and all blocks of 1's are of odd length. Show the state diagram or table of a machine that will produce an output symbol z=1 whenever a discrepancy from the above pattern is detected. The following is an example.

X:	0	0	1	0	0	0	1	1	1	0	1	1	0	0	
Z:	0	0	0	0	0	0	1	0	0	0	1	0	1	0	

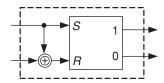
Problem 9.11. A new kind of flip-flop has been designed. It is equivalent to an *SR* flip-flop with gated inputs, as shown in Fig. P9.11.

A synchronous sequential circuit that generates an output symbol z=1 whenever the string 0101 is scanned in the input sequence is to be designed. Overlapping strings

are accepted; for example, corresponding to the input sequence 0010101, the required output sequence is 0000101.

- (a) Construct the state diagram and table for the circuit, using the letters A, B, C, etc.
- (b) Make a state assignment (use a Gray code, starting with an all-0 assignment for the initial state).
- (c) Realize the sequential circuit using the new flip-flops as memory elements. Give the logic equations for the memory elements and the output.

Fig. P9.11



Problem 9.12. The clocked memory device shown in Fig. P9.12 has one binary input Y and one binary output y. If Y(t) = 0 then y(t+1) = 0; if Y(t) = 1 then y(t+1) = y'(t).

- (a) The state table given in Table P9.12 is to be realized using two such memory devices. Choose an appropriate state assignment and give the corresponding excitation and output equations.
- (b) Briefly discuss the possibility and practicality of using such memory devices to realize an arbitrary state table.

Fig. P9.12

	N.S.	S, z			
PS	x = 0	x = 1			
\overline{A}	B, 0	B, 0			
$\frac{B}{C}$	C, 0 B, 0	A, 1 D, 0			
D	C, 0	<i>B</i> , 1			

Table P9.12

Problem 9.13. Write the state table for a synchronous circuit, with one input x and one output z, that operates according to the following specifications. At time t = 0, the initial state is A, and x(t) = 0 for t < 0. The output function is given by either (a) or (b) as follows:

- (a) z(t) = x(t) + x(t-1),
- (b) $z(t) = x(t) \cdot x(t-1)$

where the change from (a) to (b) occurs at times τ such that

$$x(\tau) = x(\tau - 1) = x(\tau - 2) = 1$$

and the change from (b) to (a) occurs at times T such that

$$x(T) = x(T-1) = x(T-2) = 0.$$

An example is shown in Fig. P9.13.

Problem 9.14. The synchronous circuit shown in Fig. P9.14, where D denotes a unit delay, produces a periodic binary output sequence. Assume that initially $x_1 = 1$, $x_2 = 1$, $x_3 = 0$, $x_4 = 0$ and that the initial output sequence is 1100101000. Thereafter, this sequence repeats itself. Find a minimal expression for the combinational circuit $f(x_1, x_2, x_3, x_4)$.

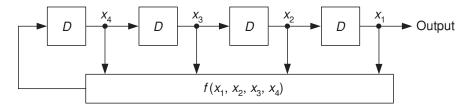


Fig. P9.14

Problem 9.15. A synchronous machine N is part of a transmitter and is used to encode binary serial messages. The coded messages are then transmitted to a receiver, as shown in Fig. P9.15. The receiver contains a synchronous machine M that is used to decode the received messages.

- (a) Given that the initial state of N is A, find the state diagram of machine M.
- (b) Suppose the initial state of N is unknown and machine M received a 10-bit message; which of the 10 bits can be uniquely decoded without an error? Explain.

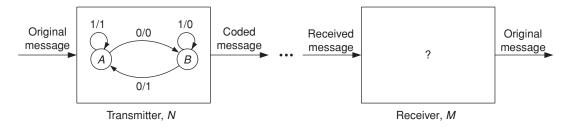


Fig. P9.15

Problem 9.16. A *palindrome* is a sequence which reads the same backward as forward, e.g., 11011 or 01010. Show the finite-state control of a Turing machine that is capable of detecting arbitrarily long palindromes. Assume that you are given a tape initially marked only with symbols #, 0, 1, where the blanks (#) separate blocks of intermixed 0's and 1's. The machine will be started on a # and then checks whether the sequence to its right is a palindrome. If not, the machine should proceed to the next block. If the sequence is a palindrome, the machine should stop at the # to the right of the block. An example is shown in Fig. P9.16.



Fig. P9.16

Hint: It is often useful in the course of computation to mark certain digits. This can be accomplished by replacing those digits with different symbols; for example, 0's may be replaced by 2's, while 1's may be replaced by 3's, etc. When these markers are no longer necessary, they are replaced with the old symbols. Use as many new symbols as necessary.

Problem 9.17. Assume that you have a Turing machine that is started at the leftmost 1 in a block of n 1's on a tape that otherwise contains only #'s (blanks), as shown in Fig. P9.17. Using as many symbols as you like:

- (a) Show a finite-state control that will duplicate the block of 1's immediately to the right of the original block, leaving the original block and the rest of the tape intact when the machine stops (viz., the block is simply doubled in size it now contains 2*n* 1's). The machine should stop at the leftmost 1.
- (b) Show a finite-state control that will produce a number of replicas equal to the original number of 1's (it stops with a block of n^2 1's).
- (c) Show a finite-state control that will increase the number of 1's to 2^n and will then stop.

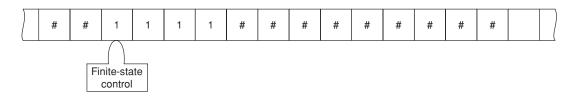


Fig. P9.17

Problem 9.18. An iterative network to be used for detecting faults in Ringtail-coded messages is to be designed. The network consists of five cells, each receiving a digit of the coded message, and is to produce an output symbol 1 when and only when an illegal message is detected. (The Ringtail code is defined in Problem 5.2.)

- (a) Construct a cell table.
- (b) Select an assignment and derive the logic equations for the output carries and the cell output.
- (c) Construct a typical cell using AND, OR, and NOT gates.

Problem 9.19. The cell output of a typical cell of an iterative network has the value 1 if and only if the input pattern of the preceding cells consists of groups of 0's and 1's such that each group contains an odd number of members.

- (a) Construct a cell table.
- (b) Realize the typical cell using AND, OR, and NOT gates.

Problem 9.20. The typical cell of an iterative network has one binary input x_i and one binary output z_i . The output $z_i = 1$ if and only if $x_i \neq x_{i-2}$. For the first two cells (i.e., i = 1, 2), assume that $x_{-1} = x_0 = 0$.

- (a) Construct a cell table.
- (b) Make a Gray-code state assignment and give the output and carry functions.