SAMPLE SOLUTION

Indian Institute of Technology Kharagpur

Department of Computer Science and Engineering

Quiz-2, Autumn 2019-20

Computer Organization and Architecture (CS31007)

Students: 108 **Date:** 3-September-2019

Full marks: 25 **Time:** 75 minutes

Name	Roll No.

INSTRUCTIONS: This quiz is open book and open notes, but access to the internet via use of smartphones/portable computers is not allowed. Answer in the space provided only. Perform all rough work in blank sheets provided, your rough work will not be evaluated. Use of calculators is allowed. ANSWER ALL QUESTIONS.

1. Apply the *Booth multiplication algorithm* to multiply two numbers $X = -123$ and $Y = 117$ expressed as signed 2's complement binary numbers. Show all steps in detail. [8]

$X = -123 = (10000101)_2$, $Y = 117 = (01110101)_2 \Rightarrow -Y = (10001011)_{2\text{'s comp.}}$

Step No.	Action.	Accumulator (8 bit)	Q (9 bit)
0.	initialize	0000 0000	100001010
1.	A-Y	1000 1011	100001010
	R.S.	11000101	110000101
2.	A+Y	0011 1010	110000101
	R.S.	00011101	011000010
3.	A-Y	10101000	011000010
	R.S.	11010100	001100001
4.	A+Y	01001001	001100001
	R.S.	00100100	100110000
5.	R.S.	00010010	010011000
6.	R.S.	00001001	001001100
7.	R.S.	00000100	100100110
8.	A-Y	10001111	100100110
	R.S.	11000111	110010011

$\therefore$ Product $= (1100011111001001)_{2\text{'s comp.}} = -14391$

(a) Consider a magnetic hard disk with the following parameters: Average seek time 10 ms; Rotation rate 5400 RPM; Transfer rate 3.5 MB/second; number of sectors per track 60; Sector size 512 bytes; Controller overhead 6.0 ms. Calculate: (i) the average time to read a single sector, and, (ii) the average time to read 8 KB in 16 consecutive sectors in the same cylinder. [4]

i) Average time to read a single Sector = ~~rot. delay~~
= Seek time + rot. latency + transfer time + Controller overhead
$= 10\text{ms} + \frac{1/2}{(5400/60)} * 10^3\text{ms} + \frac{\frac{1}{2}\text{kB}}{(3.5\times1024)\text{kB}} * 10^3\text{ms} + 6.0\text{ms}$
$= 10\text{ms} + 5.56\text{ms} + 0.14\text{ms} + 6.0\text{ms} =$ **21.70 ms**

ii) Only the transfer time would be affected.
∴ time required = $(10 + 5.56 + 0.14*8 + 6)$ ms = **22.68 ms**

(b) Two (nk)-bit numbers $A = a_{nk}a_{nk-1}\ldots a_1$ and $B = b_{nk}b_{nk-1}\ldots b_1$ are being added using the following scheme. The bits are partitioned into n groups, each group consisting of k bits. For each group of k bits, an ideal carry lookahead adder (CLA), implemented as two-level AND-OR circuit, is employed to compute the sum. These (n of them) CLA adders are then serially cascaded as in ripple-carry adders. Estimate the hardware cost and delay of the proposed adder in terms of n and k. [4]

For each CLA block with "k" ~~adder~~ bit processing ability, delay is $O(1)$, cost is $O(k^3)$, assuming ideal CLAs.
∴ for whole adder, cost is $O(nk^3)$, delay is $O(n)$.

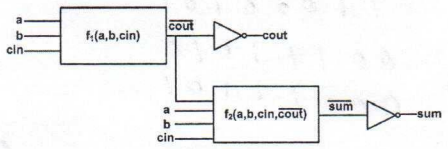

Figure 1: Adder without XOR.

2. Designer *XOR–HATER* hates XOR gates. Hence, he was faced with a challenge when he was asked to design a full–adder, as the *sum* bit is essentially an 3–input XOR function. He finally came up with the circuit shown in Figure–1 as the solution, which does not use any XOR gate. Determine the Boolean functions $f_1()$ and $f_2()$. [9]

K-map of cout:

ab \ cin	0	1
00	(0)	0
01	(0)	1
11	1	1
10	(0)	1

Grouping the 0's, $\overline{cout} = a'b' + b'c_{in}' + c_{in}'a' = f_1()$

Now, "Sum" of a full adder is basically the 3-bit odd parity detector.

$\therefore \overline{sum} = abc_{in} + ab'c_{in}' + a'bc_{in}' + a'b'c_{in}$

$= abc_{in} + b'c_{in}'(a+b+c_{in}) + c_{in}'a'(a+b+c_{in}) + a'b'(a+b+c_{in})$

$= abc_{in} + (a+b+c_{in})c_{out}' = f_2()$