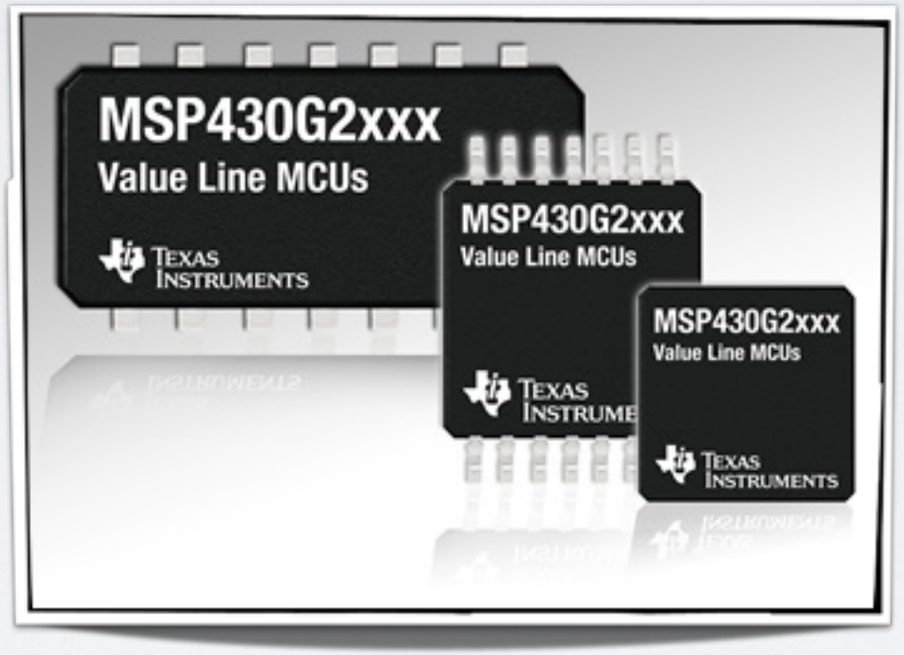
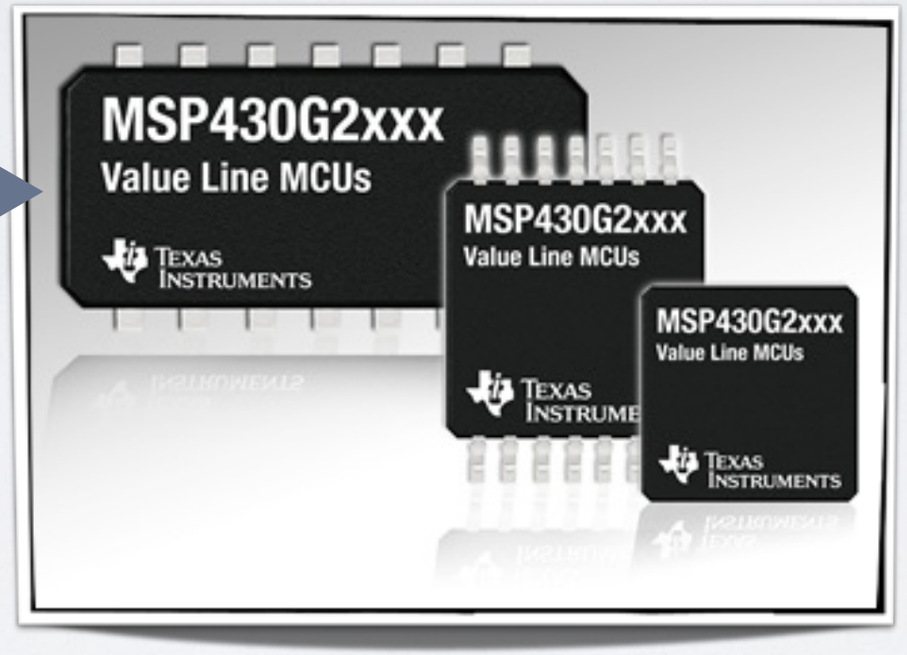
MICROPROCESSADORES E MICROCONTROLADORES

ENCAPSULAMENTOS



ENCAPSULAMENTOS

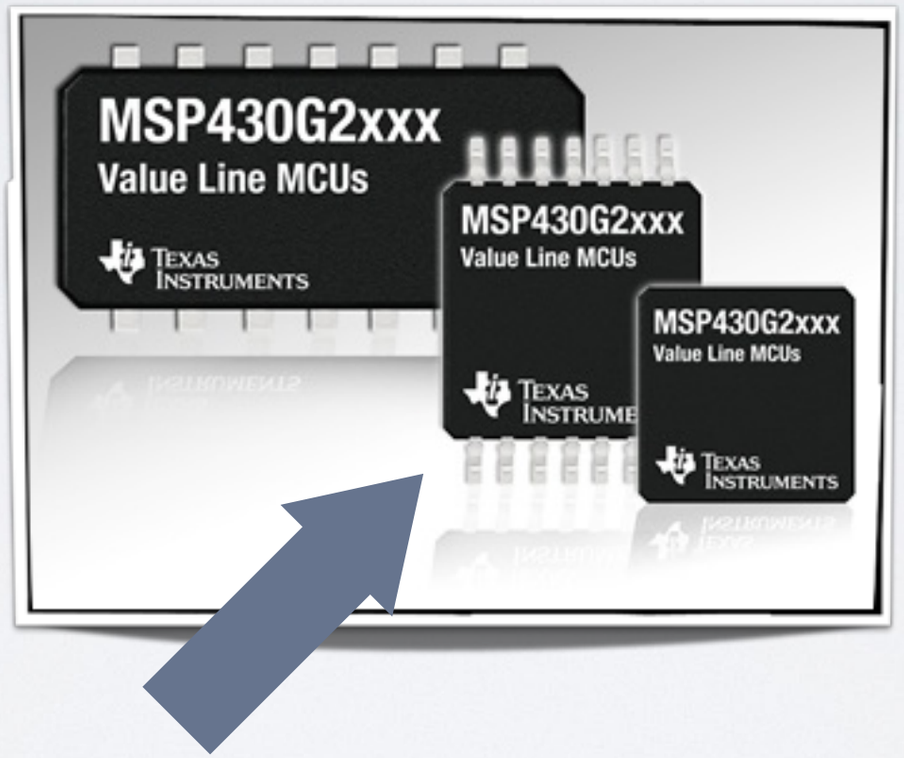
PDIP



2,54 mm (0,1")

entre pinos

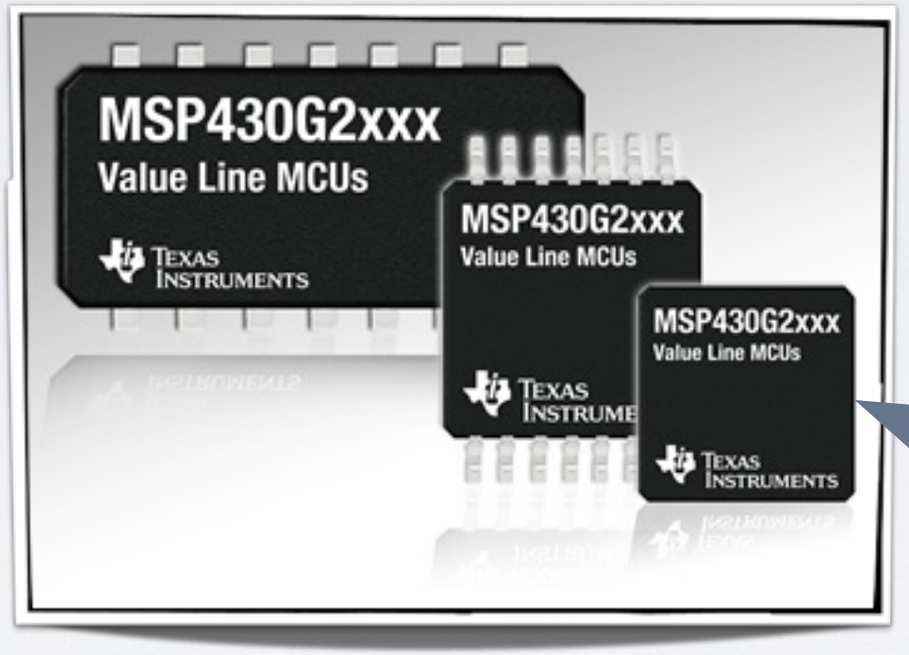
ENCAPSULAMENTOS



TSSOP

0,65 mm (0,025") entre pinos

ENCAPSULAMENTOS



QFN

Quadrado de 4mm

0,65 mm (0,025")
entre pinos

PINAGEM

PW or N PACKAGE
(TOP VIEW)

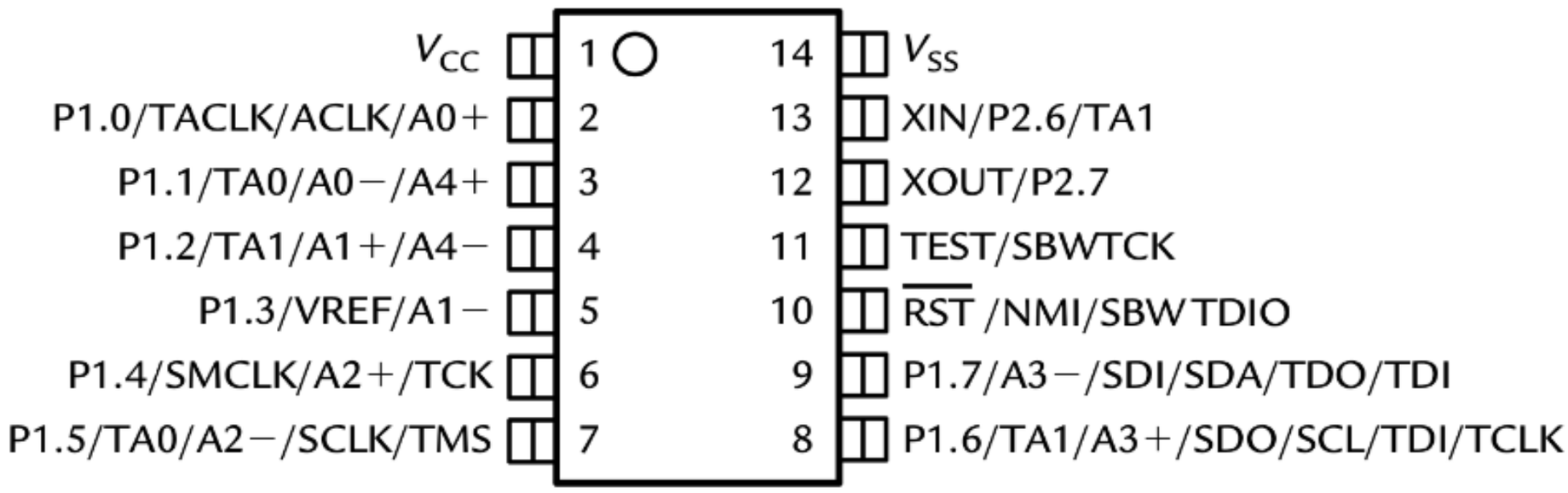
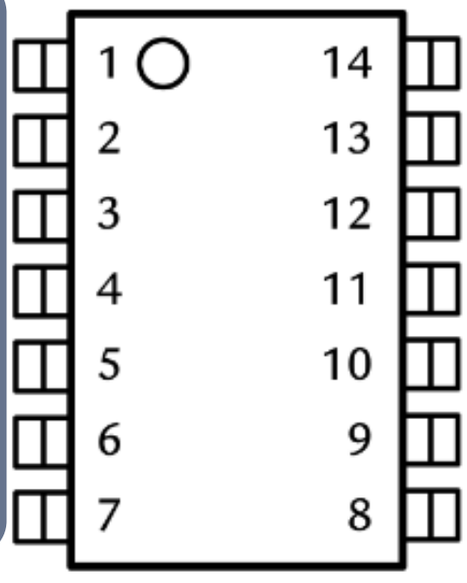


Figure 2.1: Pin-out of the MSP430F2003 and F2013, taken from the data sheet.

PINAGEM

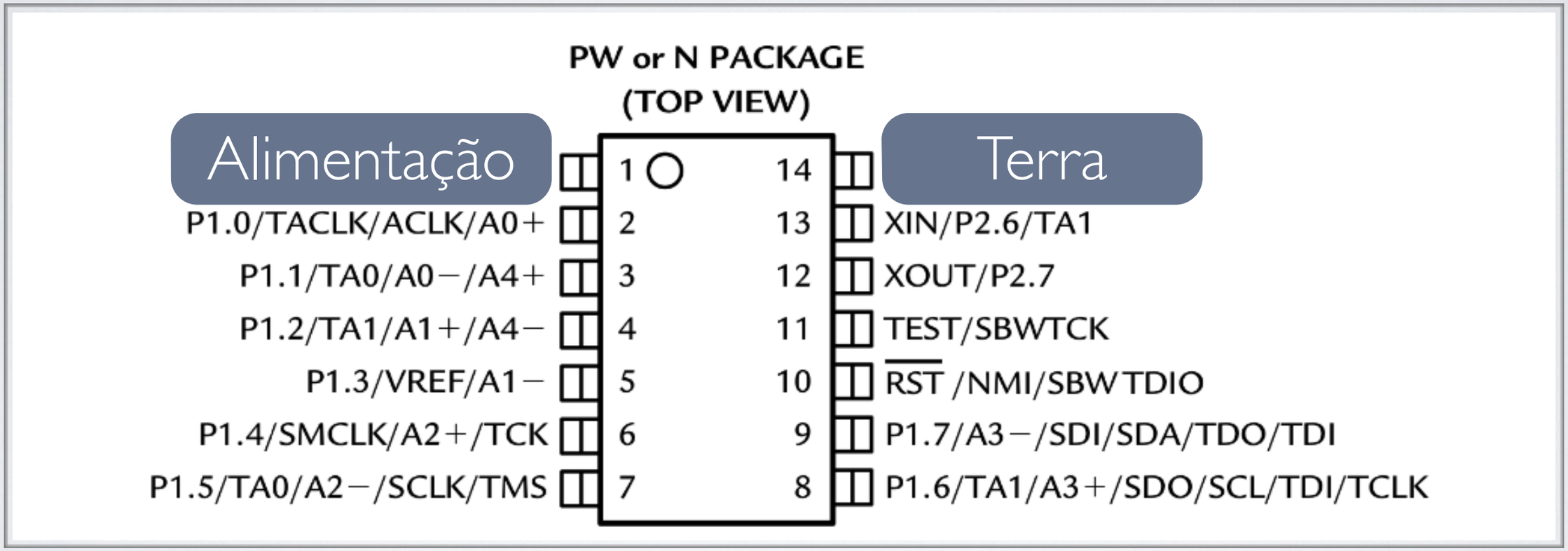
Silício é barato, pinos são caros

PW or N PACKAGE
(TOP VIEW)

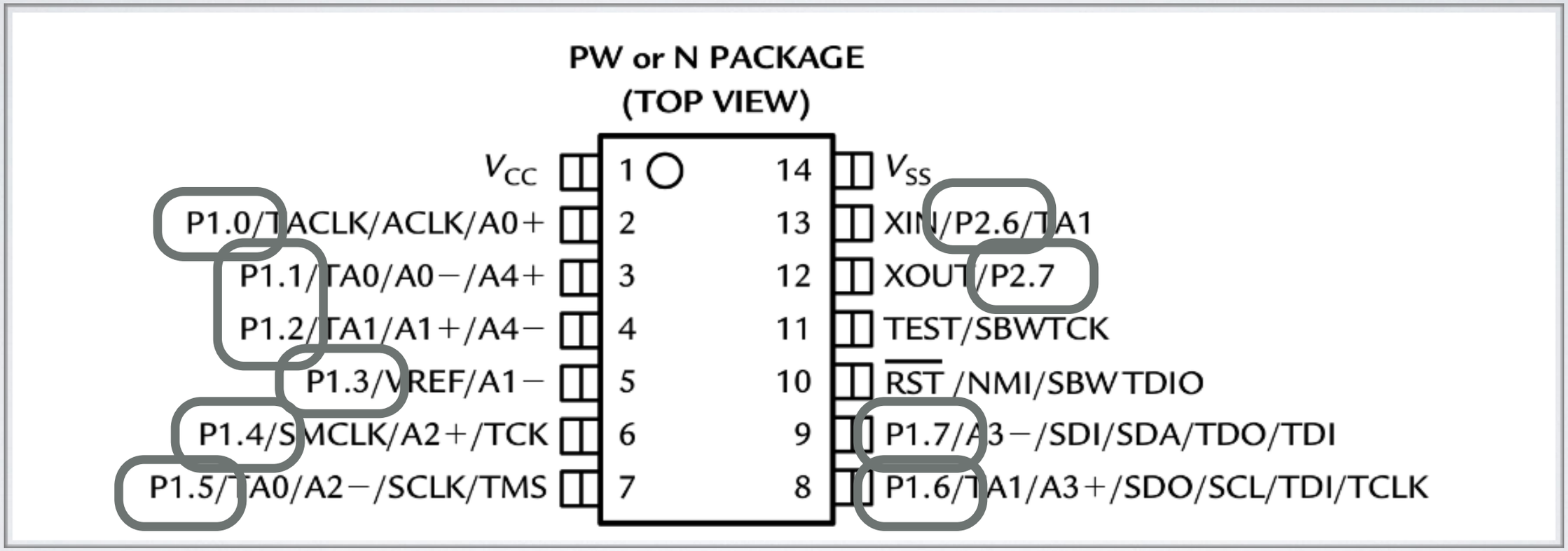


Pinos são compartilhados por funções do MSP430

PINAGEM

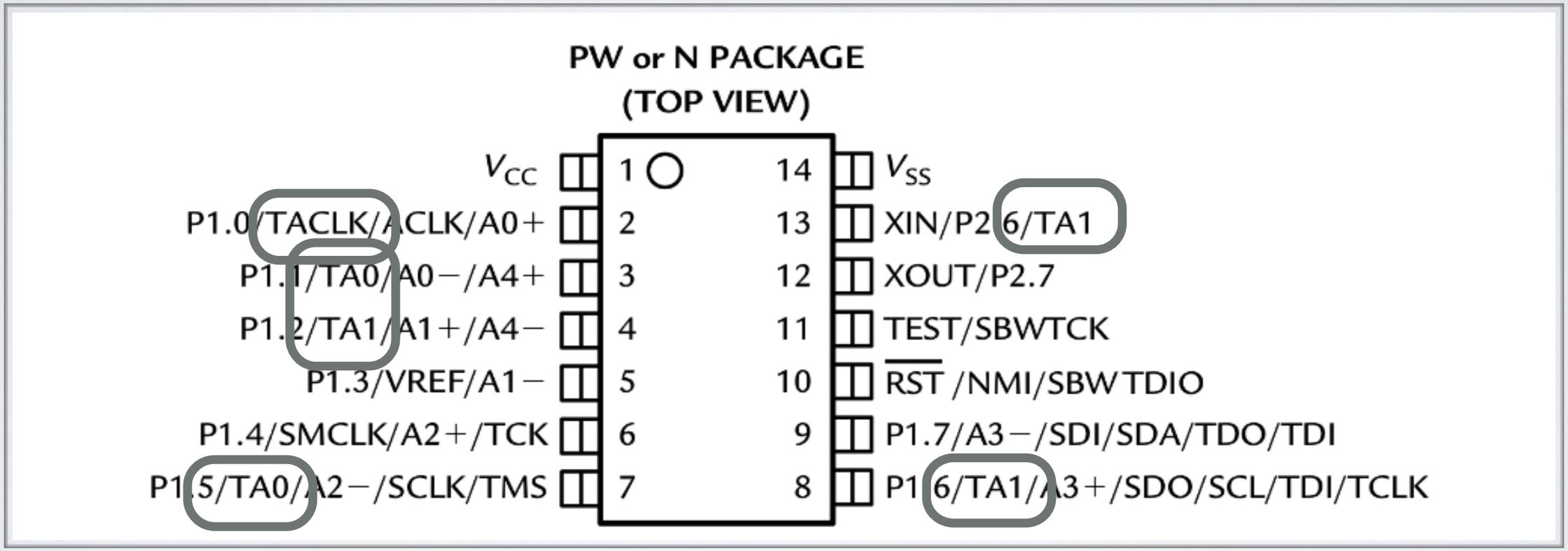

PW or N PACKAGE
(TOP VIEW)
Alimentação
Terra
P1.0/TACLK/ACLK/A0+
P1.1/TA0/A0−/A4+
P1.2/TA1/A1+/A4−
P1.3/VREF/A1−
P1.4/SMCLK/A2+/TCK
P1.5/TA0/A2−/SCLK/TMS
XIN/P2.6/TA1
XOUT/P2.7
TEST/SBWTCK
RST /NMI/SBW TDIO
P1.7/A3−/SDI/SDA/TDO/TDI
P1.6/TA1/A3+/SDO/SCL/TDI/TCLK
1
2
3
4
5
6
7
8
9
10
11
12
13
14

PINAGEM



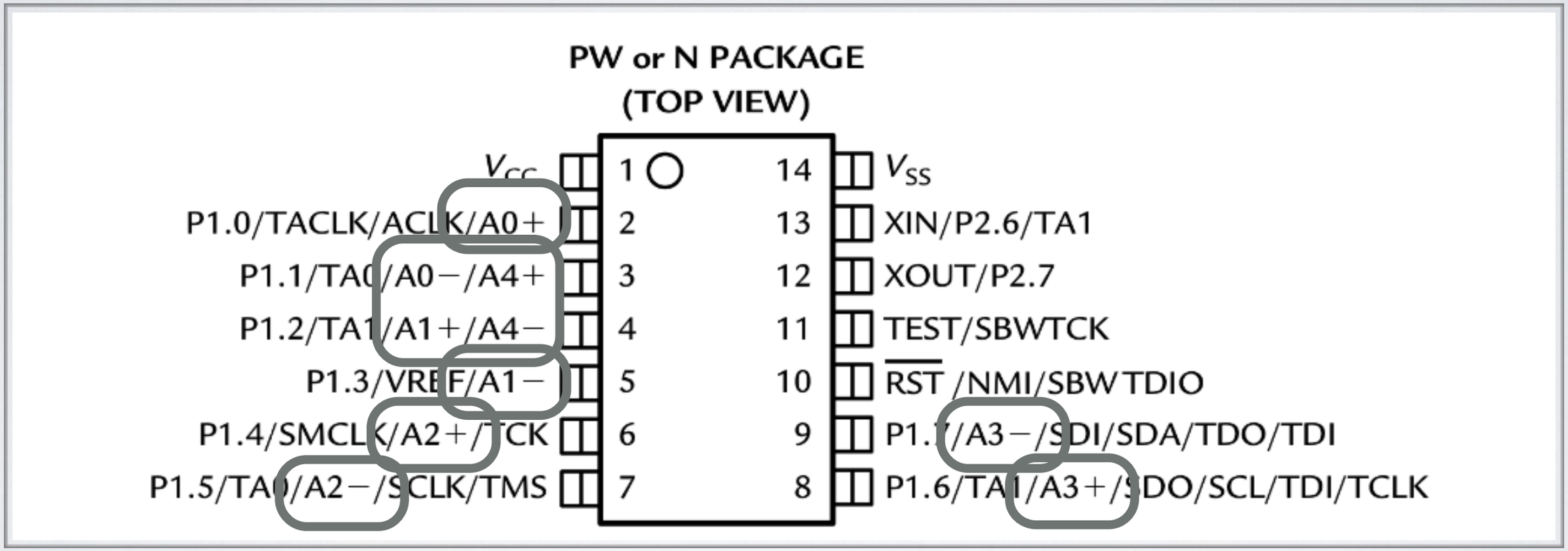
P1.0-P1.7 e P2.6-P2.7 são entradas e saídas digitais

PINAGEM



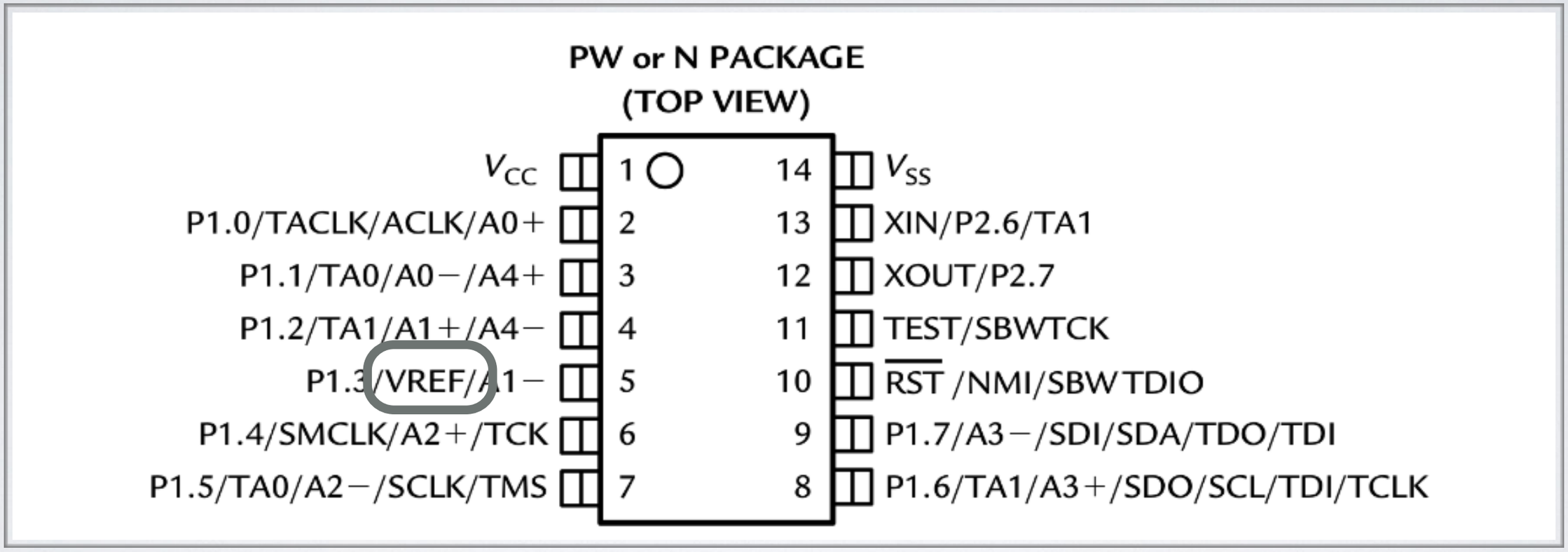
TACLK pode ser usado como entrada do clock do Timer_A. TA0 e TA1 podem ser entradas ou saídas do Timer_A.

PINAGEM



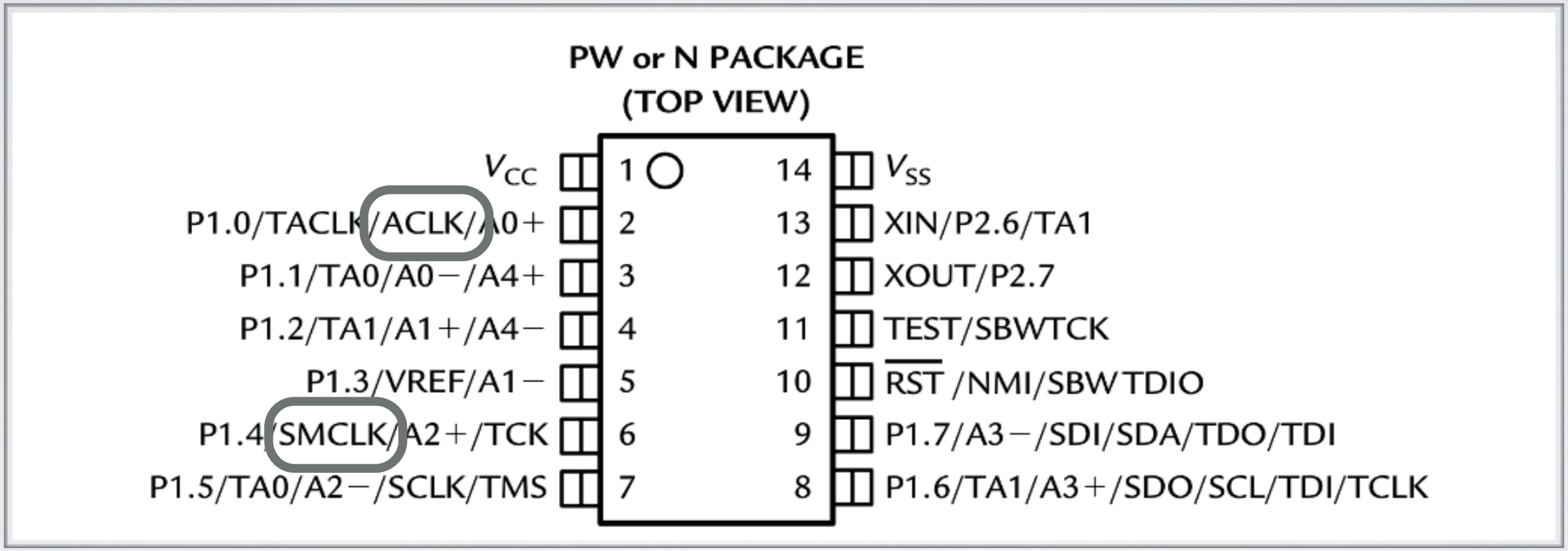
A0-, A0+, ..., A3-, A3+ são entradas do conversor A/D

PINAGEM



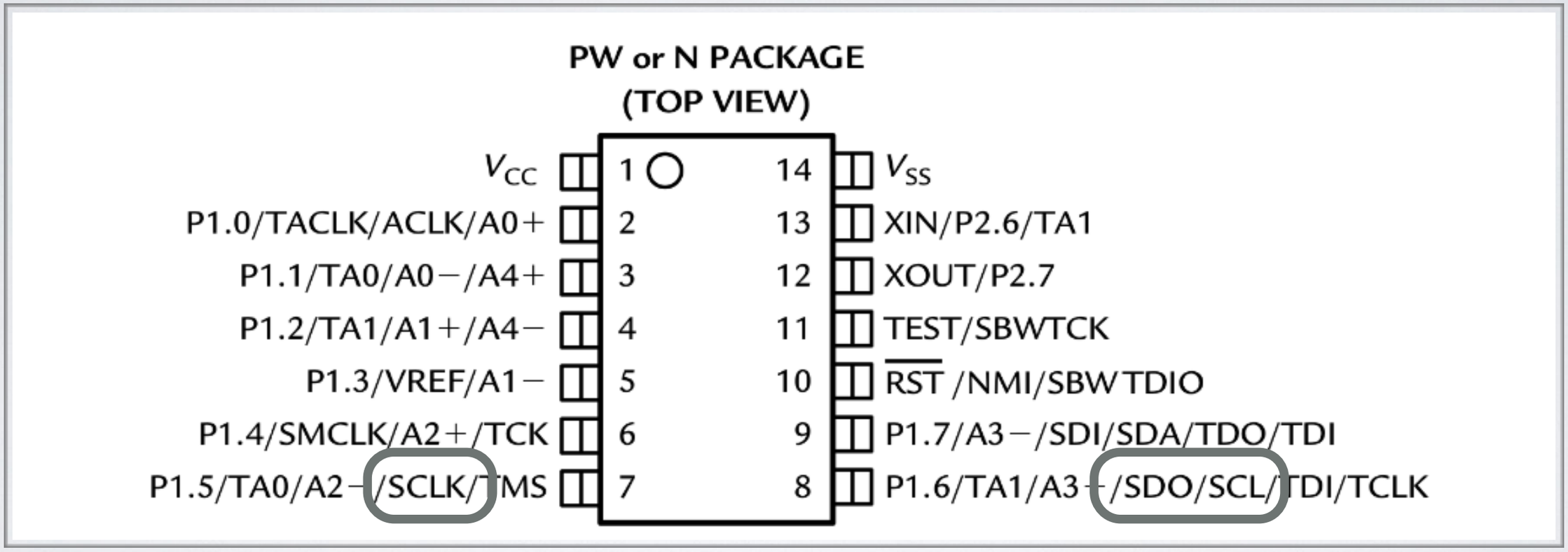
VREF é a tensão de referência para o conversor A/D

PINAGEM



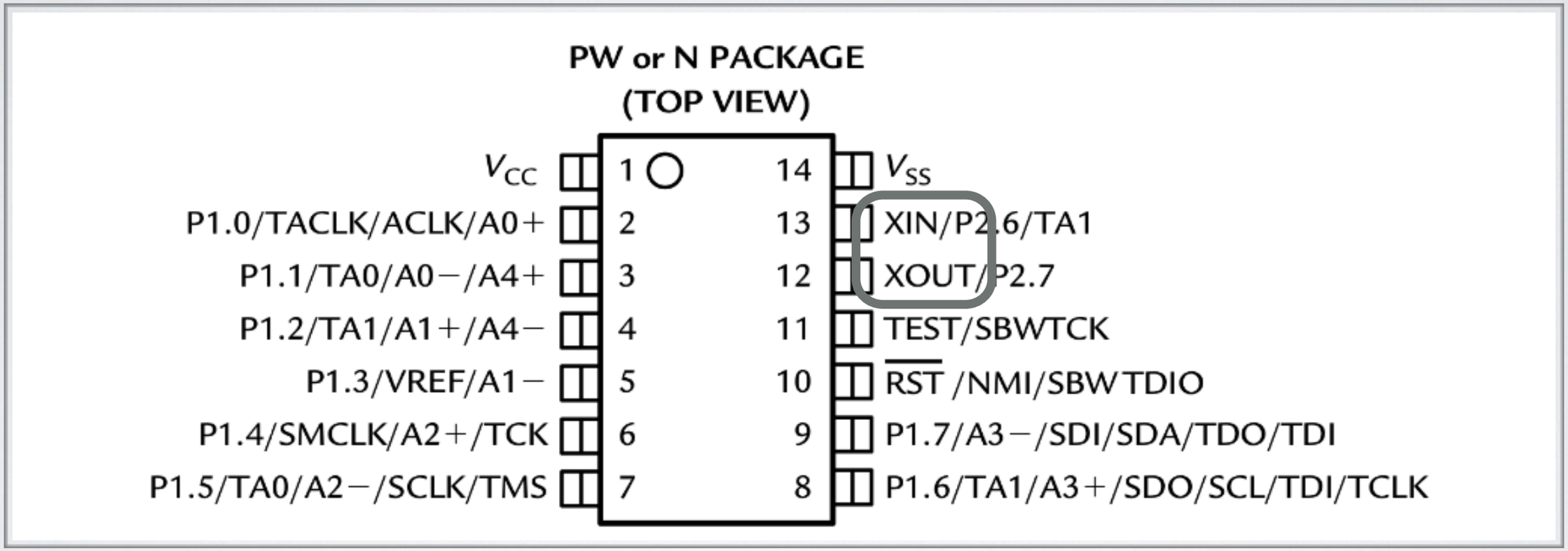
SMCLK e ACLK são saídas para o sinal de clock do MSP430, para serem aproveitados por outros componentes e para testar o MSP430

PINAGEM



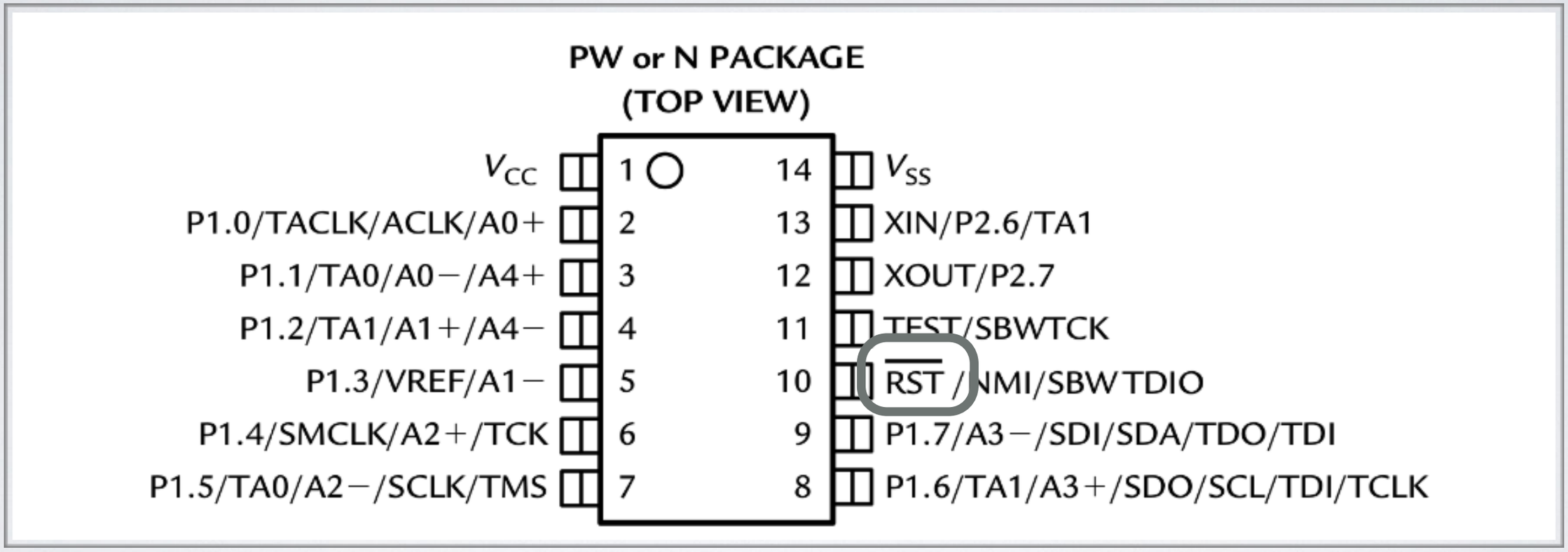
SCLK, SDO e SCL são usados pela interface serial universal (comunicação SPI e I2C)

PINAGEM



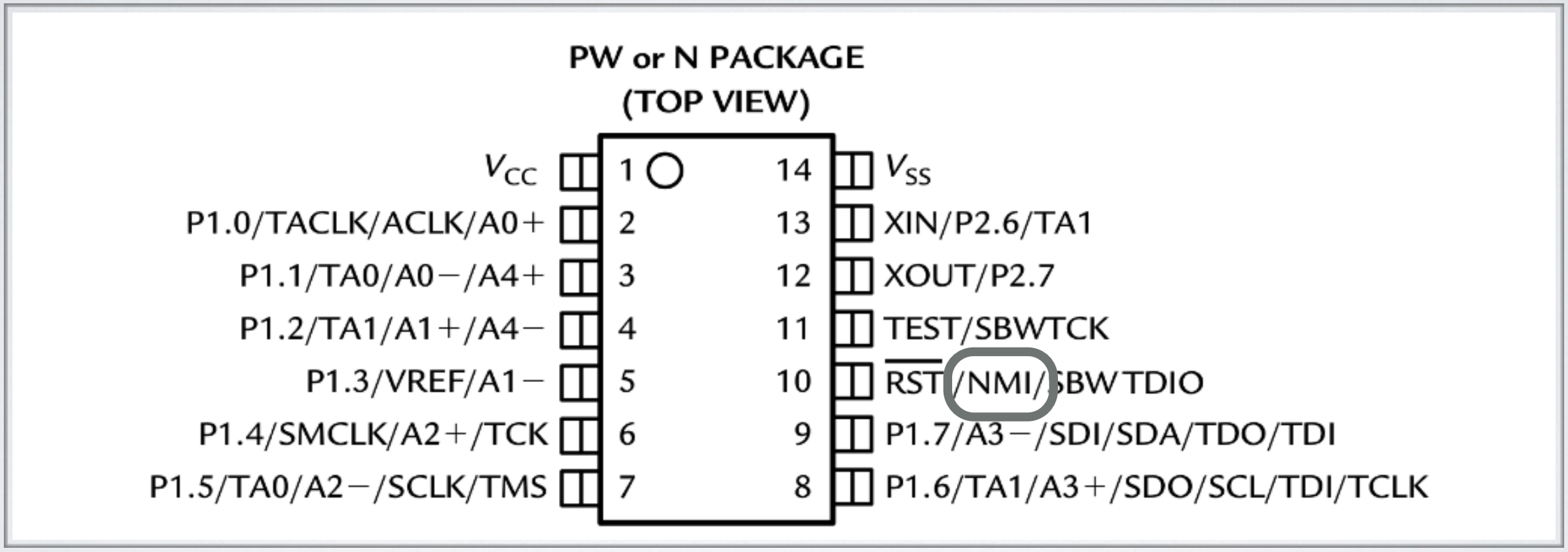
XIN e XOUT são as conexões para o cristal externo, para gerar um clock estável

PINAGEM



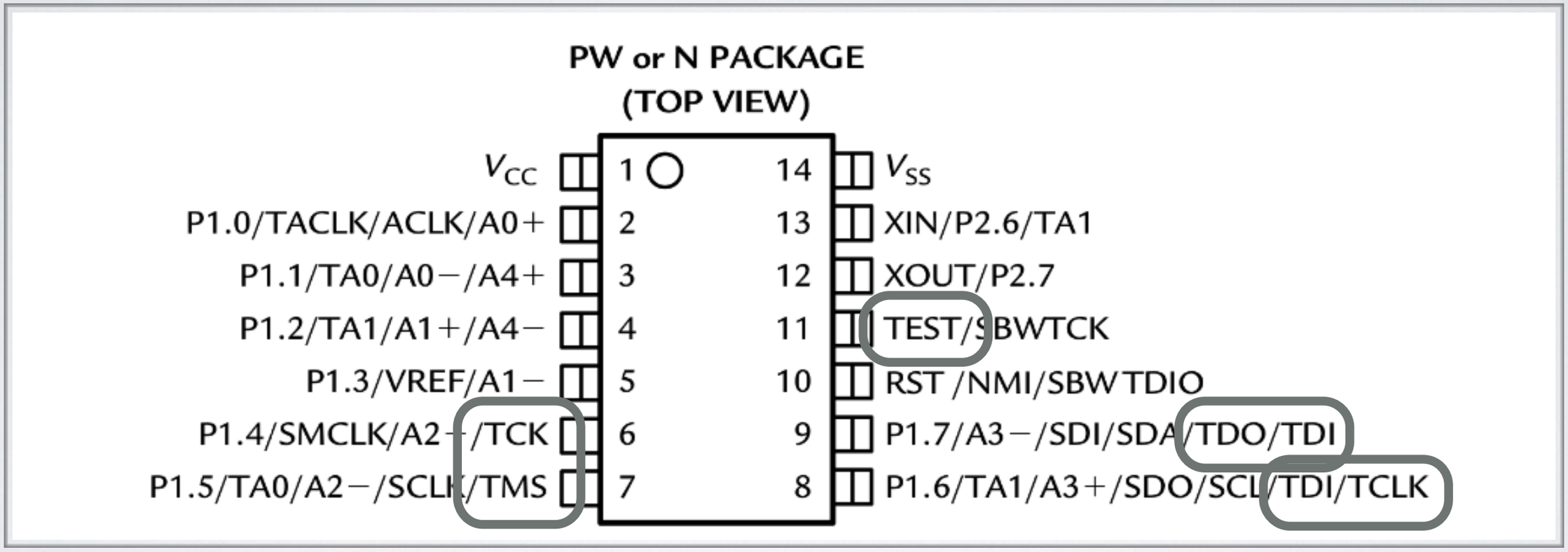
_RST reseta o MSP430 quando levado ao nível baixo

PINAGEM



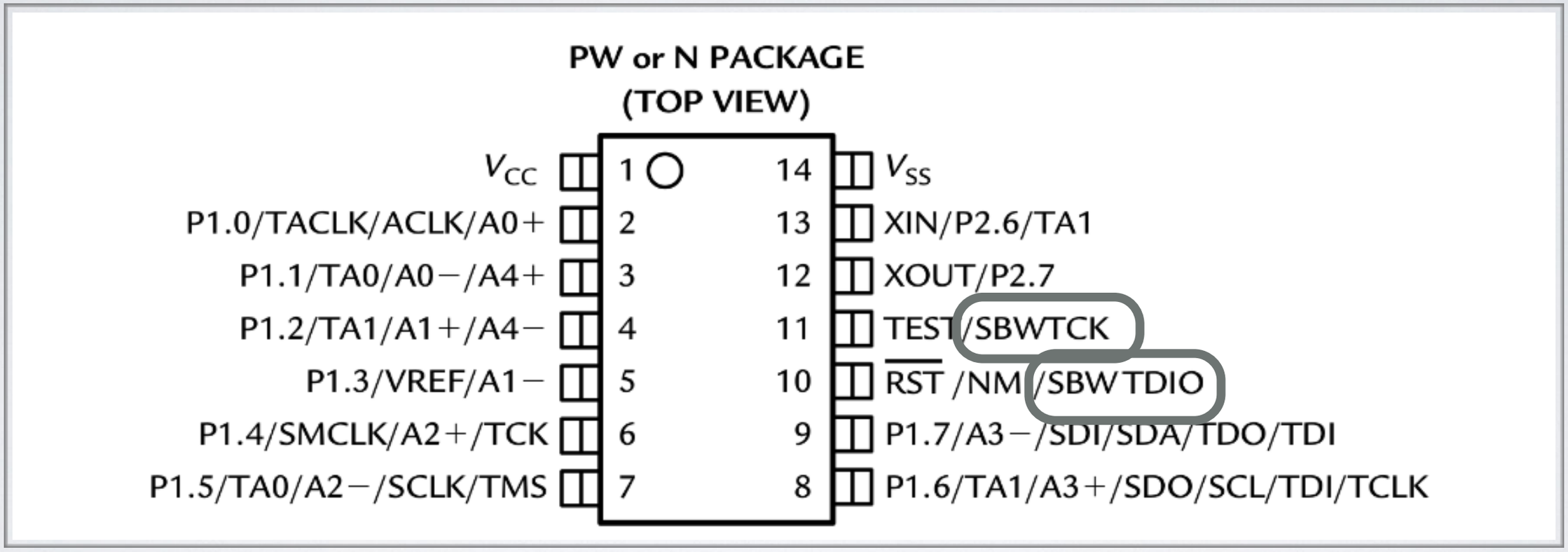
NMI é a entrada para interrupção não-mascarável, que permite um sinal externo interromper o programa principal

PINAGEM



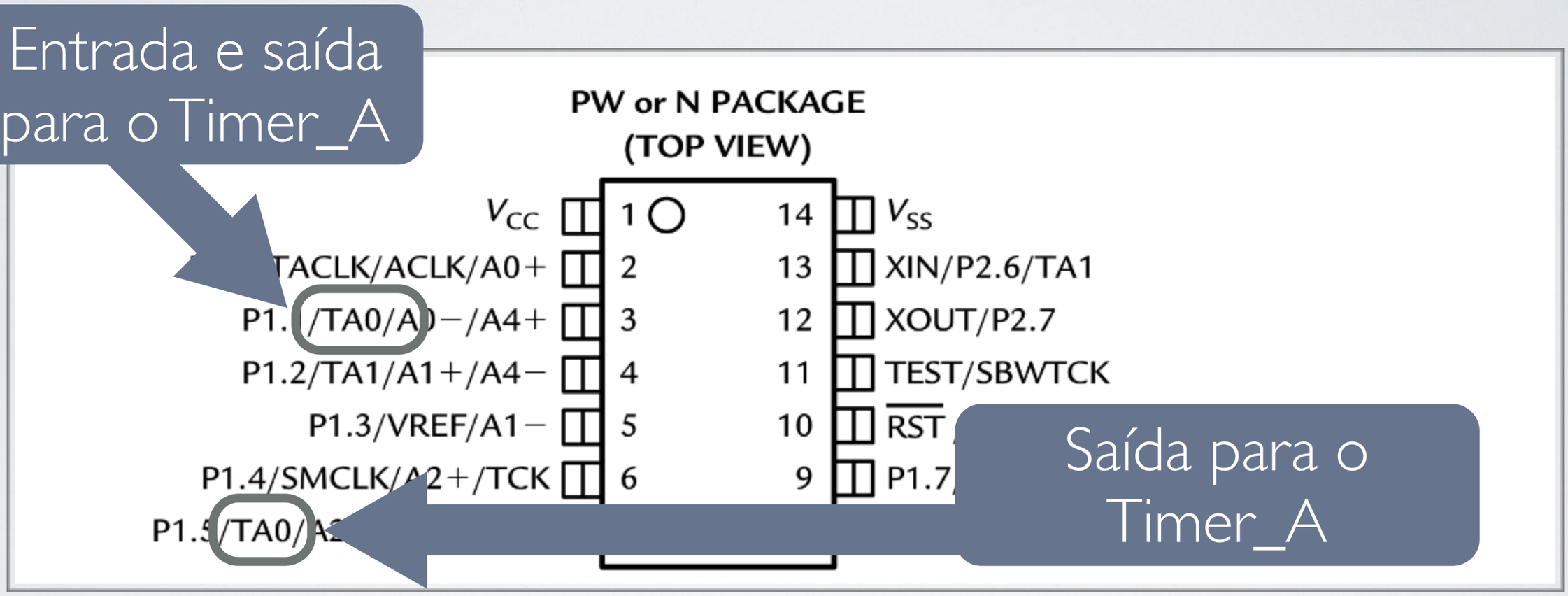
TCK, TMS, TCLK, TDI e TDO formam
a interface JTAG, usada para
programar e debugar o MSP430

PINAGEM



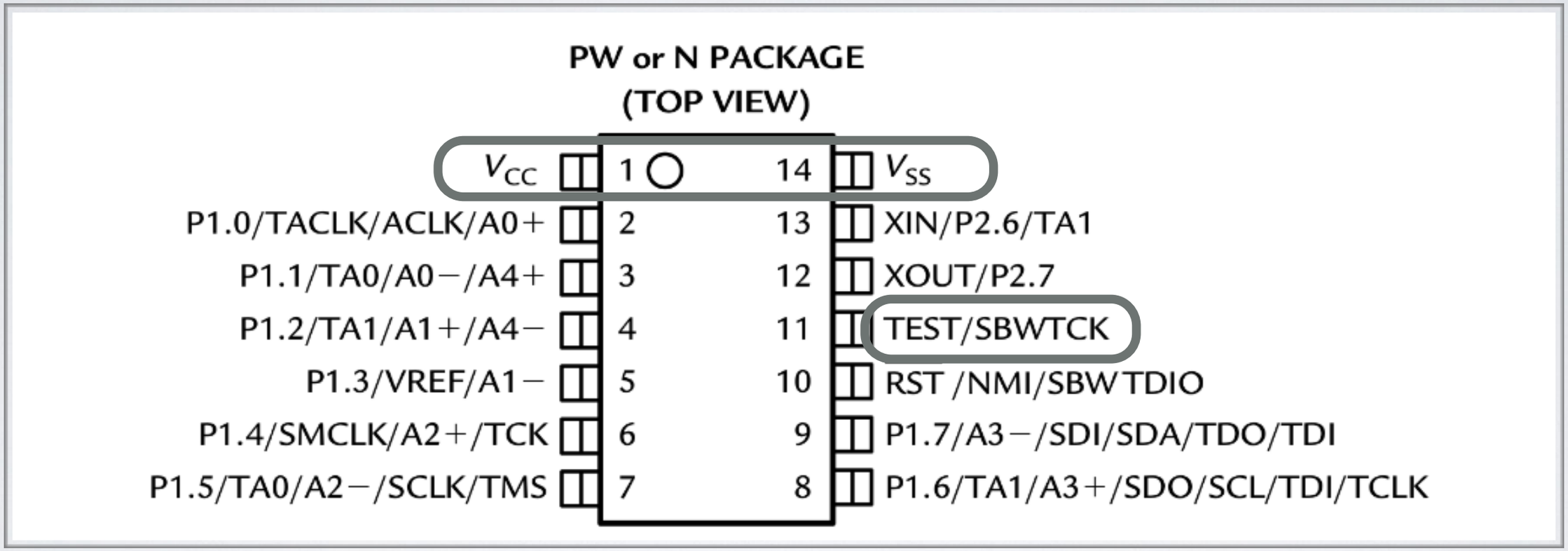
SBWTCK e SBWTDIO formam a interface Spy-Bi-Wire, uma alternativa ao JTAG

PINAGEM



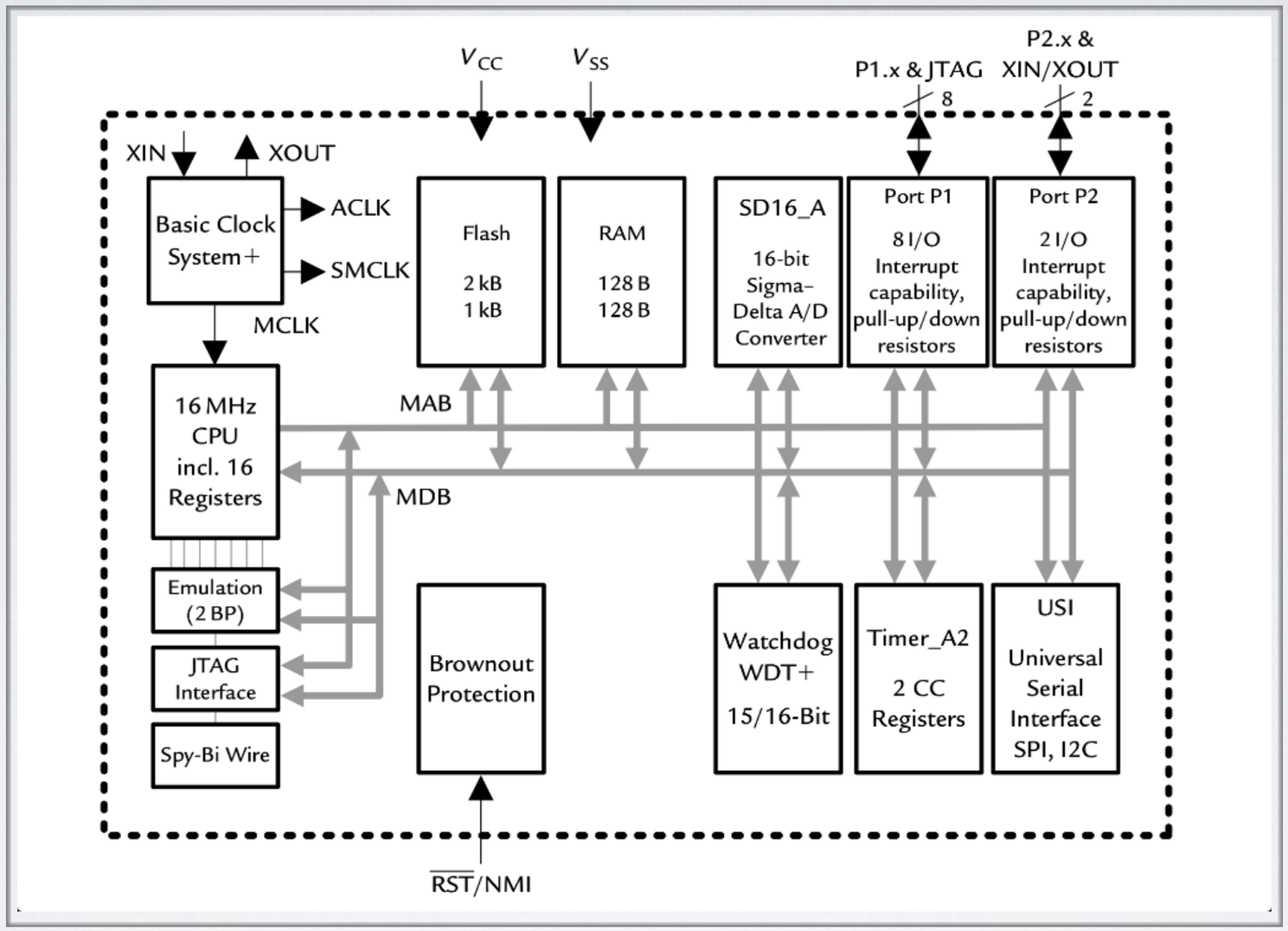
A mesma função em dois pinos diferentes pode não funcionar da mesma forma

PINAGEM

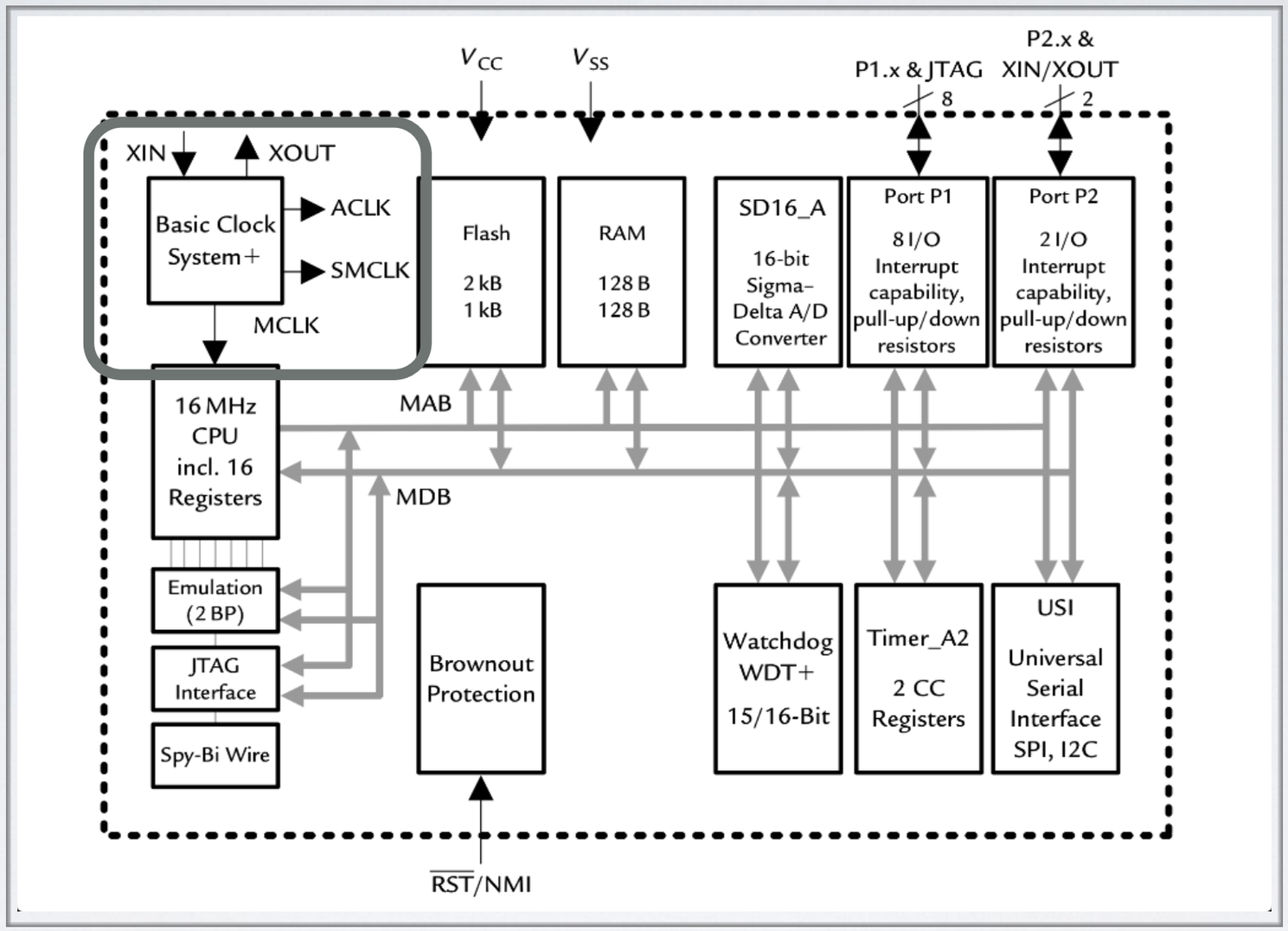


Únicos pinos que não podem alterados

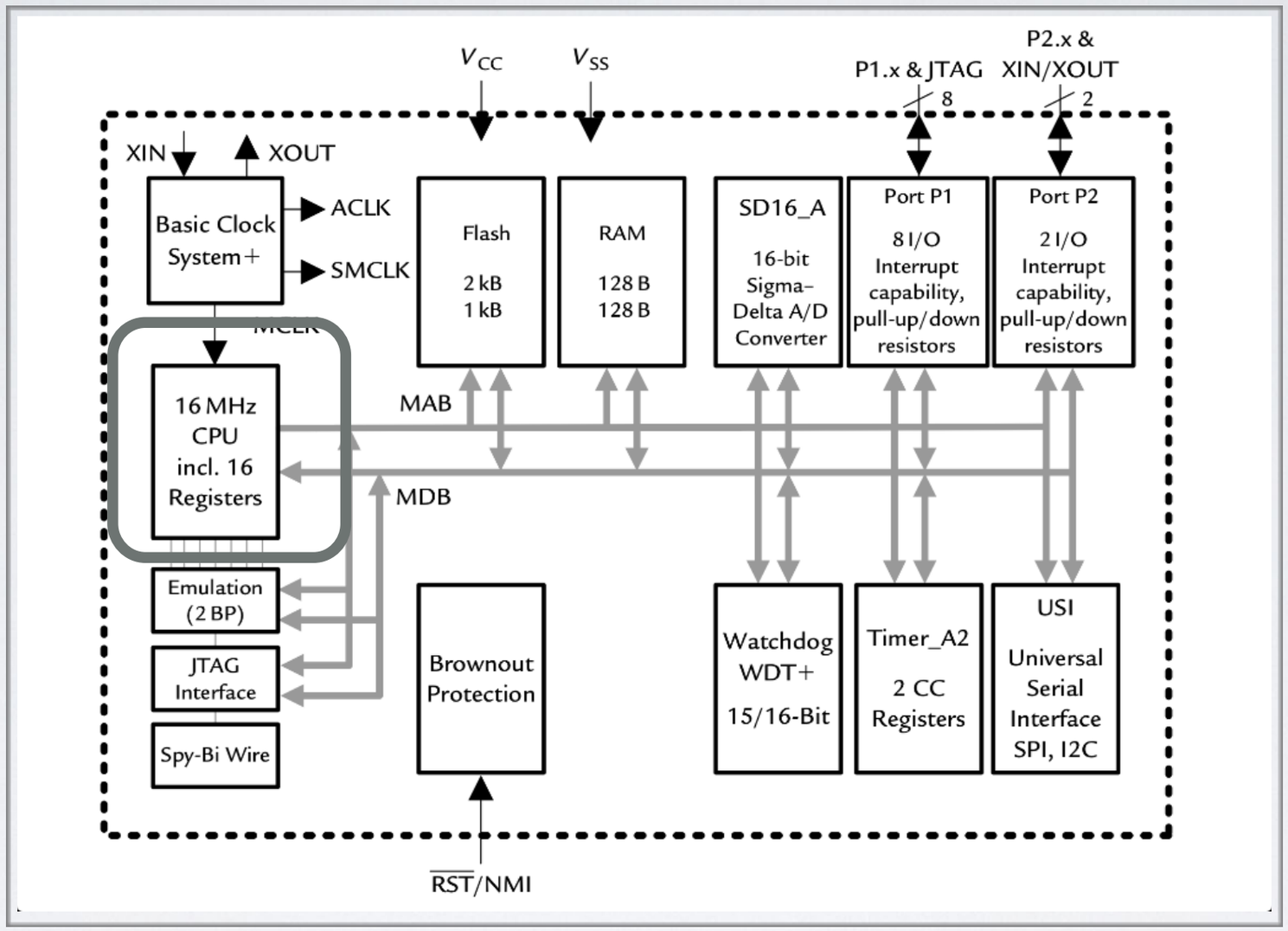
VISÃO INTERNA



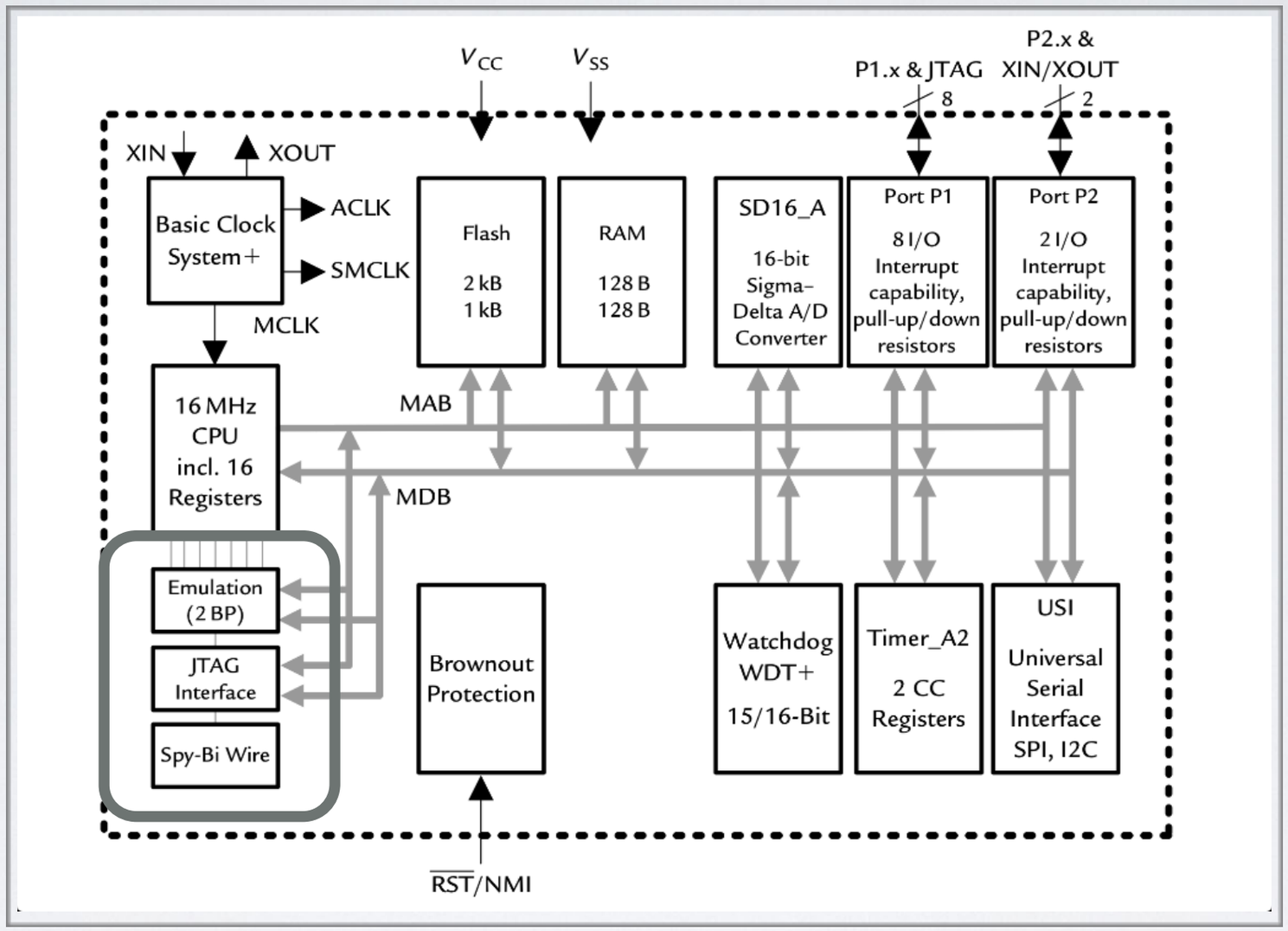
VISÃO INTERNA



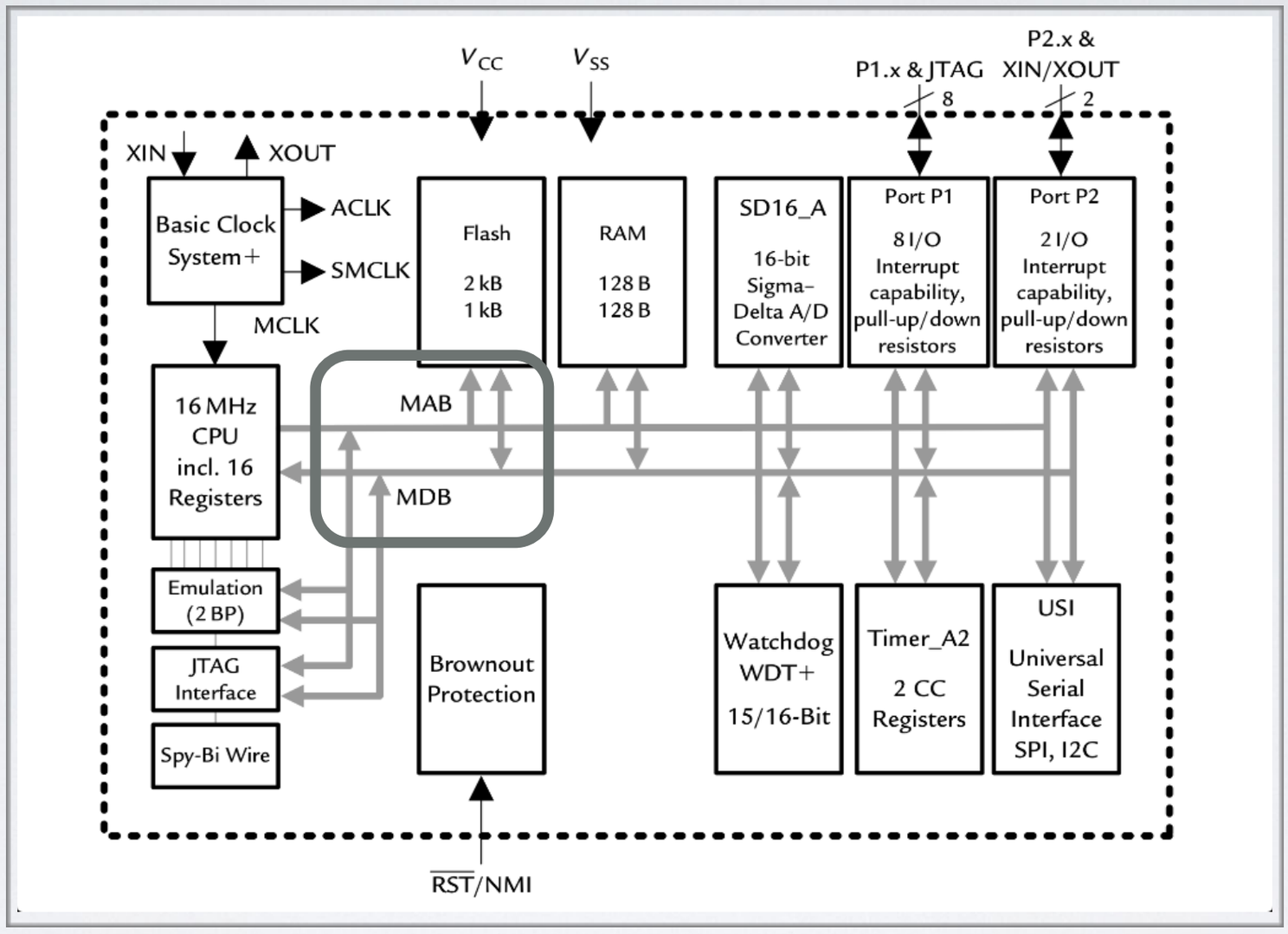
VISÃO INTERNA



VISÃO INTERNA



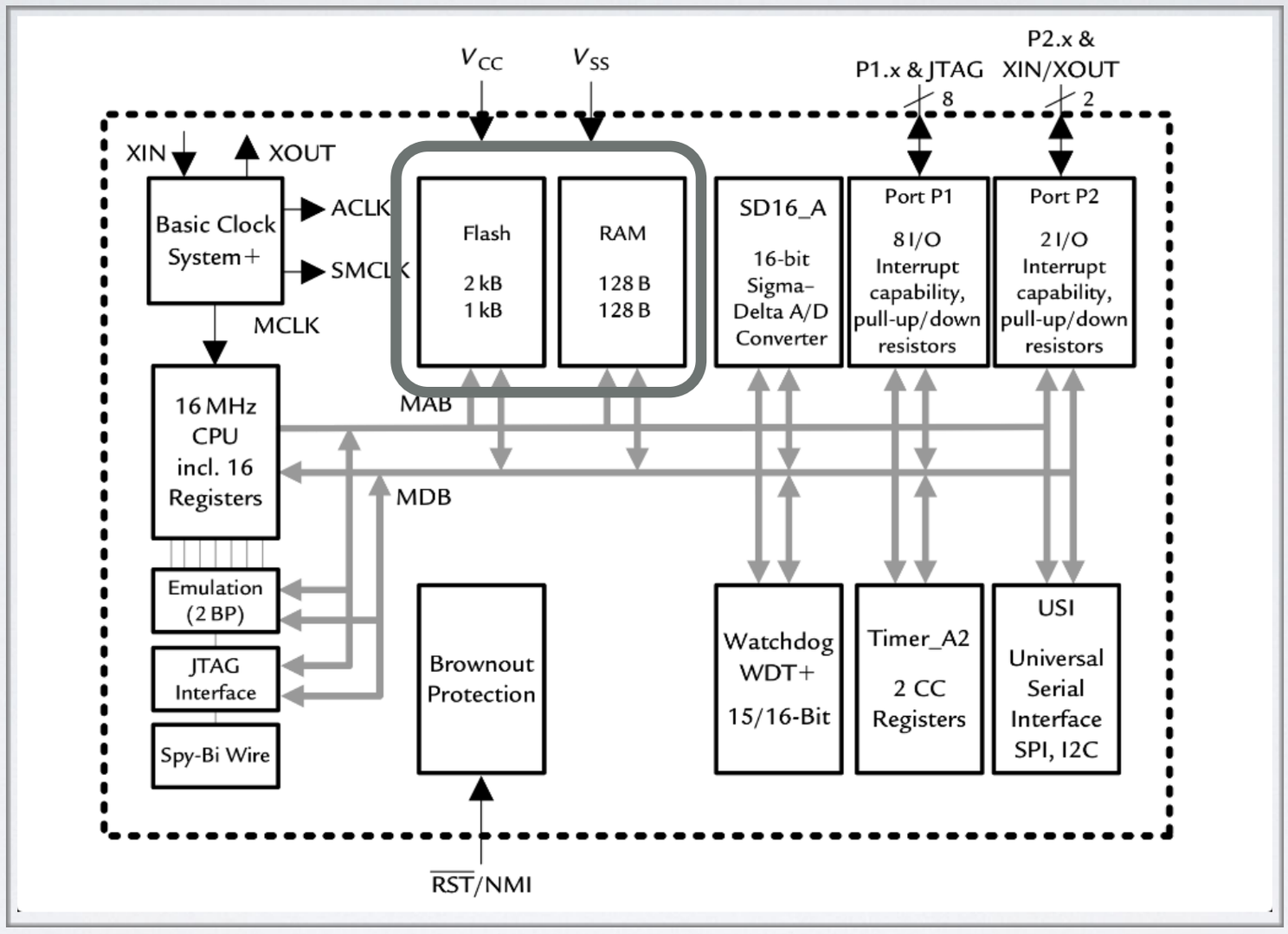
VISÃO INTERNA



MAB - barramento de endereços na memória

MDB - barramento de dados na memória

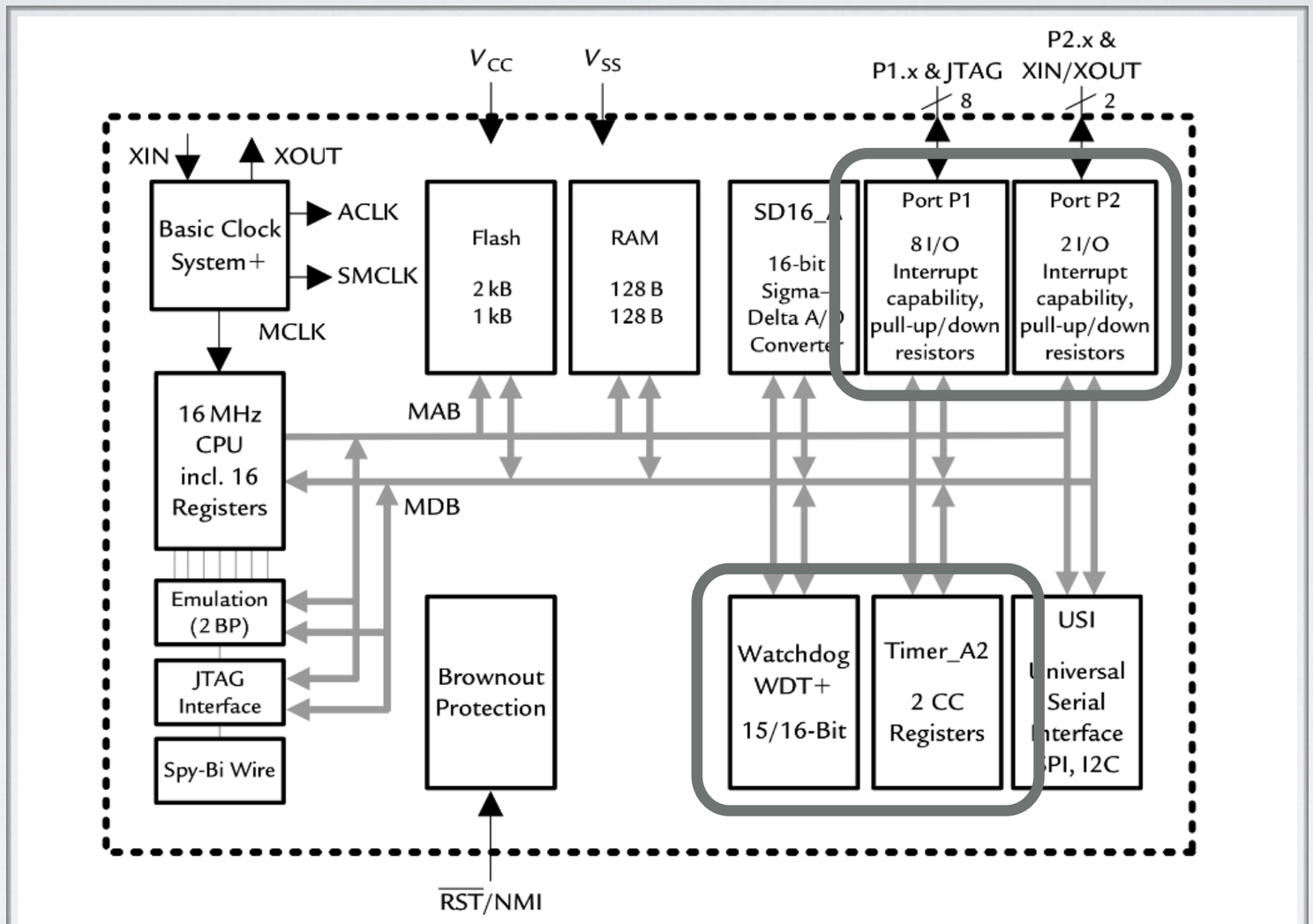
VISÃO INTERNA



MSP430F2003 tem 1KB de flash e 128 bytes de RAM

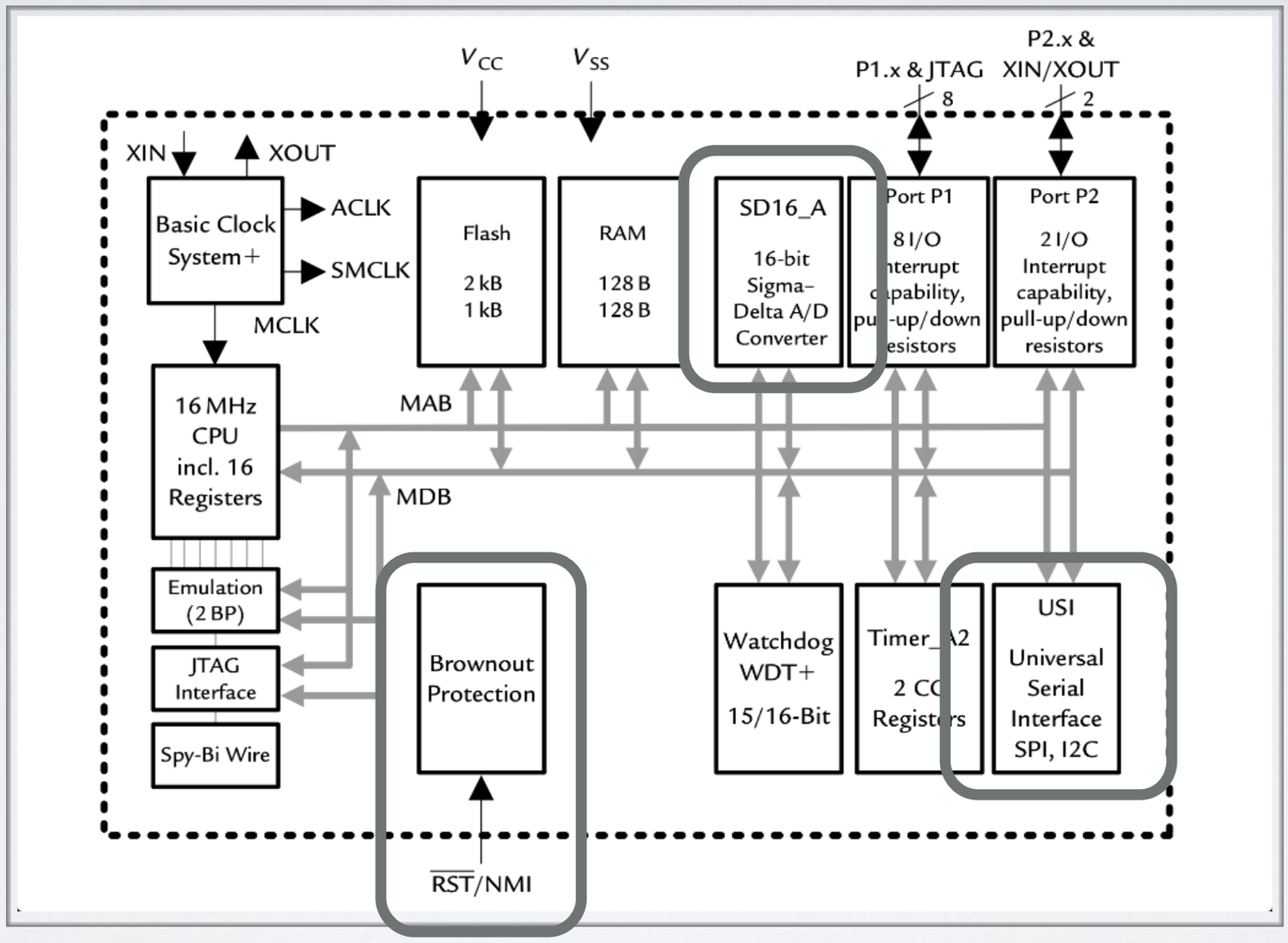
MSP430F2231 tem 2KB de flash e 128 bytes de RAM

VISÃO INTERNA



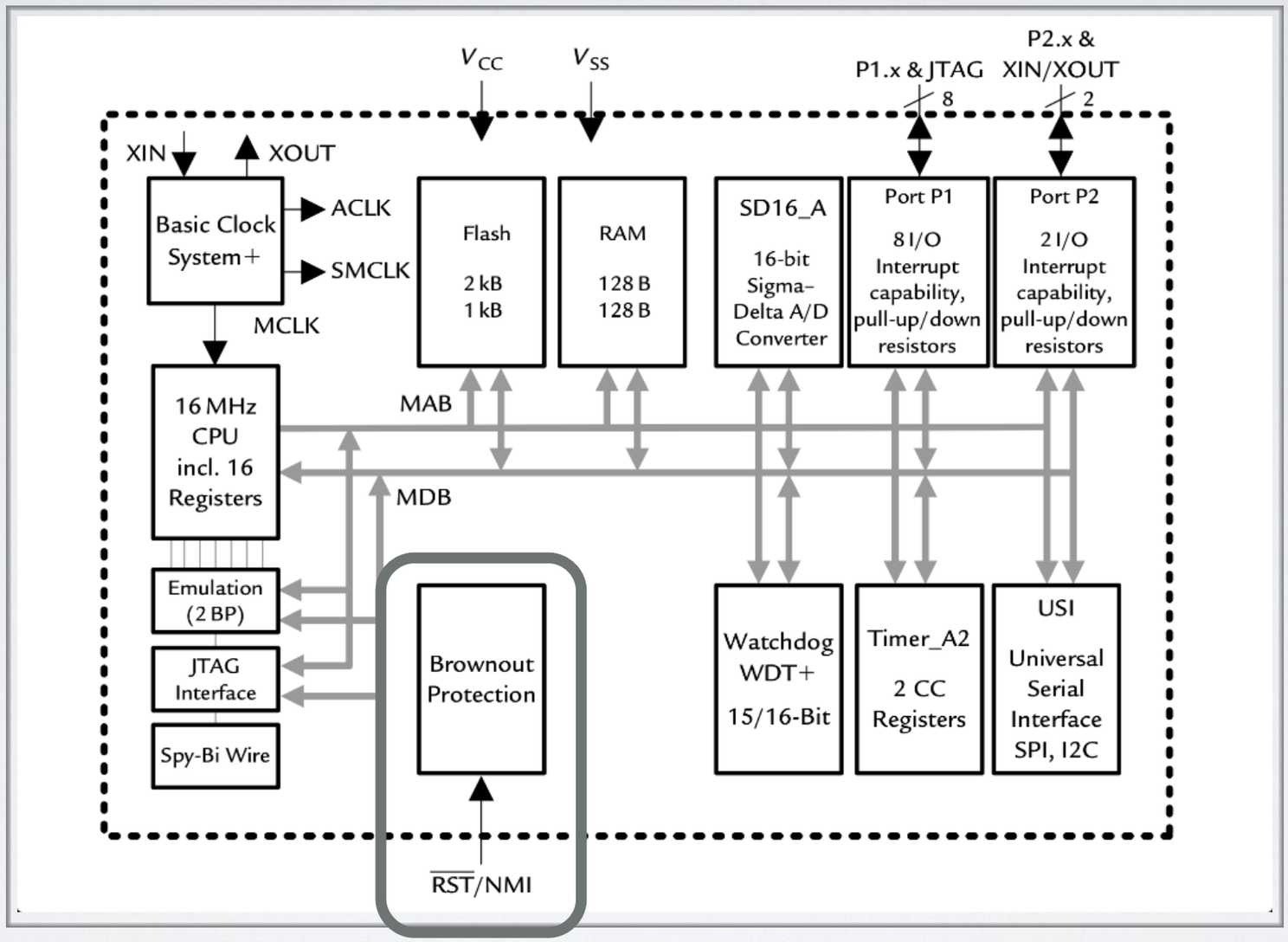
Periféricos presentes em todos os modelos de MSP430

VISÃO INTERNA



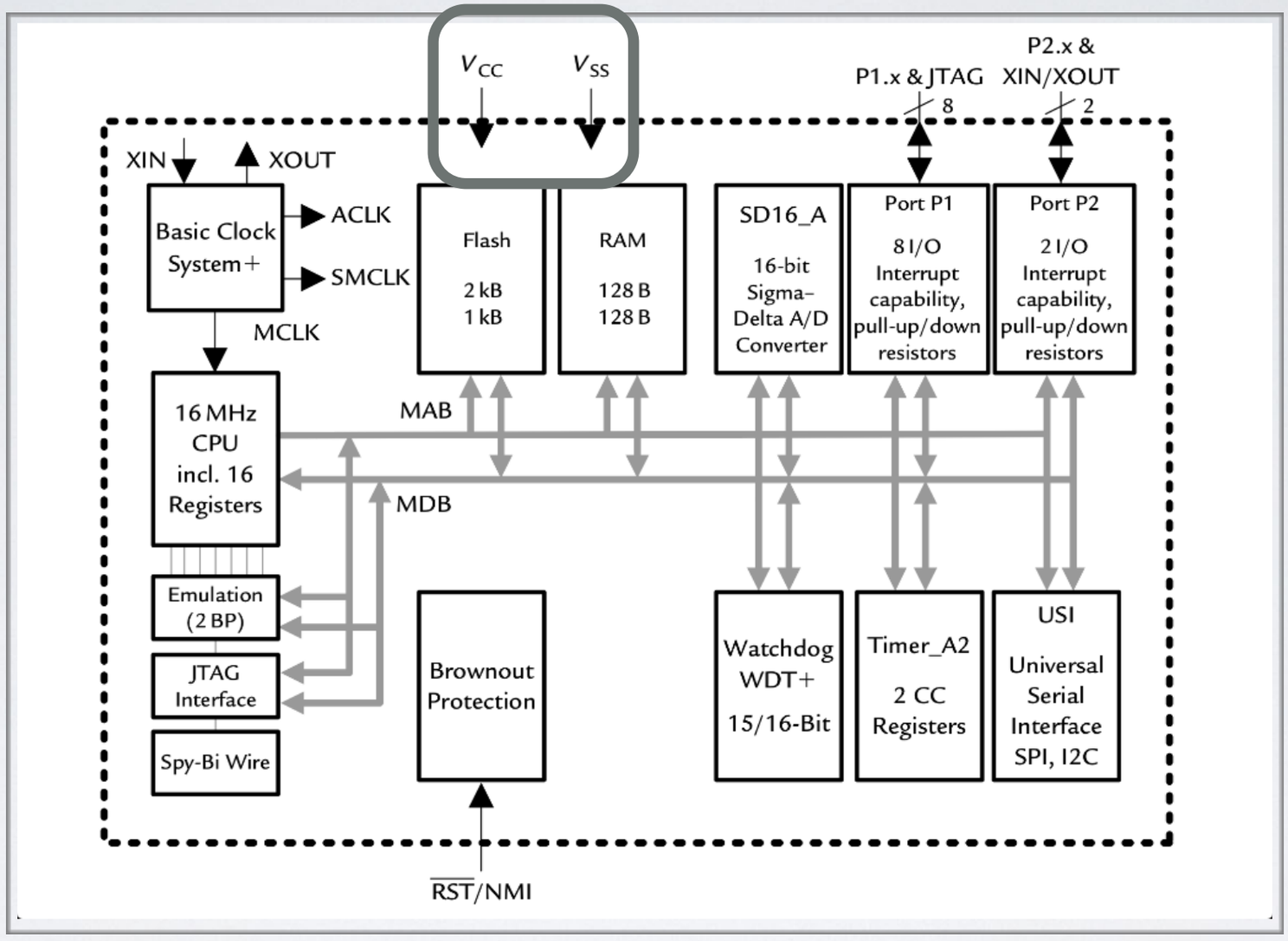
Periféricos dependentes do modelo de MSP430

VISÃO INTERNA



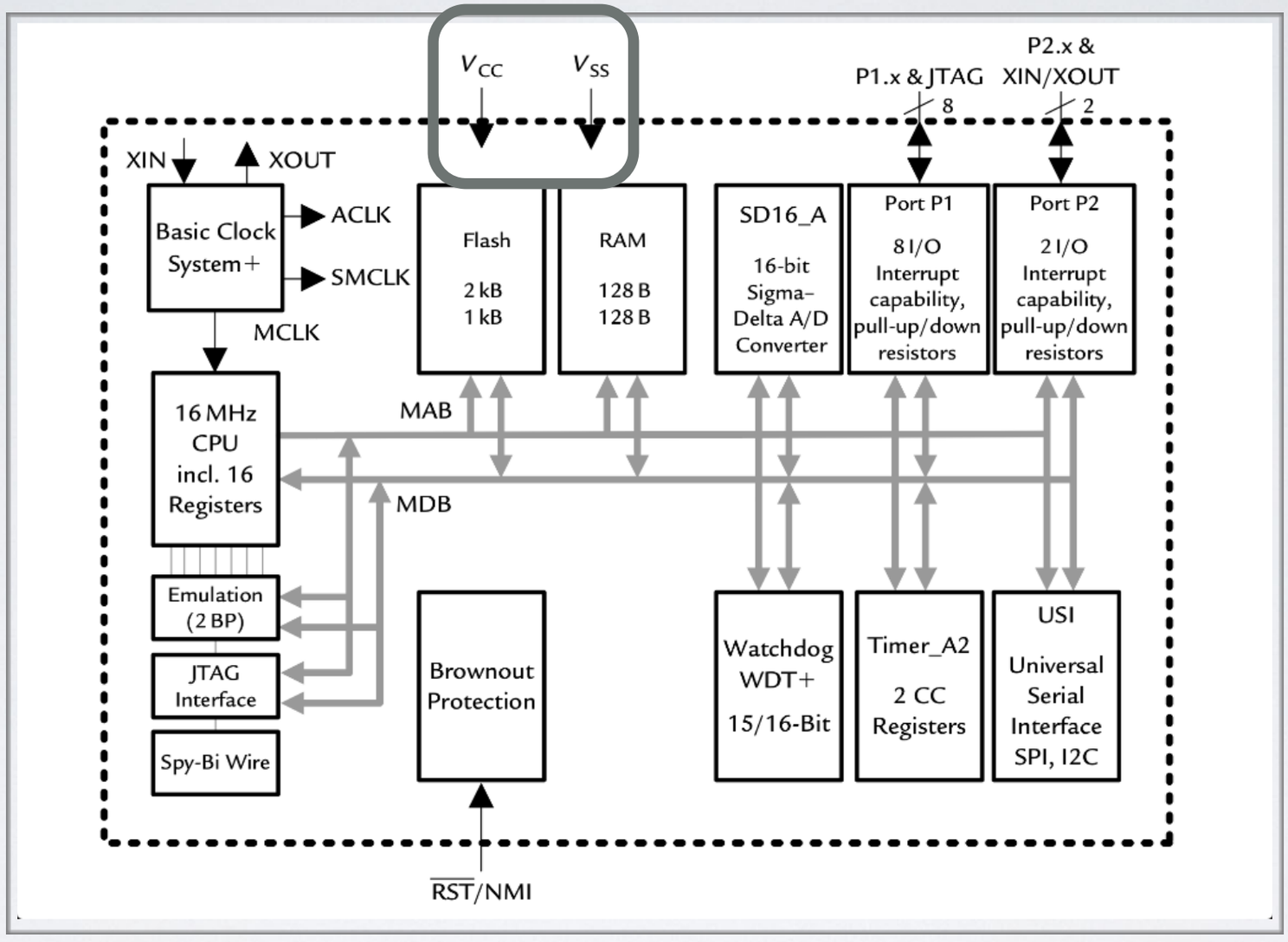
Proteção para baixos níveis de tensão de alimentação

VISÃO INTERNA



VSS é o terra, e VCC é a alimentação (1,8-3,6V para o MSP430F2013)

VISÃO INTERNA



De acordo com o nível de VCC, perde-se algumas funcionalidades, como a programação da flash e o clock em frequência máxima

MEMÓRIA

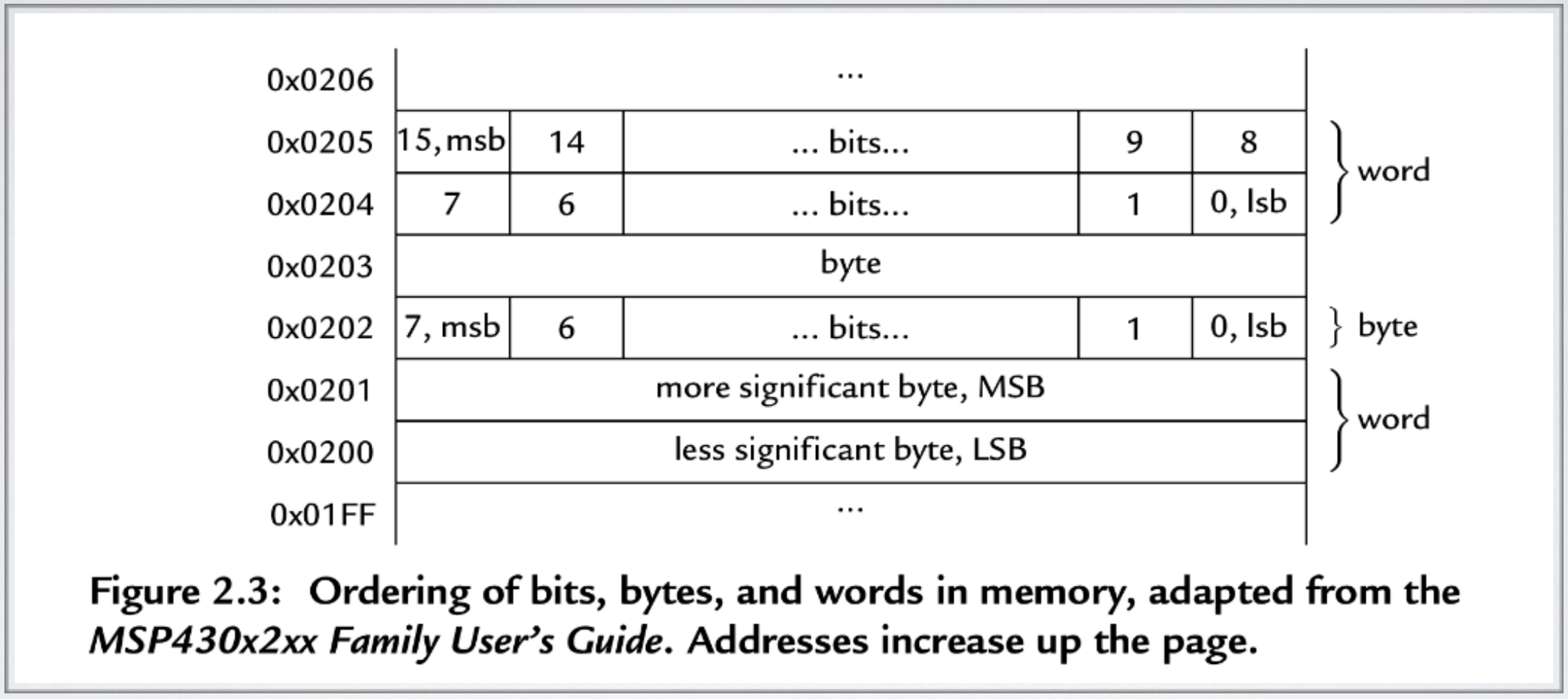
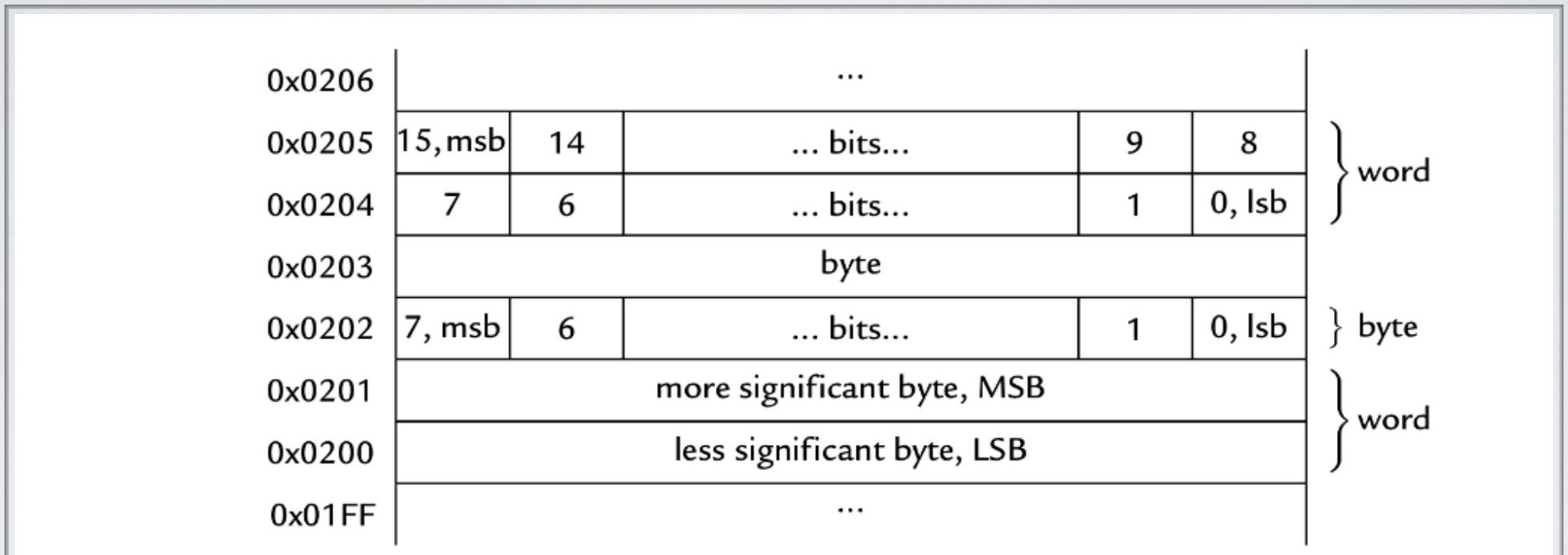


Figure 2.3: Ordering of bits, bytes, and words in memory, adapted from the *MSP430x2xx Family User's Guide*. Addresses increase up the page.

MEMÓRIA

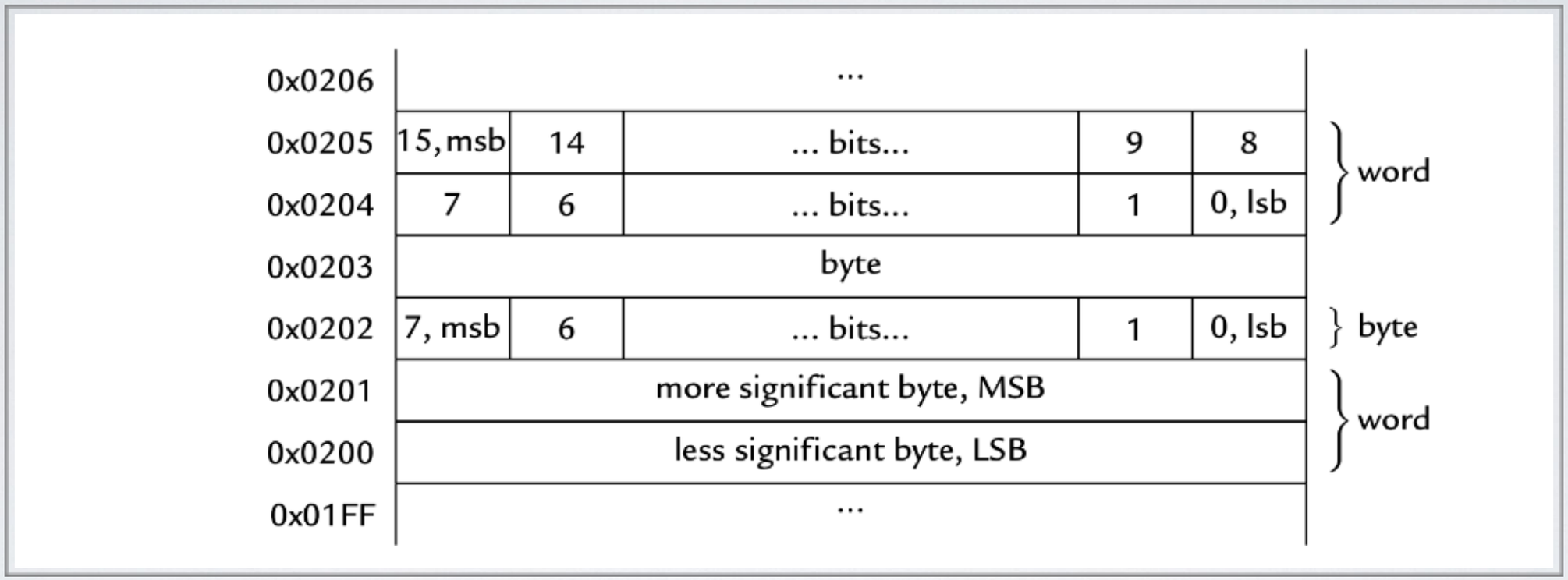


Memória separada em bytes

Barramento de endereço de 16 bits

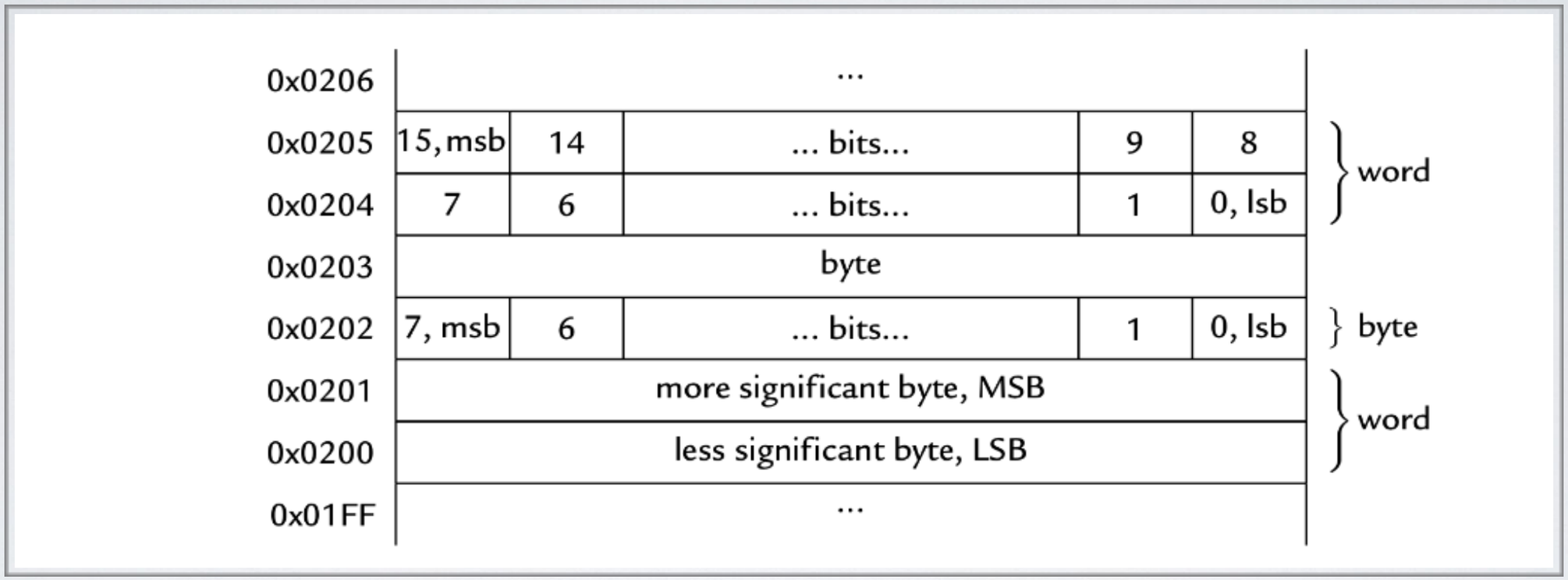
2^16 = 64KB de memória

MEMÓRIA



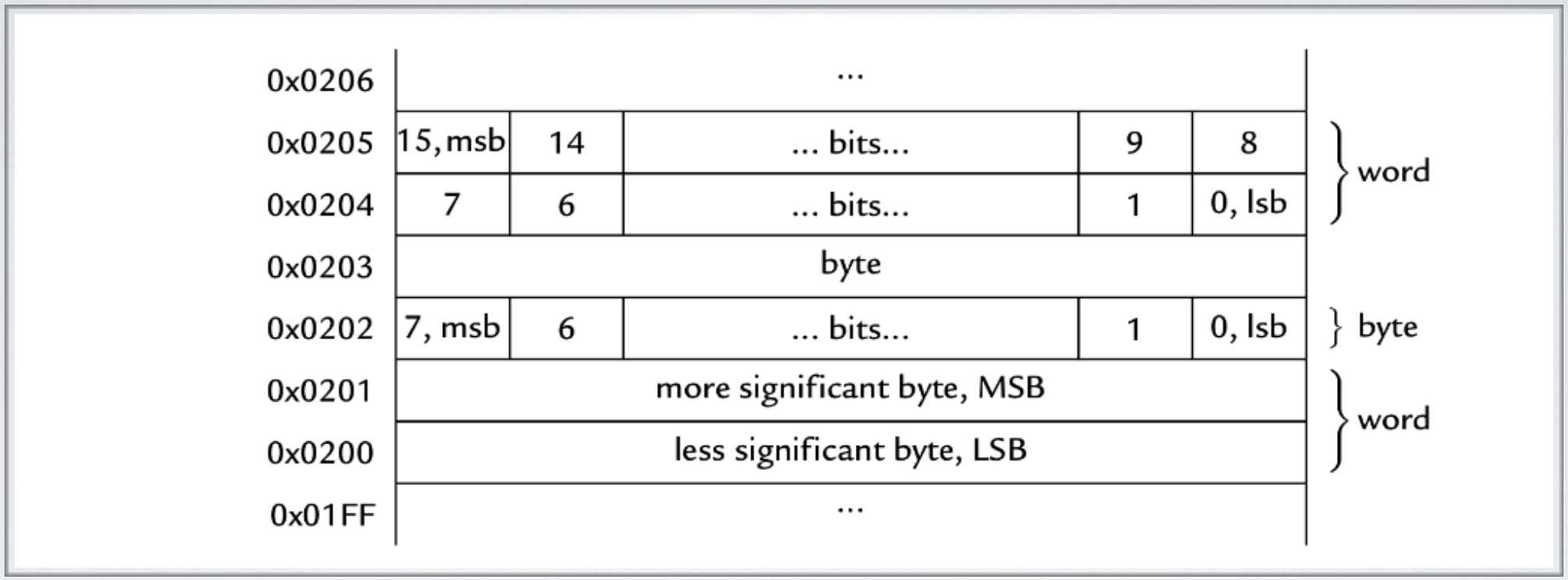
Primeiro endereço é 0x0000
(IE1 - Interrupt Enable 1 Register),
último é 0xFFFF

MEMÓRIA



Não há conexões dos barramentos para conectar memória externa, nem maneira de aumentar a memória interna

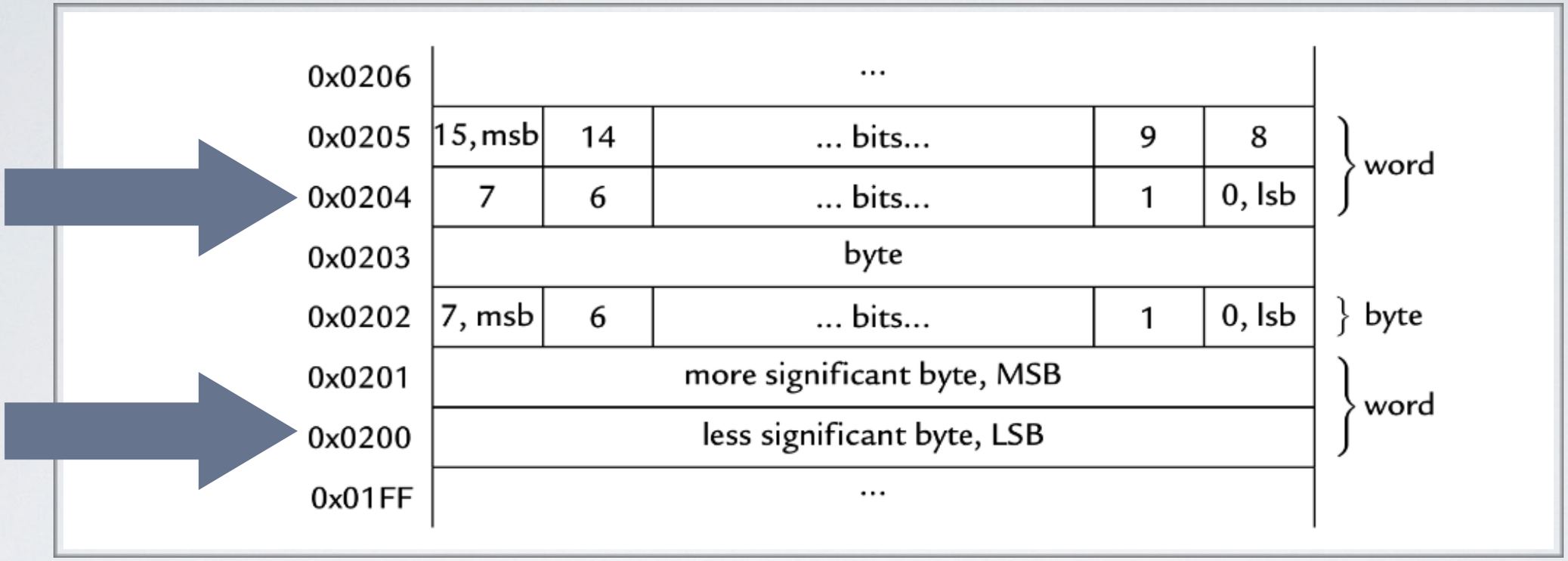
MEMÓRIA



Barramento de memória é de 16 bits

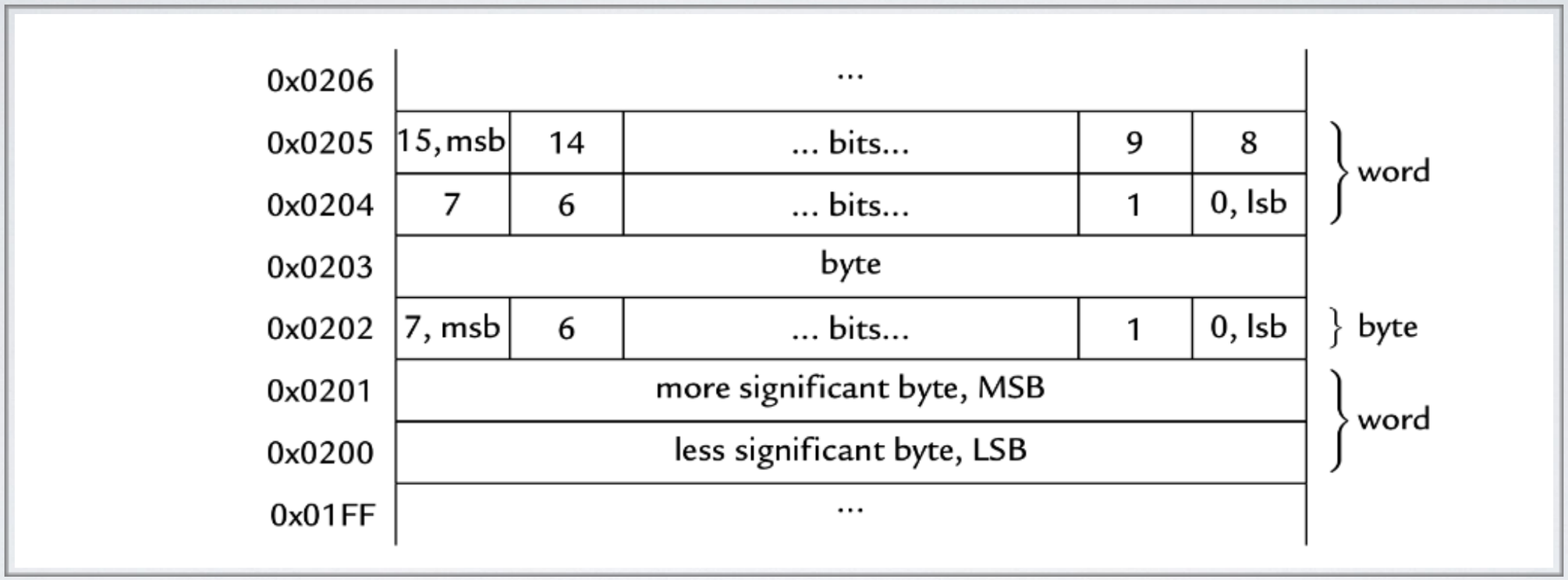
Transfere bytes ou palavras de 2 bytes

MEMÓRIA



O endereço da palavra de 2 bytes é dado pelo byte no endereço menor (sempre par), e esta palavra pode ser lida em um ciclo de clock do barramento

MEMÓRIA

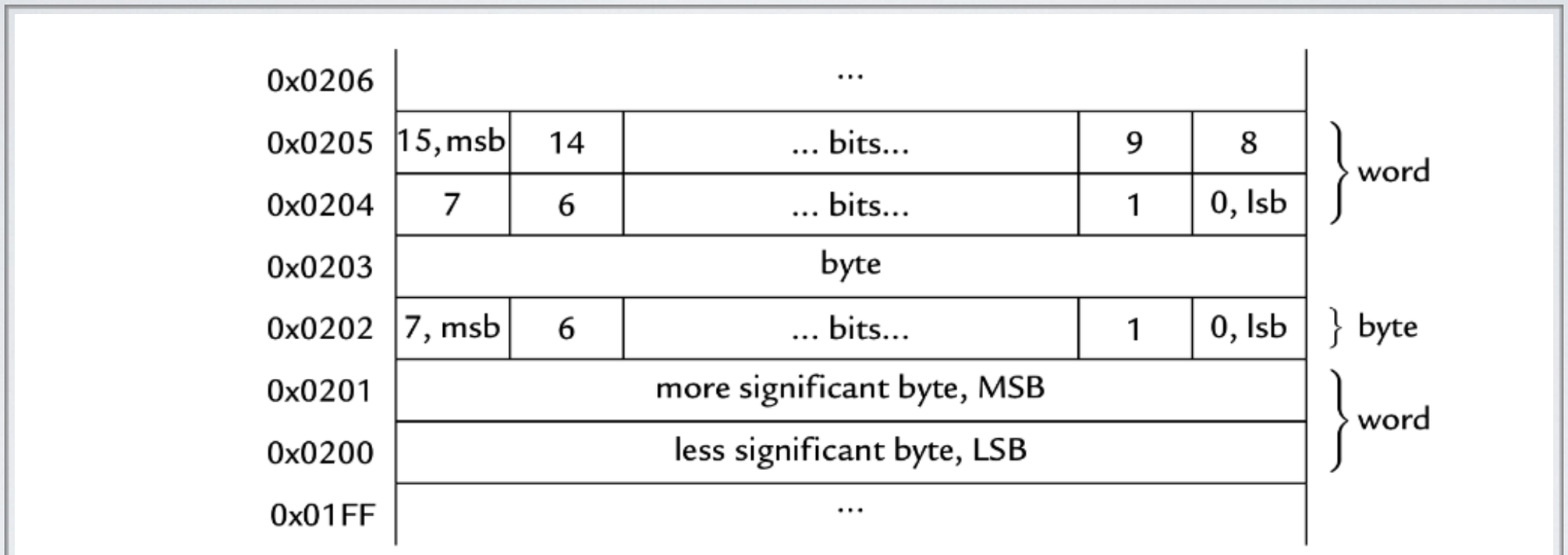


A palavra 0x1234 é armazenada no endereço 0x0200 da seguinte maneira:

0x34 em 0x0200

0x12 em 0x0201

MEMÓRIA



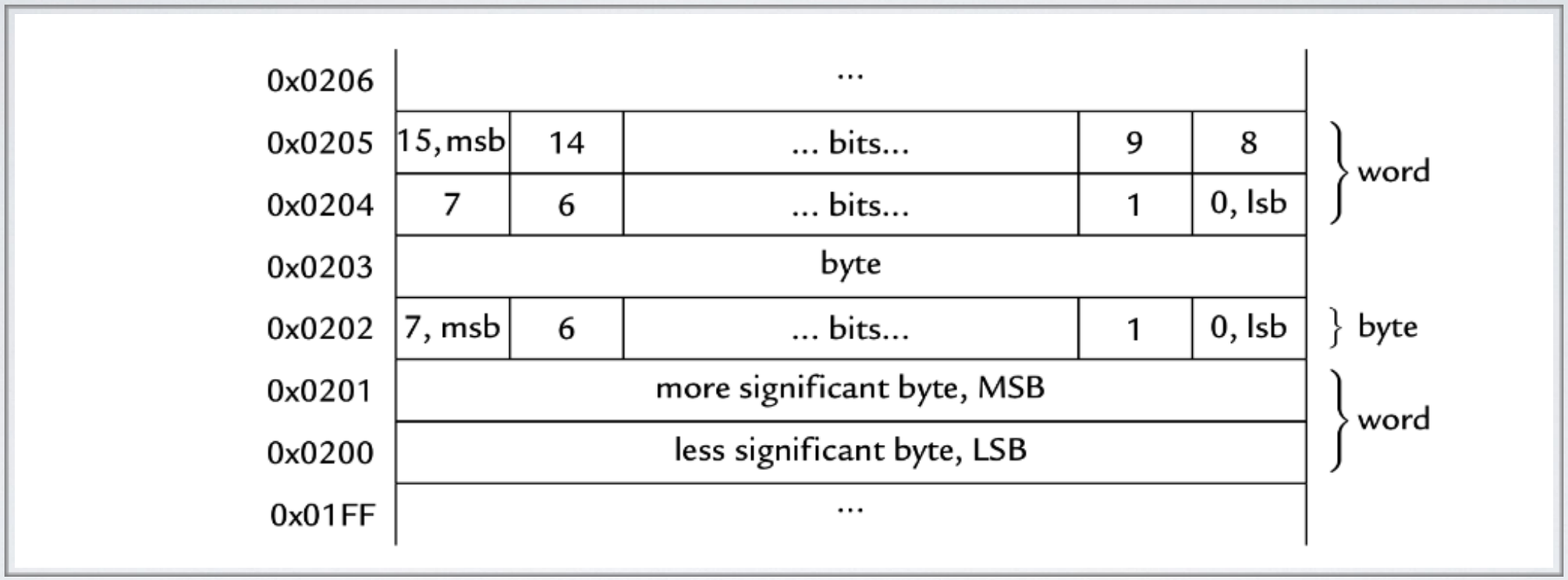
A palavra 0x1234 é armazenada no endereço 0x0200 da seguinte maneira:

0x34 em 0x0200

0x12 em 0x0201

MSP430 é Little-endian

MEMÓRIA



A palavra 0x1234 é armazenada no endereço 0x0200 da seguinte maneira:

0x34 em 0x0200

0x12 em 0x0201

O contrário chama-se Big-endian

MAPA DE MEMÓRIA

Address	Type of memory
0xFFFF	interrupt and reset
0xFFC0	vector table
0xFFBF	flash code memory
0xF800	(lower boundary varies)
0xF7FF	
0x1100	
0x10FF	flash
0x1000	information memory
0x0FFF	*bootstrap loader*
0x0C00	(*not in F20xx*)
0x0BFF	
0x0280	
0x027F	RAM
0x0200	(upper boundary varies)
0x01FF	peripheral registers
0x0100	with word access
0x00FF	peripheral registers
0x0100	with byte access
0x000F	special function registers
0x0000	(byte access)

Figure 2.4: Memory map of the MSP430F2013, based on the data sheet and the *MSP430x2xx Family User's Guide*. Addresses increase up the page and are not drawn to scale. Gray regions are unused and their size varies considerably between devices. The F2013 does not have a bootstrap loader but I have shown its location because it is present in most variants of the MSP430.

MAPA DE MEMÓRIA

Address	Type of memory
0xFFFF	interrupt and reset
0xFFC0	vector table
0xFFBF	flash code memory
0xF800	(lower boundary varies)
0xF7FF	
0x1100	
0x10FF	flash
0x1000	information memory
0x0FFF	*bootstrap loader*
0x0C00	(*not in F20xx*)
0x0BFF	
0x0280	
0x027F	RAM
0x0200	(upper boundary varies)
0x01FF	peripheral registers
0x0100	with word access
0x00FF	peripheral registers
0x0100	with byte access
0x000F	special function registers
0x0000	(byte access)

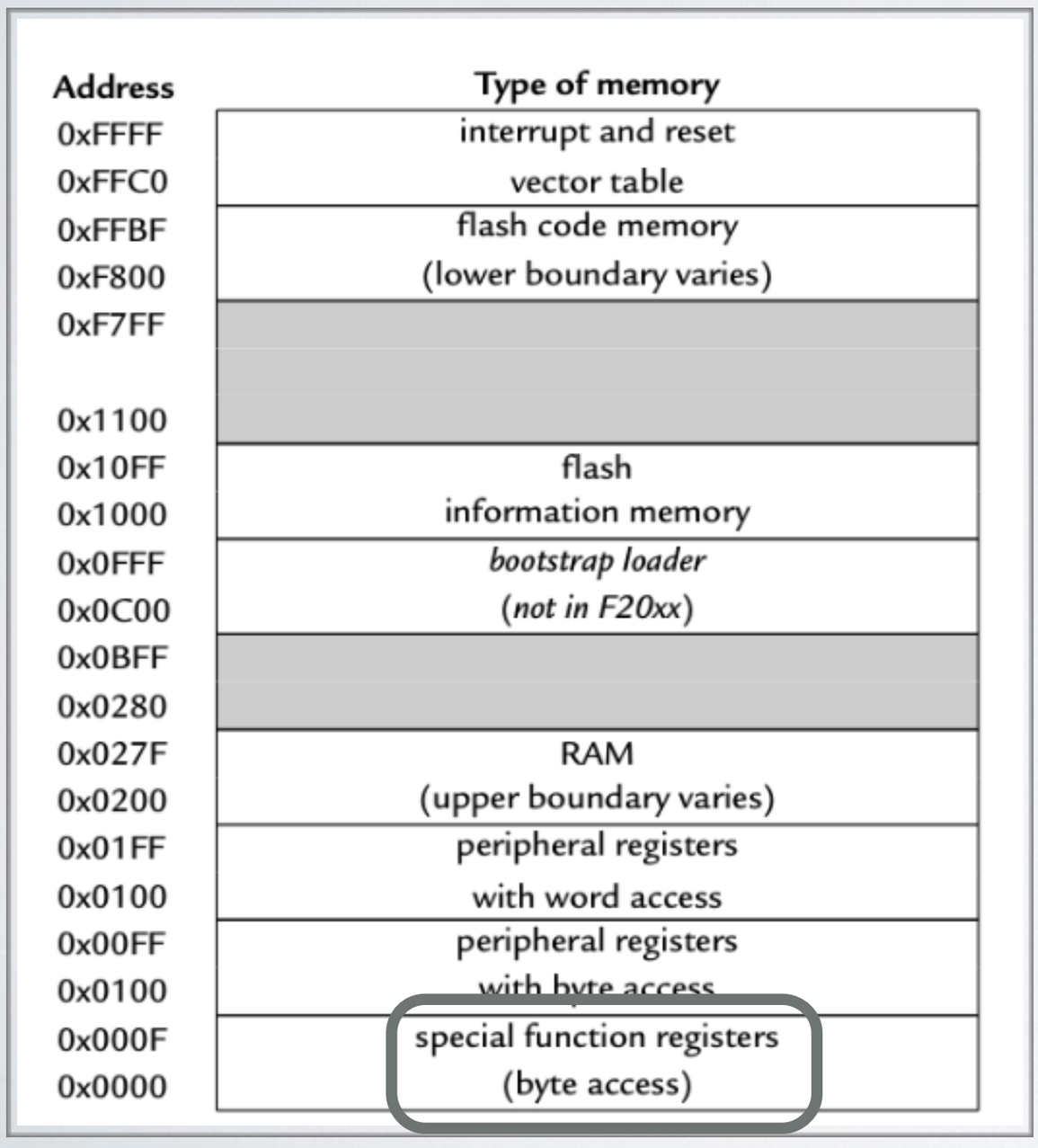
Mapas de memória variam de acordo com os modelos do MSP430, mudando o tamanho da RAM e do espaço para código

MAPA DE MEMÓRIA

Address	Type of memory
0xFFFF	interrupt and reset
0xFFC0	vector table
0xFFBF	flash code memory
0xF800	(lower boundary varies)
0xF7FF	
0x1100	
0x10FF	flash
0x1000	information memory
0x0FFF	*bootstrap loader*
0x0C00	(*not in F20xx*)
0x0BFF	
0x0280	
0x027F	RAM
0x0200	(upper boundary varies)
0x01FF	peripheral registers
0x0100	with word access
0x00FF	peripheral registers
0x0100	with byte access
0x000F	special function registers
0x0000	(byte access)

Certas partes não são utilizadas (em cor cinza na figura ao lado)

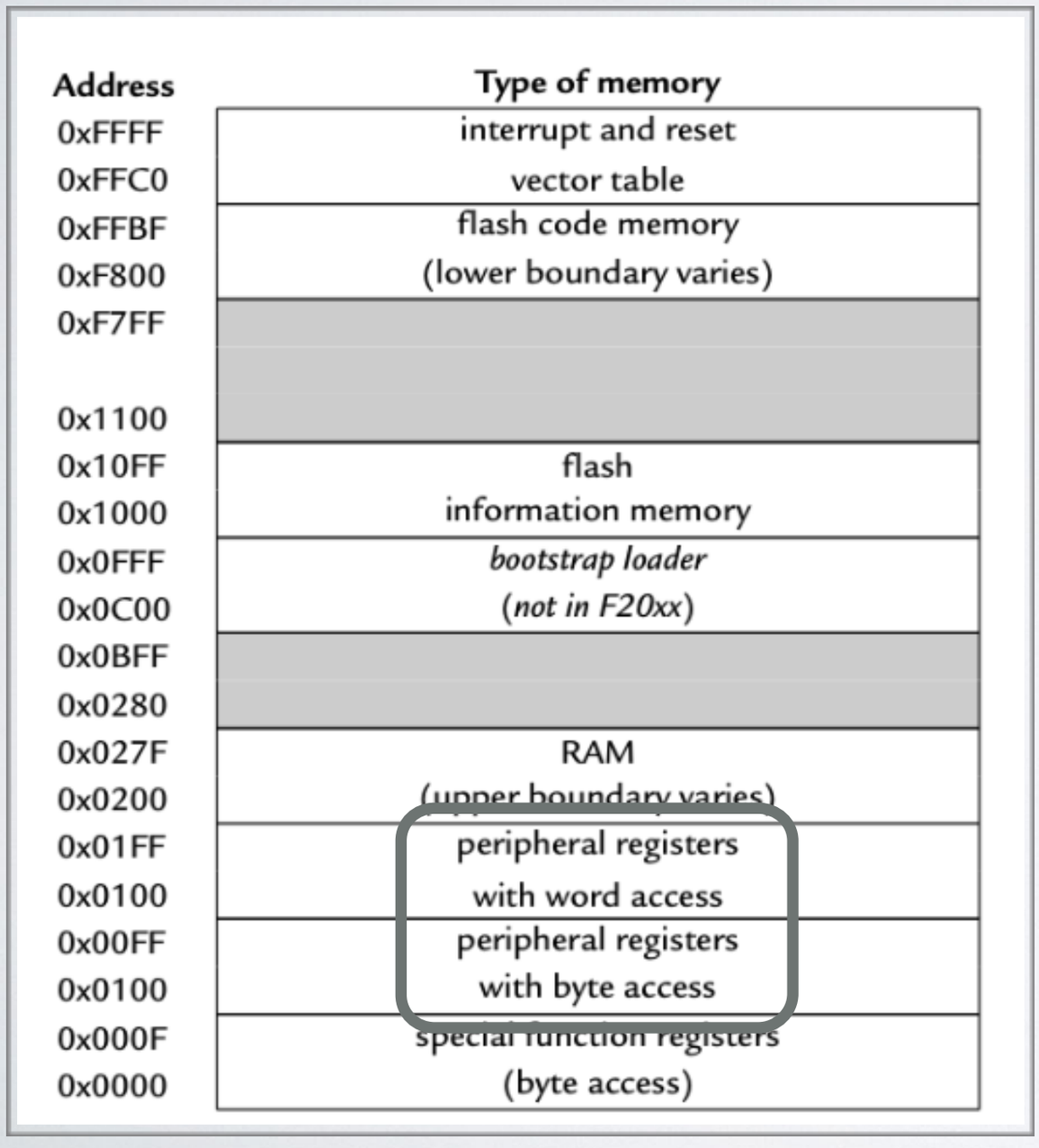
MAPA DE MEMÓRIA



Habilitam funções de alguns módulos

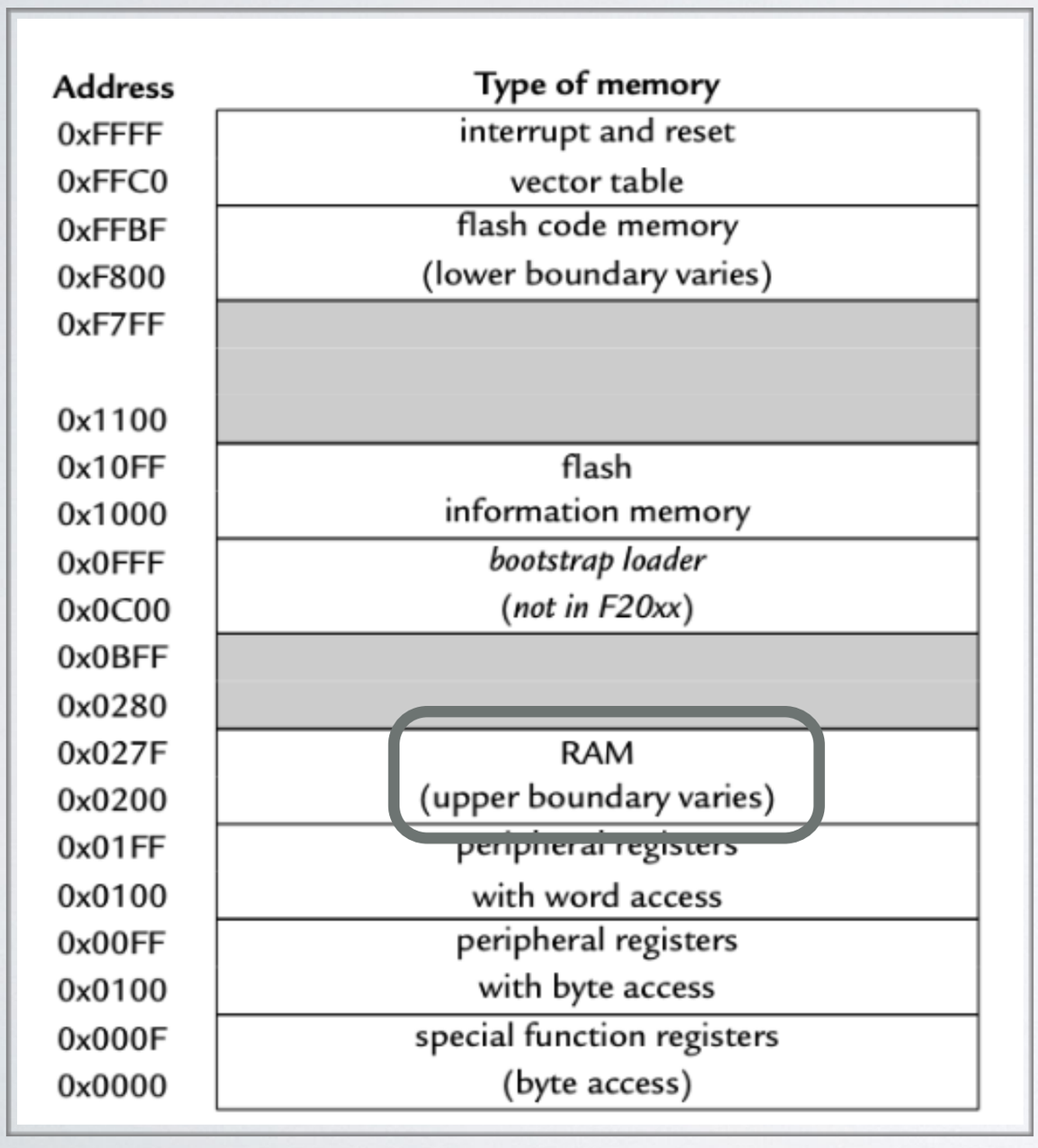
Habilitam e sinalizam interrupções dos periféricos

MAPA DE MEMÓRIA



Comunicação entre CPU e periféricos

MAPA DE MEMÓRIA

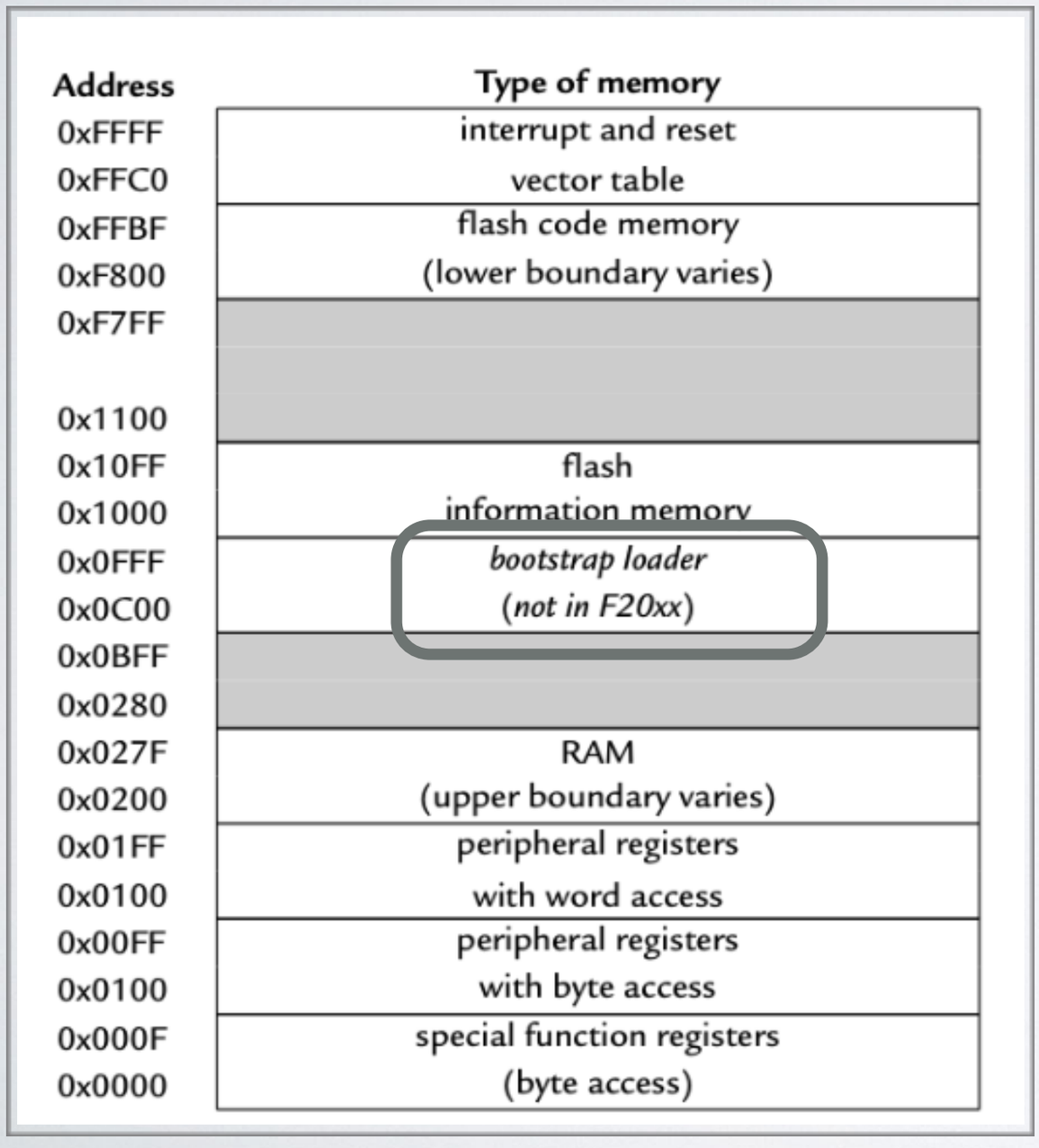


Usada para variáveis

Começam em 0x0200

O fim da RAM depende do modelo de MSP430

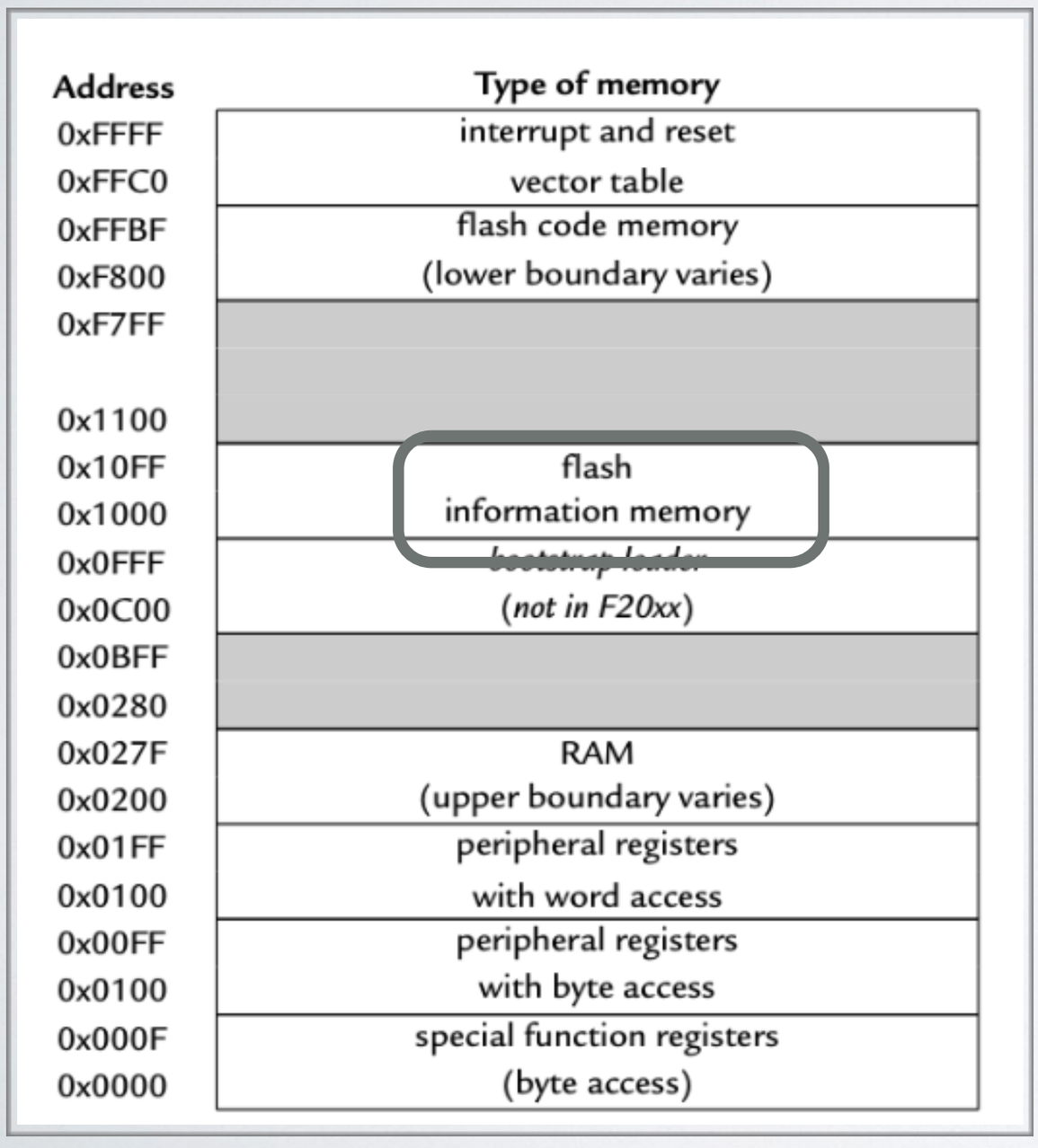
MAPA DE MEMÓRIA



Programa para comunicar usando o protocolo serial padrão (RS232)

Não é tão importante hoje em dia, devido à porta USB

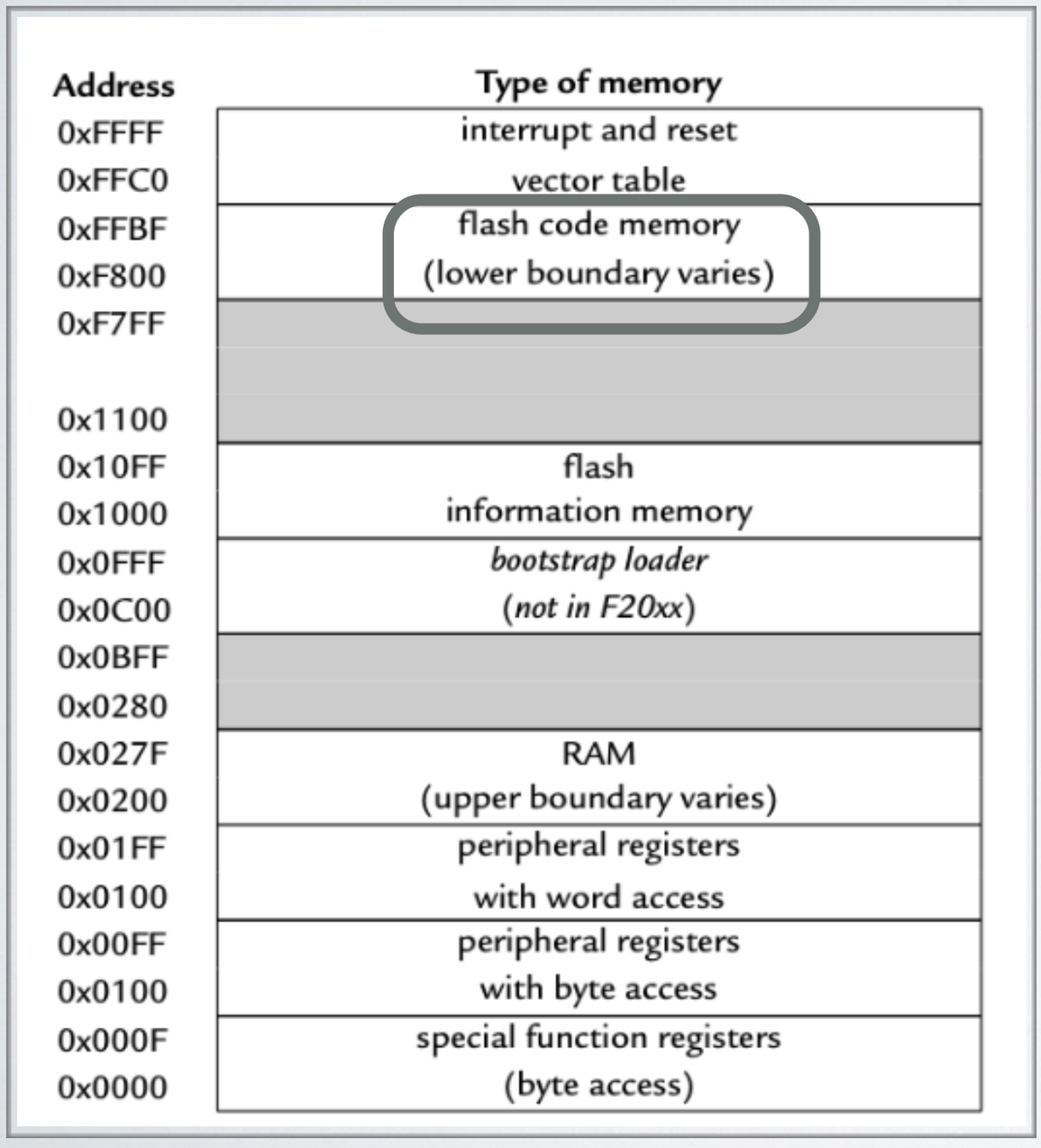
MAPA DE MEMÓRIA



256 bytes para memória não-volátil

Números de série, configurações da última vez em que o sistema foi usado etc.

MAPA DE MEMÓRIA



Programa

O endereço menor depende do modelo de MSP430

MAPA DE MEMÓRIA

Address	Type of memory
0xFFFF	interrupt and reset
0xFFC0	vector table
0xFFBF	flash code memory
0xF800	(lower boundary varies)
0xF7FF	
0x1100	
0x10FF	flash
0x1000	information memory
0x0FFF	*bootstrap loader*
0x0C00	(*not in F20xx*)
0x0BFF	
0x0280	
0x027F	RAM
0x0200	(upper boundary varies)
0x01FF	peripheral registers
0x0100	with word access
0x00FF	peripheral registers
0x0100	with byte access
0x000F	special function registers
0x0000	(byte access)

Lida com interrupções

CPU

15	... bits ...	0
R0/PC	program counter	0
R1/SP	stack pointer	0
R2/SR/CG1	status register	
R3/CG2	constant generator	
R4	general purpose	
⋮		
R15	general purpose	

Figure 2.5: Registers in the CPU of the MSP430.

CPU

15	... bits ...	0
R0/PC	program counter	0
R1/SP	stack pointer	0
R2/SR/CG1	status register	
R3/CG2	constant generator	
R4	general purpose	
⋮		
R15	general purpose	

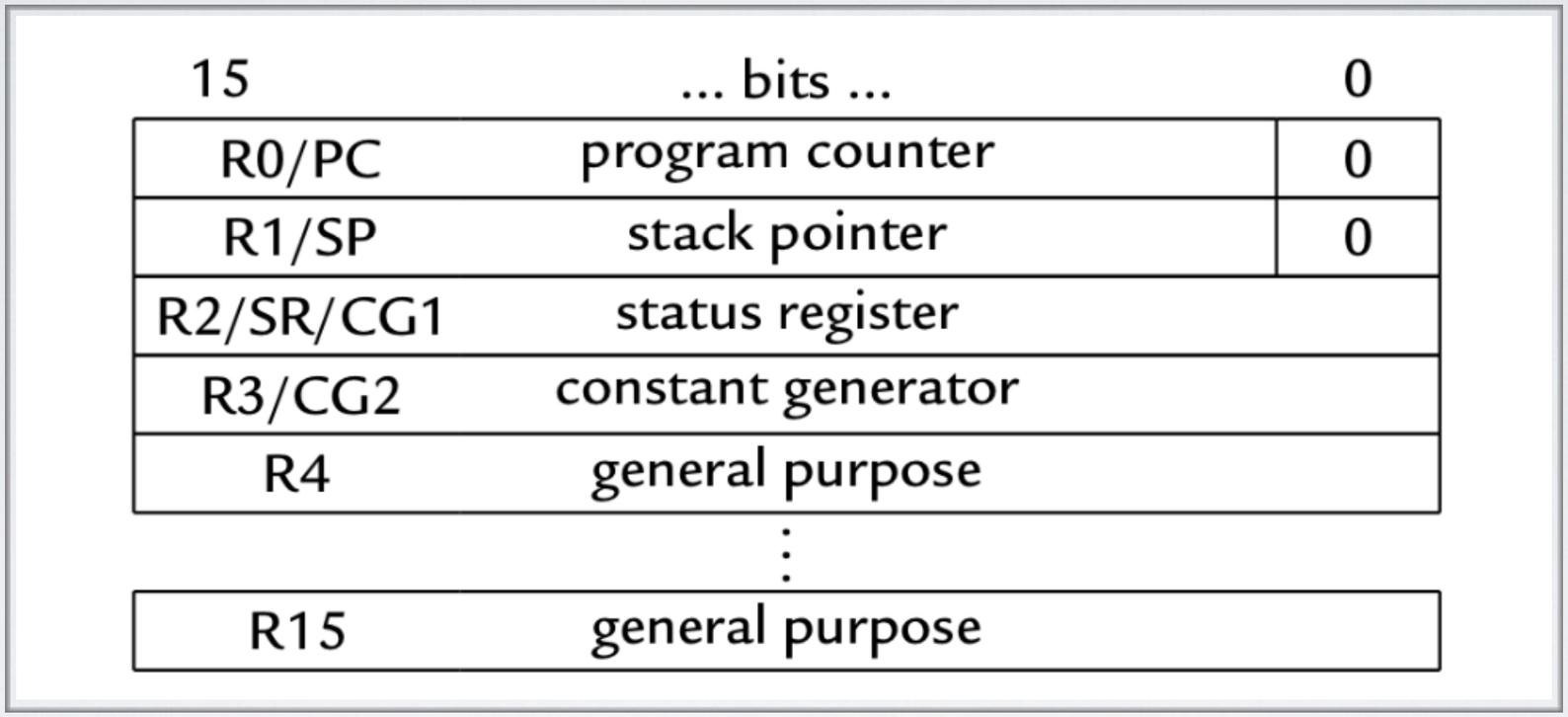
Executa instruções, faz bifurcações por software e por hardware

CPU

15	... bits ...	0
R0/PC	program counter	0
R1/SP	stack pointer	0
R2/SR/CG1	status register	
R3/CG2	constant generator	
R4	general purpose	
⋮		
R15	general purpose	

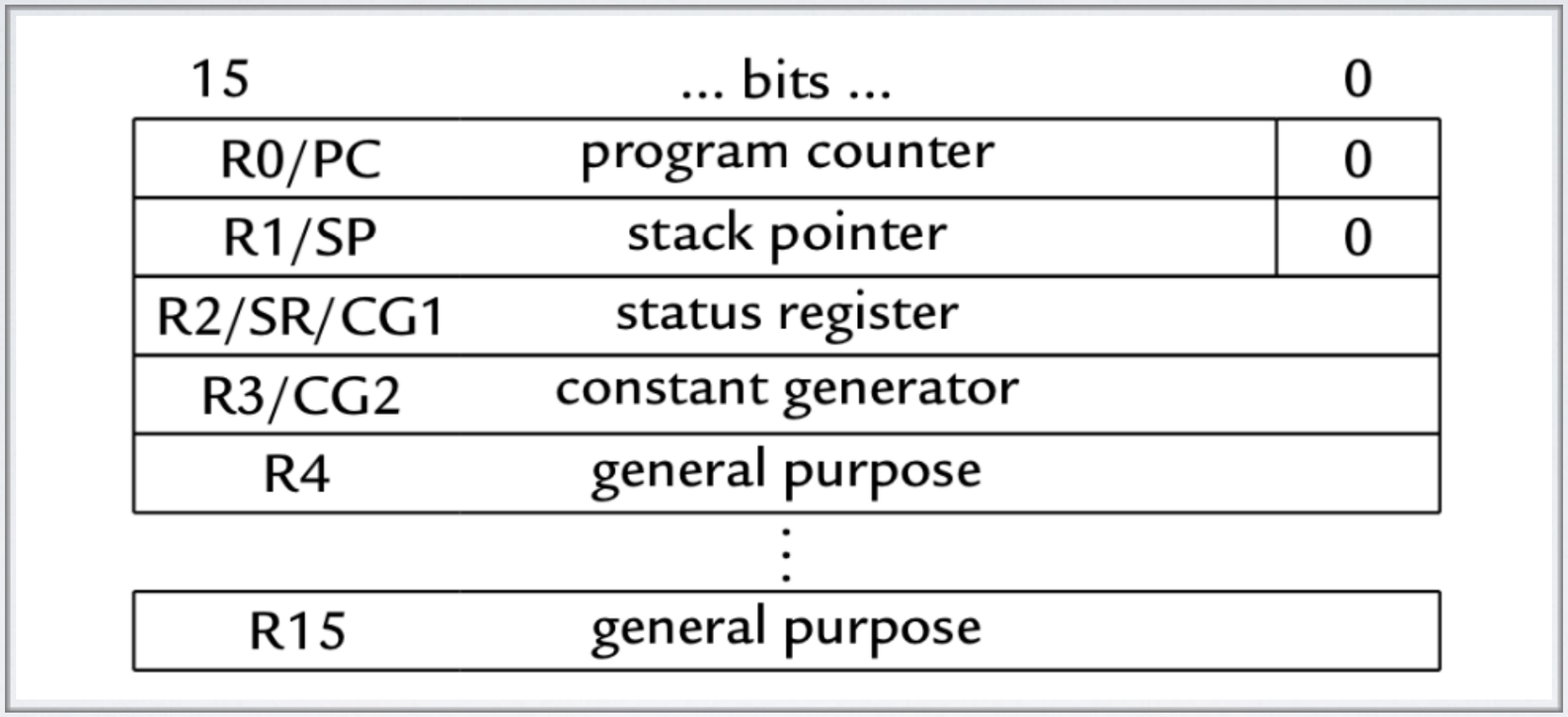
Possui uma unidade lógico-aritmética (ULA), 16 registradores e a lógica de decodificação das instruções

CPU



Roda em uma frequência máxima de 16MHz para os MSP430F2xxx e alguns MSP430x4xx, 8MHz para os demais

CPU



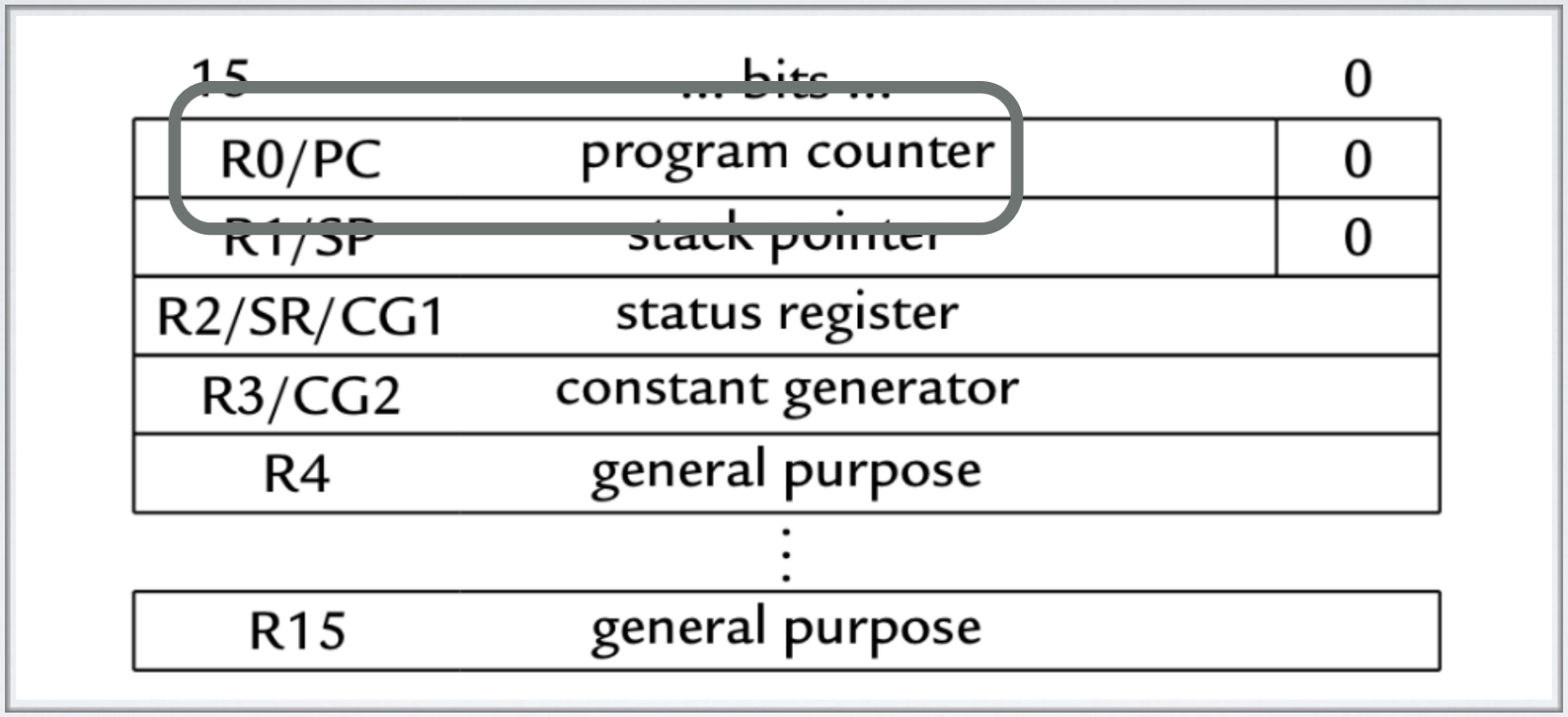
Possui lógica estática: não possui uma frequência mínima de operação, e seu estado não é perdido quando pára de funcionar

CPU

15	... bits ...	0
R0/PC	program counter	0
R1/SP	stack pointer	0
R2/SR/CG1	status register	
R3/CG2	constant generator	
R4	general purpose	
⋮		
R15	general purpose	

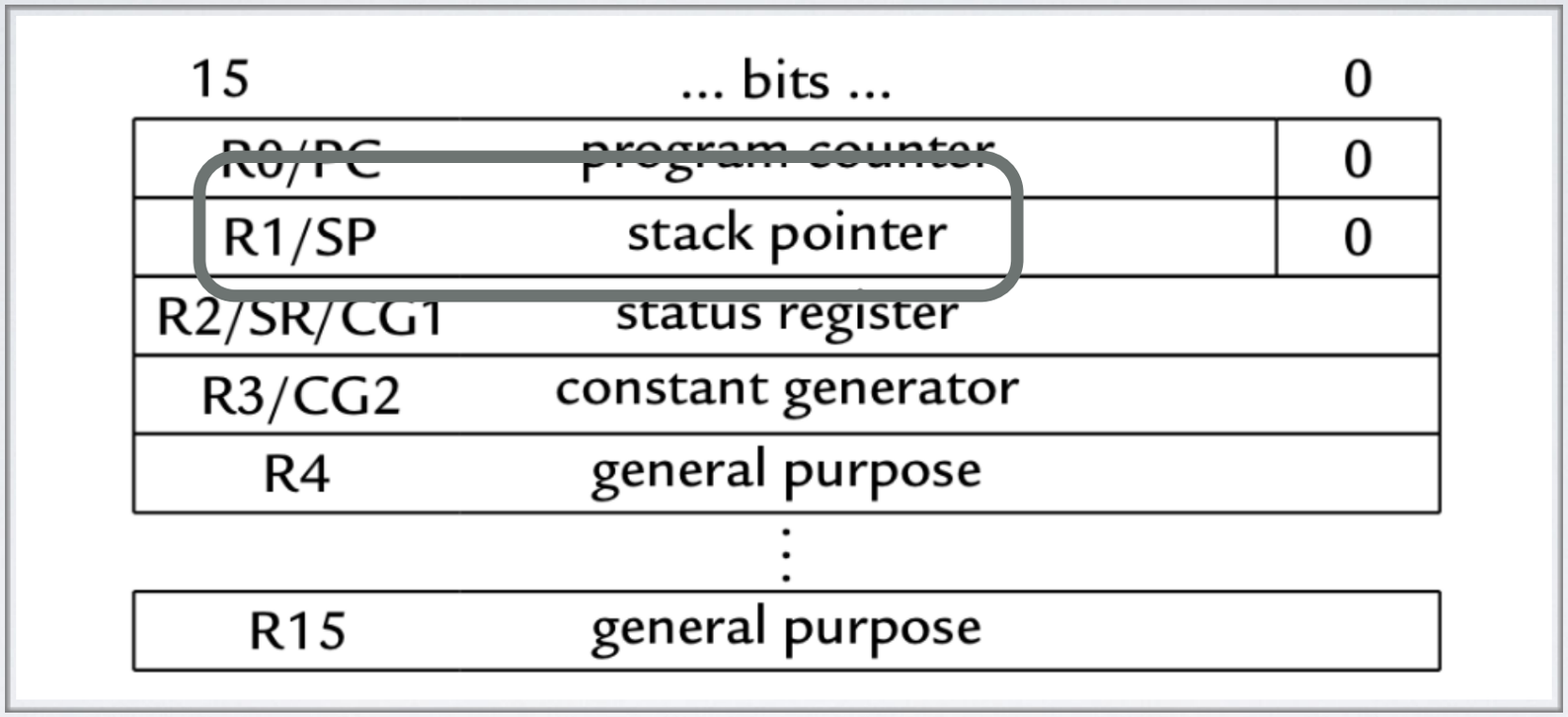
Registradores não estão na memória principal, e sim na CPU (diferente de alguns processadores)

CPU



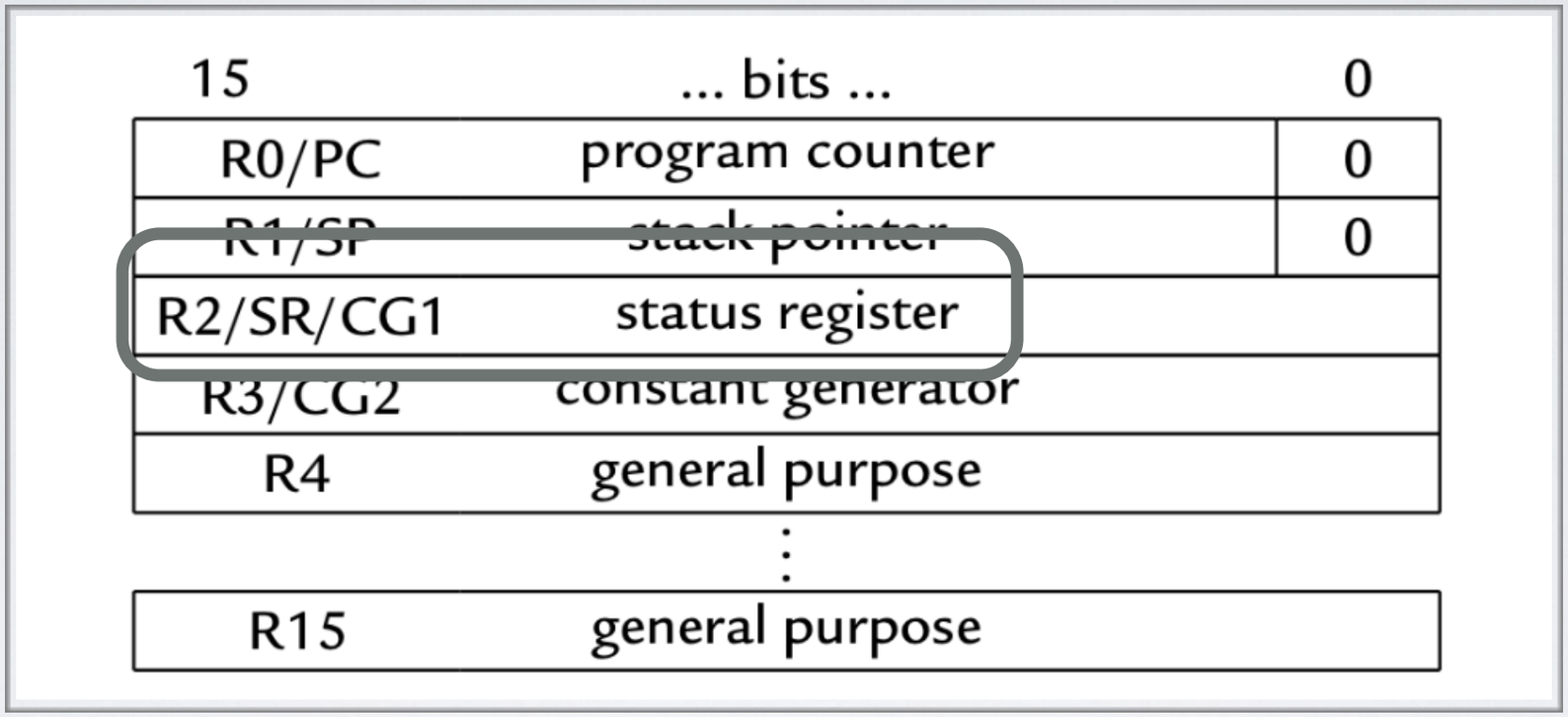
Aponta para o endereço da próxima instrução a ser executada

CPU



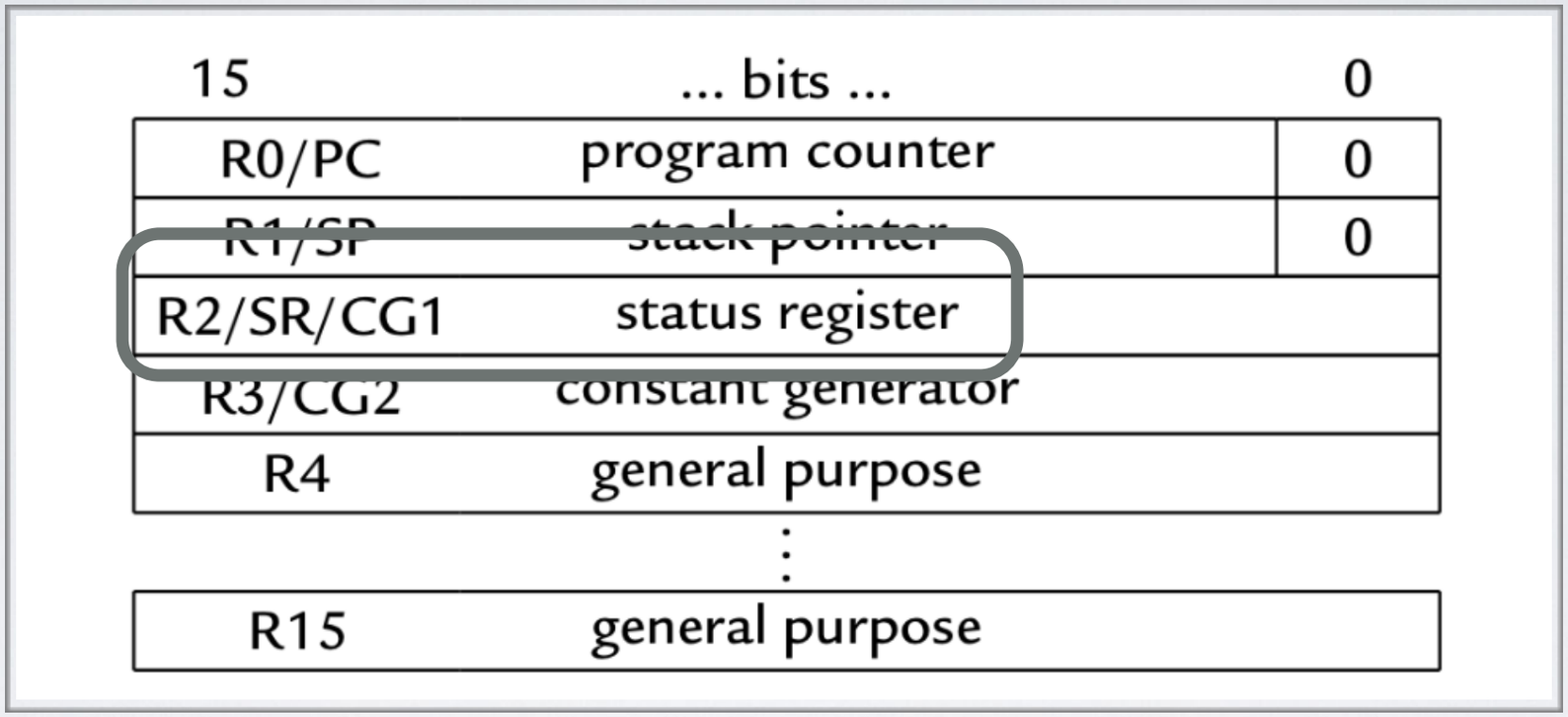
Aponta para o menor endereço da pilha, que guarda informações importantes quando se chama uma subrotina, como o endereço de retorno para o PC

CPU



Flags (bits) de estado C, Z, N, V, GIE, CPUOFF, OSCOFF, SCG0 e SCG1

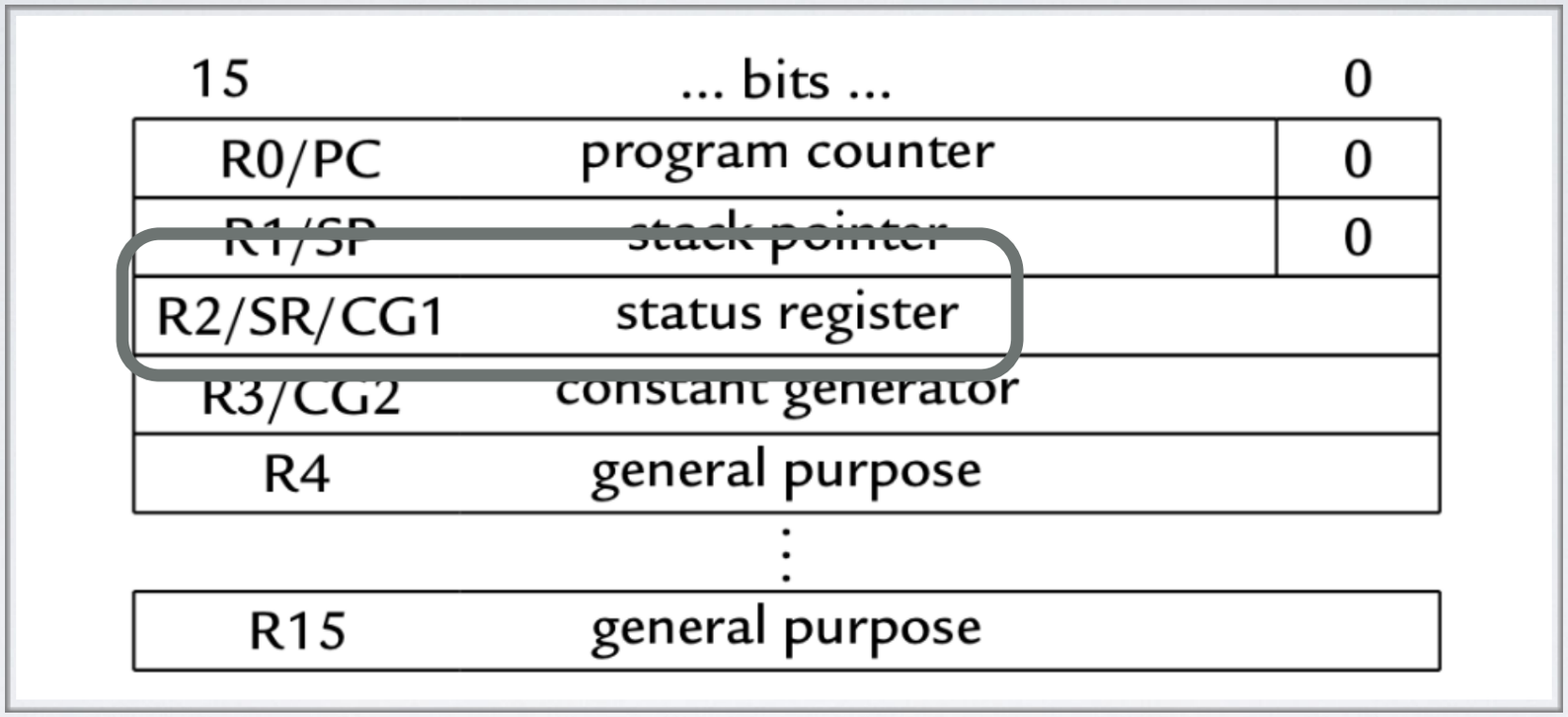
CPU



Flags (bits) de estado

Z: 1 quando a última operação resultou em zero

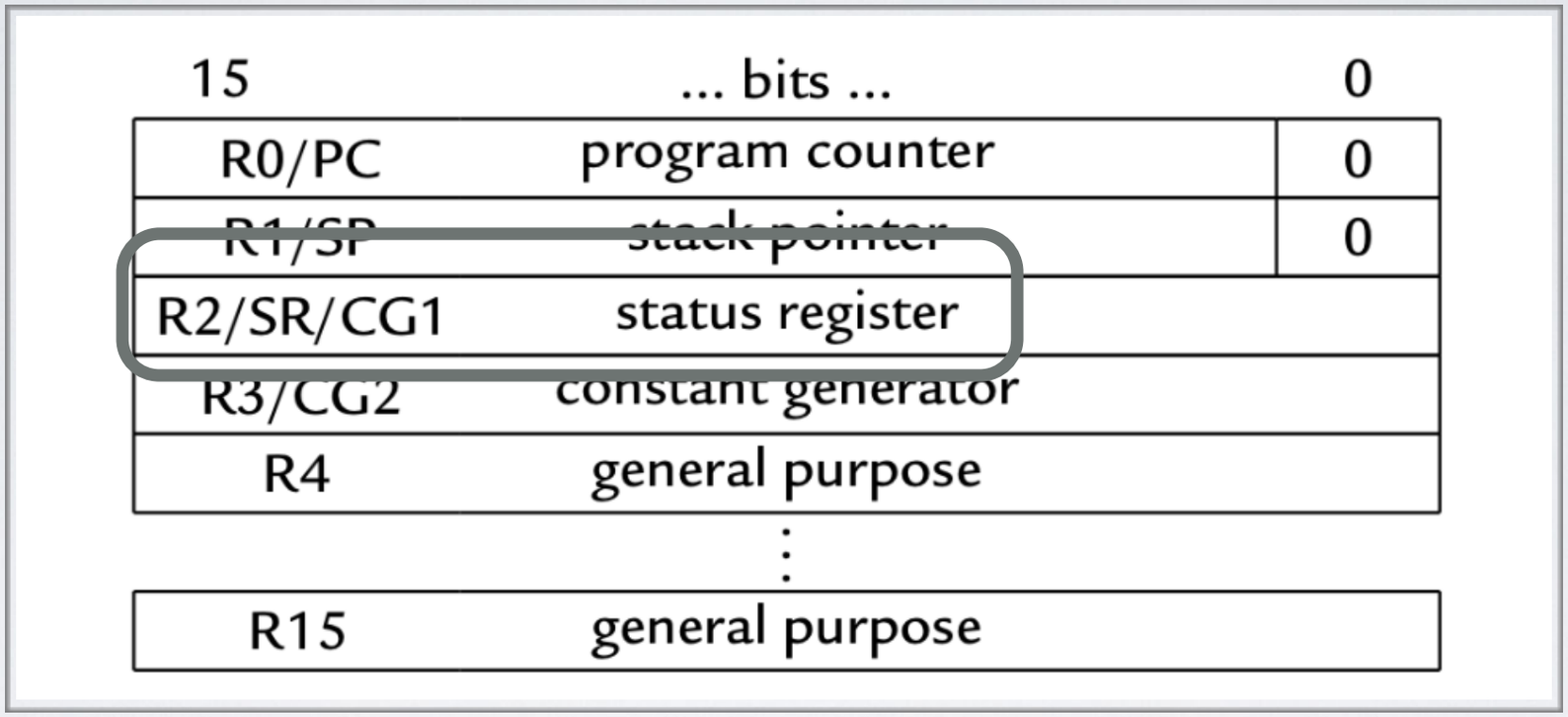
CPU



Flags (bits) de estado

GIE: habilita interrupções mascaráveis

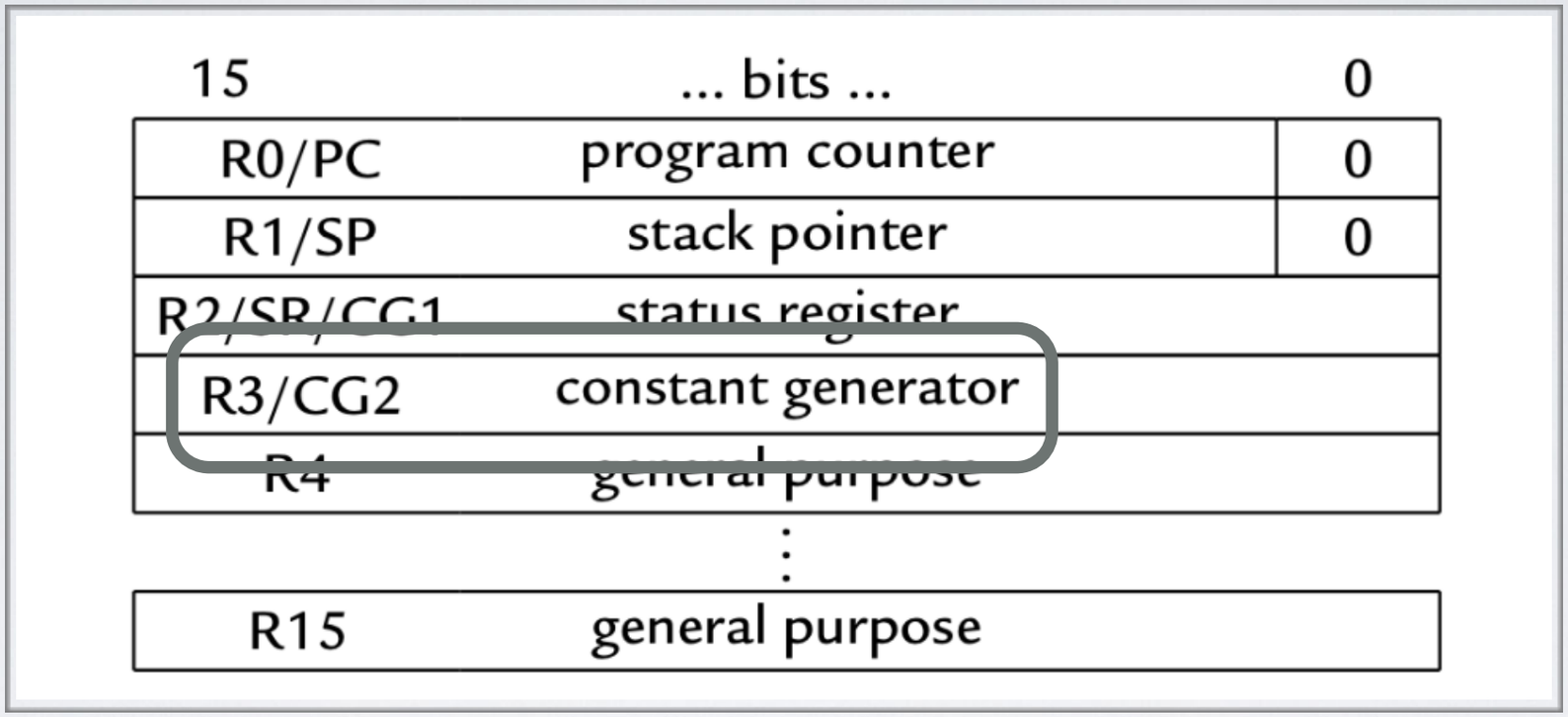
CPU



Flags (bits) de estado

CPUOFF, OSCOFF, SCG0 e SCG1: controlam o modo de operação do MSP430

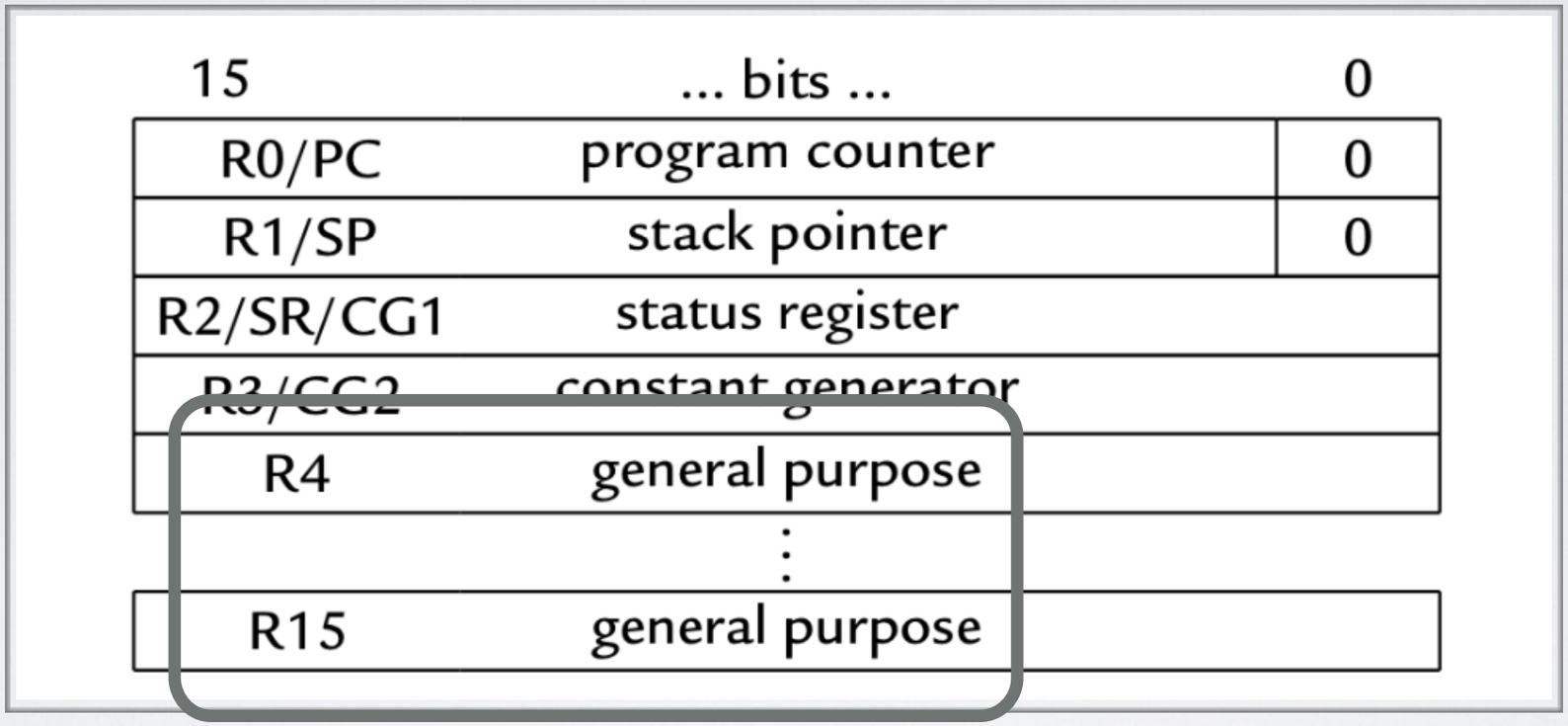
CPU



Fornece os 6 valores mais utilizados

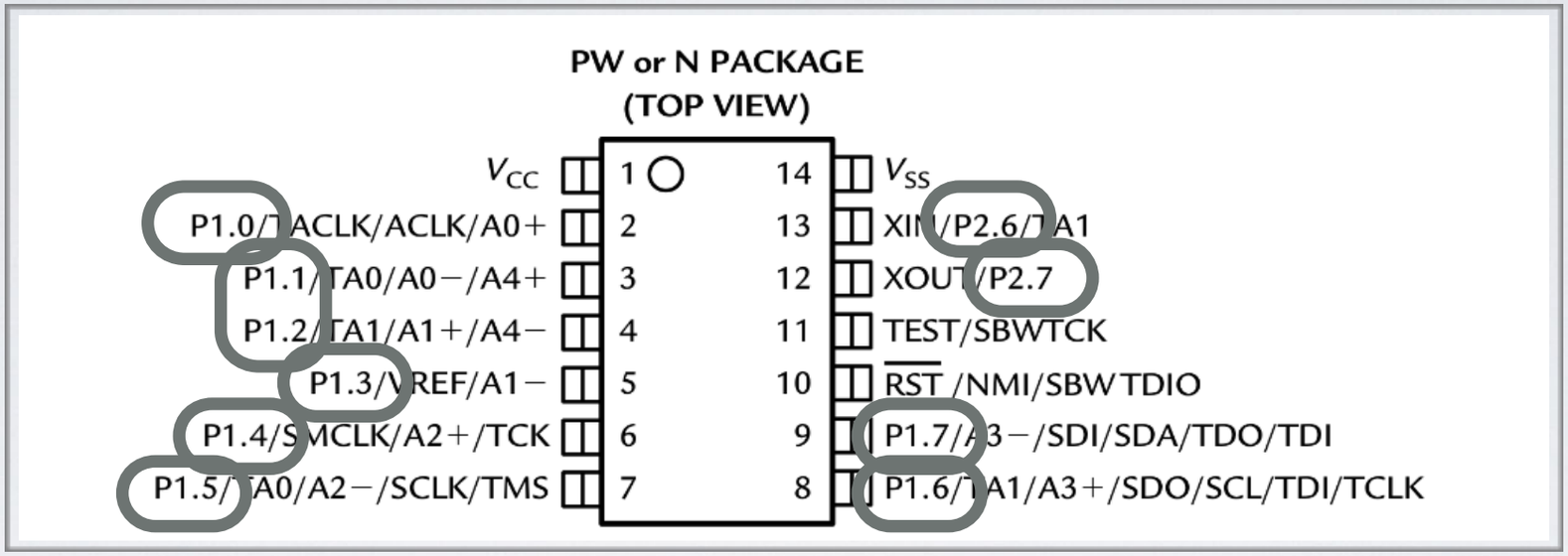
O compilador e o montador se encarregam dos detalhes

CPU



Uso geral

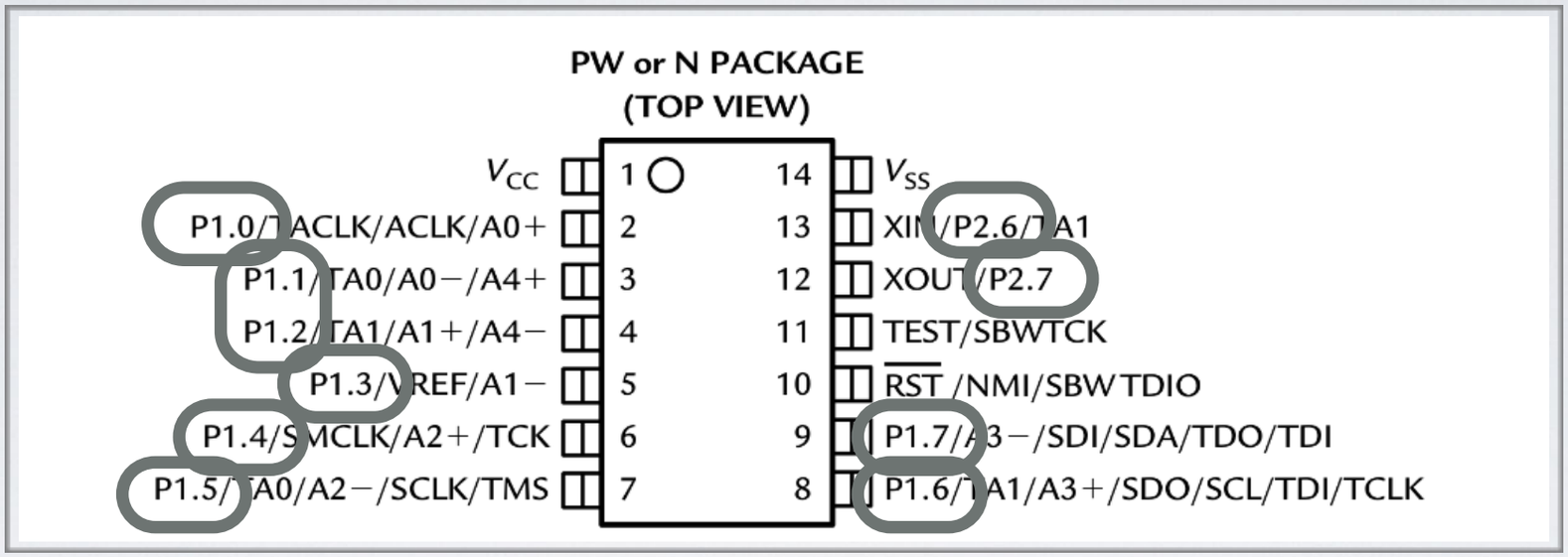
DIGITAL I/O MAPPING



P1.0-P1.7 e P2.6-P2.7 são entradas e saídas digitais

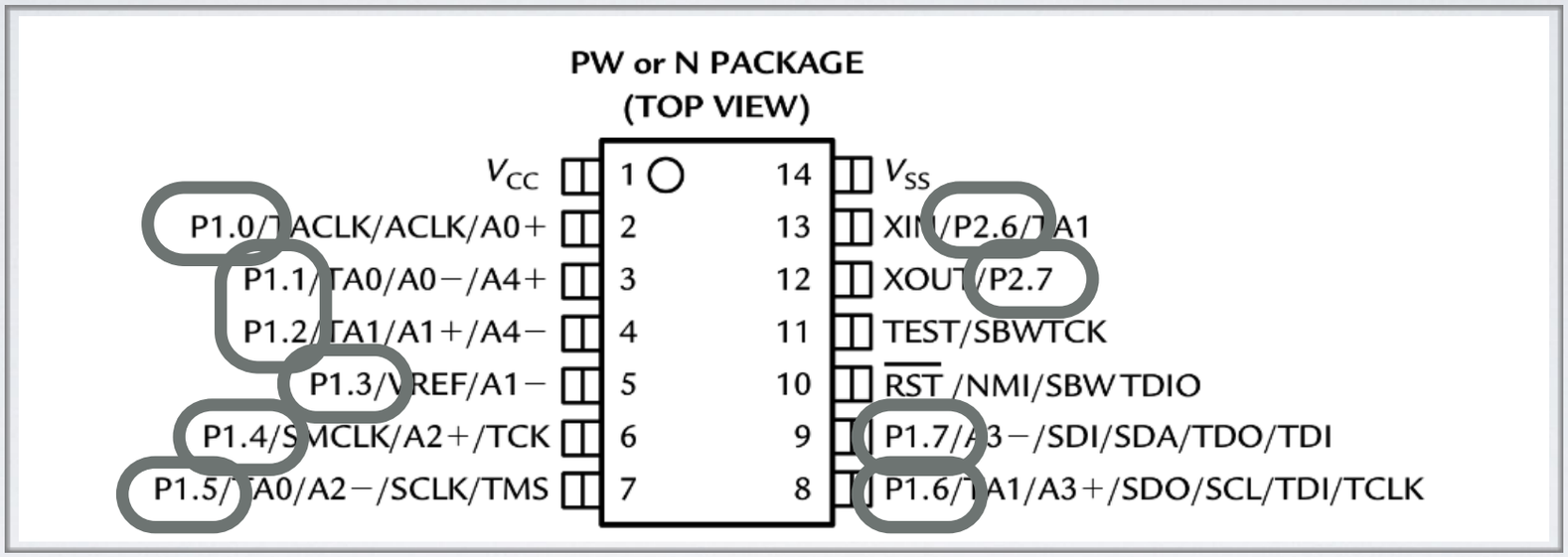
Alguns desses pinos podem interromper o sistema

DIGITAL I/O MAPPING



O processador do MSP430
enxerga essas portas através de
registradores periféricos
(endereços na memória)

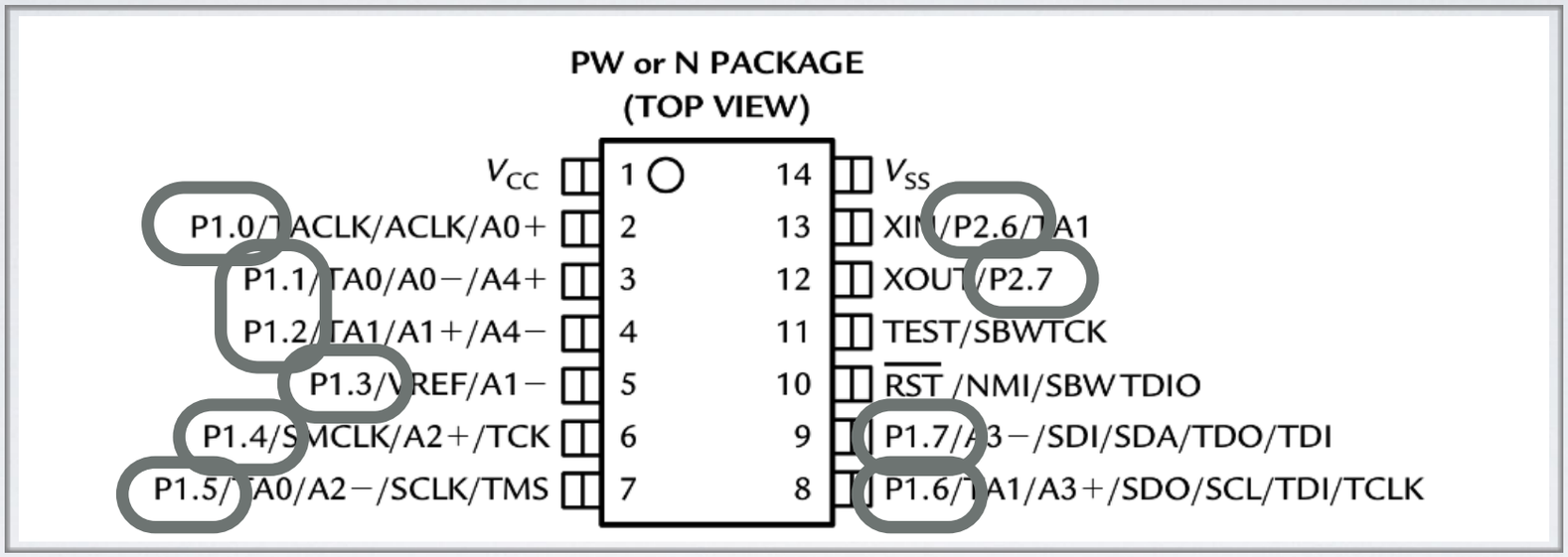
DIGITAL I/O MAPPING



Cada porta ==> um byte

Cada pino ==> um bit de cada byte

DIGITAL I/O MAPPING

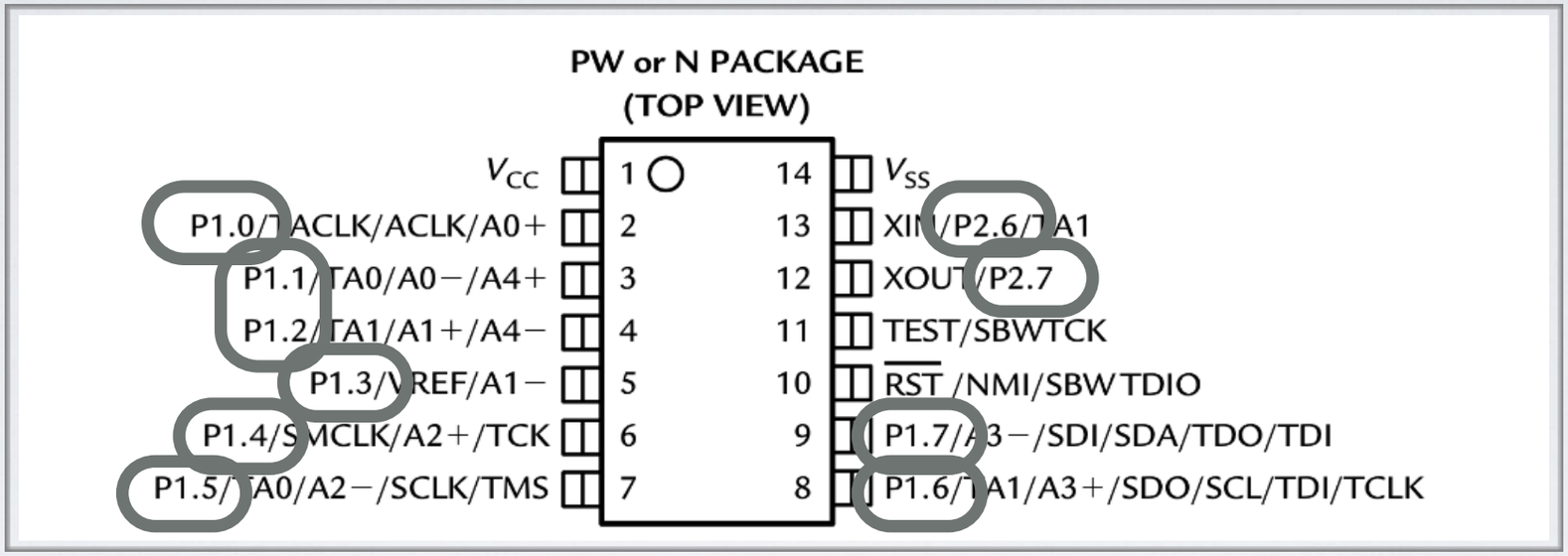


Por exemplo, P1IN apresenta os valores de entrada na porta P1

Pino em Vss ==> bit correspondente = 0

Pino em Vcc ==> bit correspondente = 1

DIGITAL I/O MAPPING

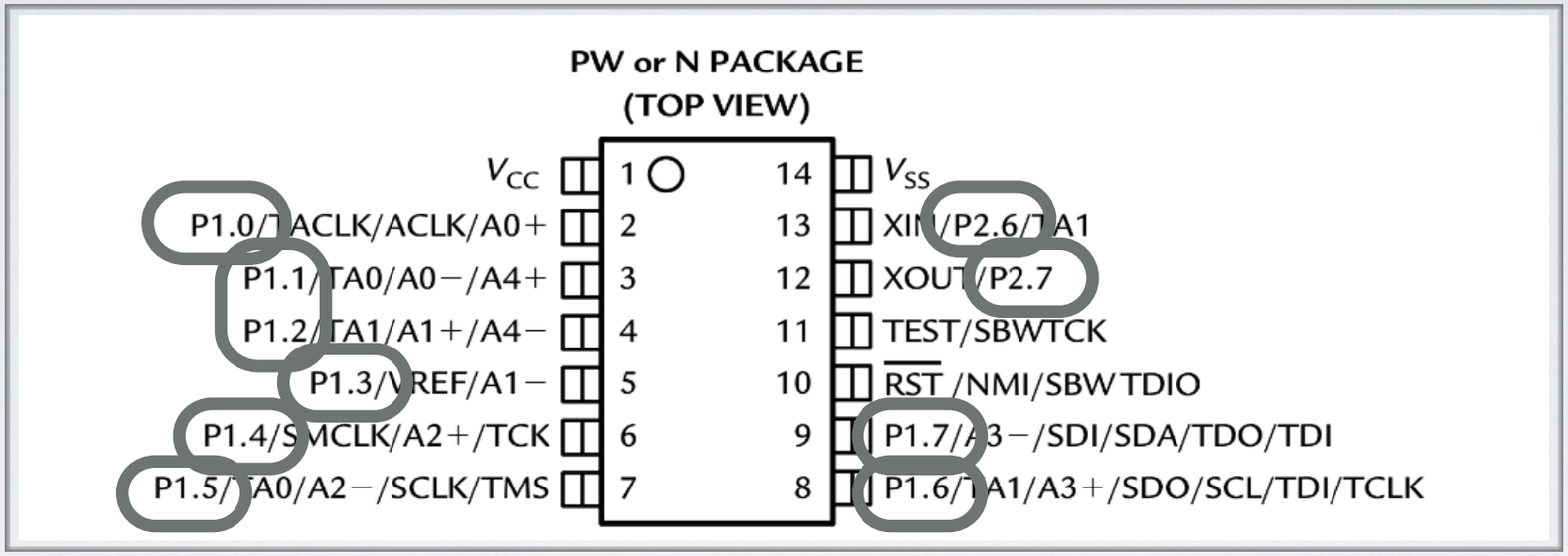


Por exemplo, P2OUT apresenta os valores de entrada na porta P2

Bit correspondente = 0 ==> Pino em Vss

Bit correspondente = 1 ==> Pino em Vcc

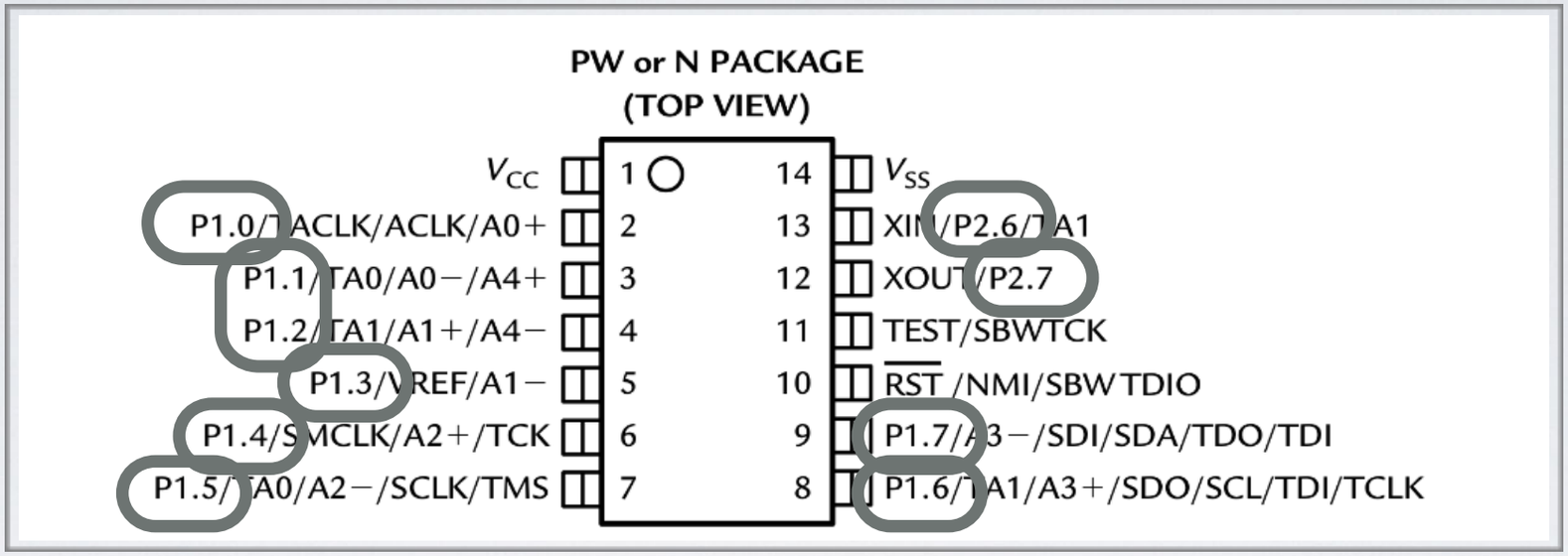
DIGITAL I/O MAPPING



Registradores mais importantes para a porta P1

P1IN: registrador volátil read-only com os valores de entrada

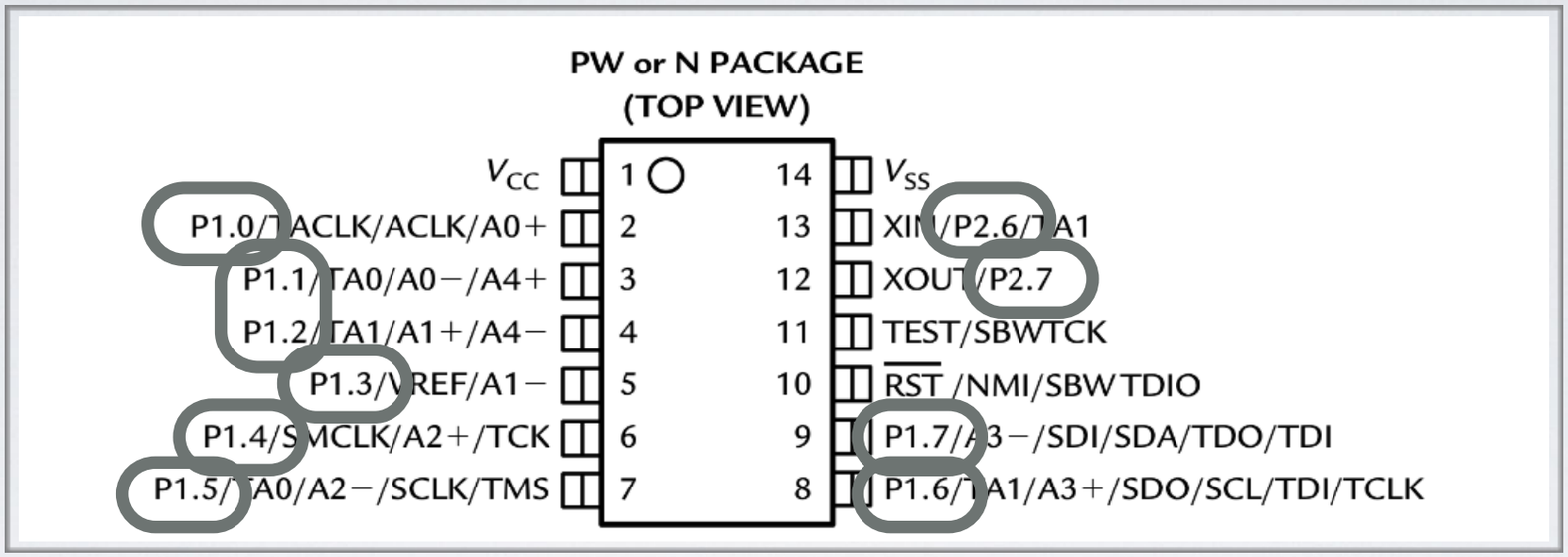
DIGITAL I/O MAPPING



Registradores mais importantes para a porta P1

P1OUT: escrever neste registrador leva o pino de saída a Vss ou Vcc, se o pino for configurado como saída. Caso contrário, o valor correspondente é guardado num buffer e aparece no pino quando este for configurado como saída

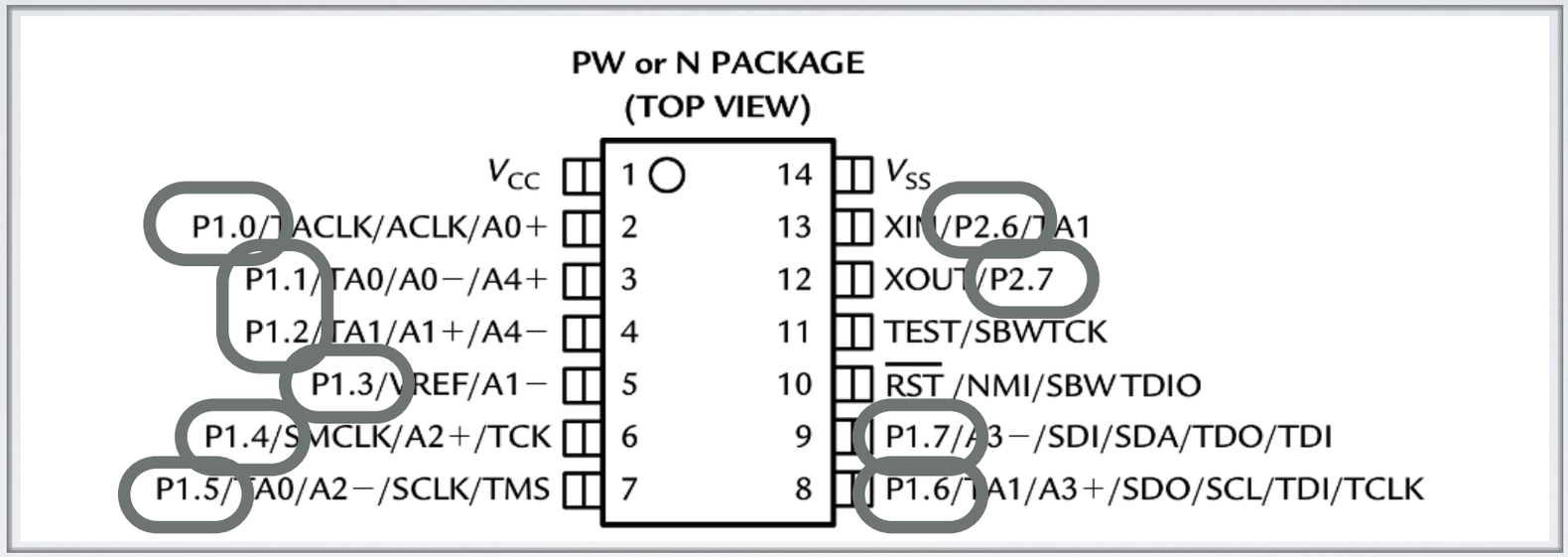
DIGITAL I/O MAPPING



Registradores mais importantes para a porta P1

P1DIR: define se o pino é de entrada (bit correspondente = 0) ou de saída (bit correspondente = 1)

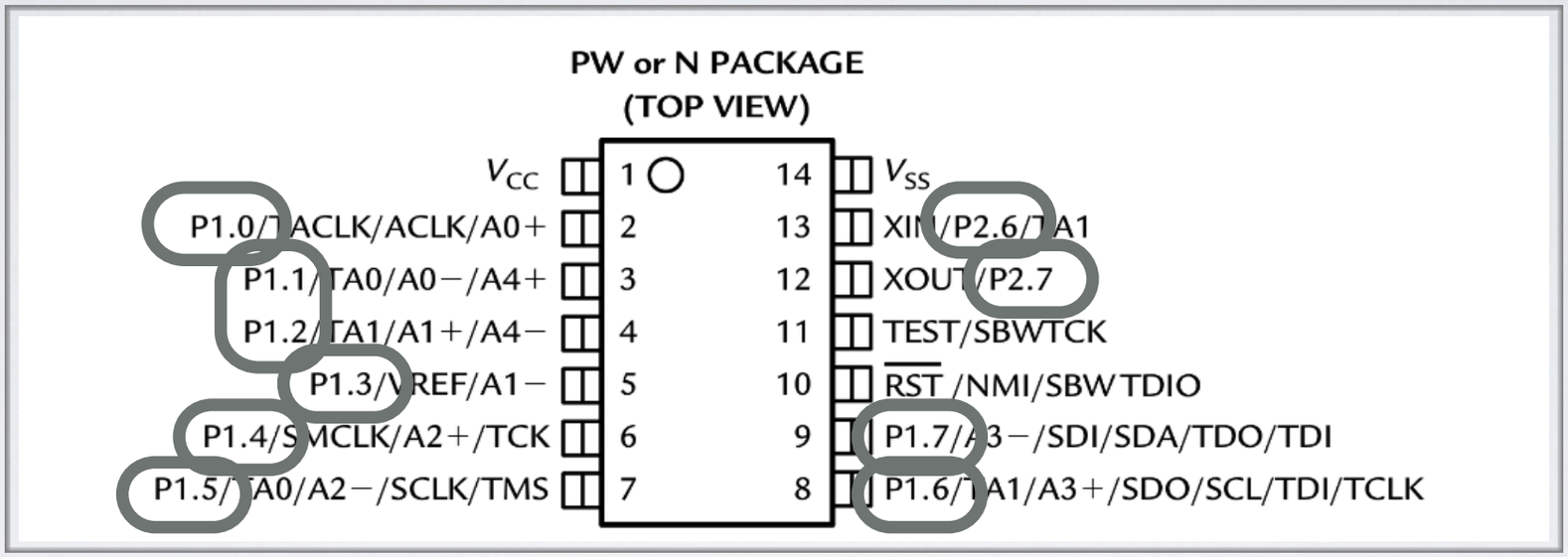
DIGITAL I/O MAPPING



Exemplo: configurar em C todos os pinos da porta P1 como saída e levá-los para Vcc

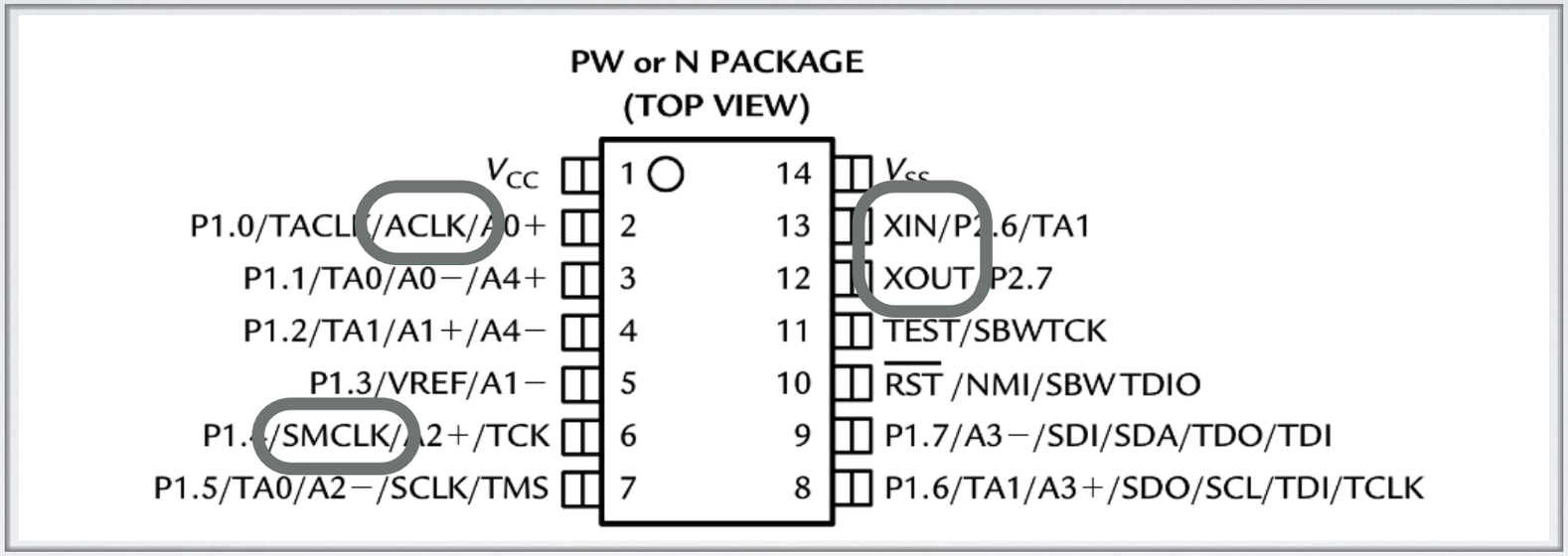
```
P1DIR = 0xFF;
P1OUT = 0xFF;
```

DIGITAL I/O MAPPING



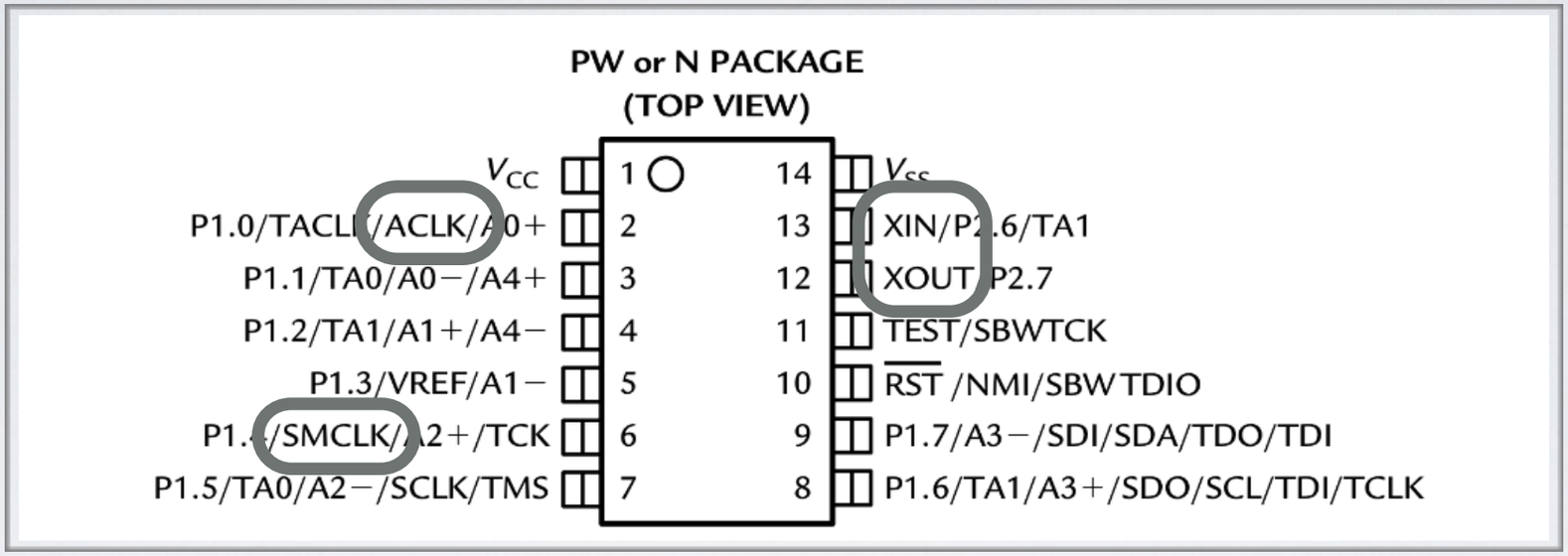
Outros periféricos do MSP430 são controlados por registradores semelhantes

GERADOR DE CLOCK



Sinal de clock é uma onda quadrada cujas bordas acionam diferentes hardwares de forma sincronizada

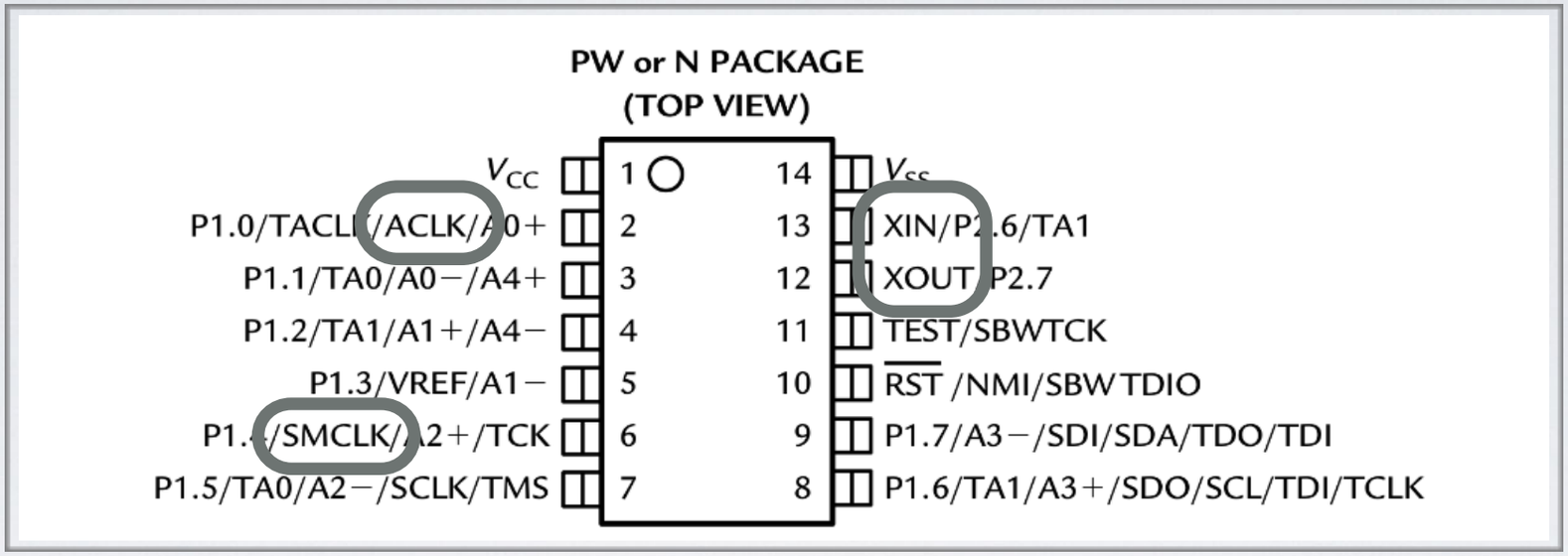
GERADOR DE CLOCK



Para trabalhar com baixo consumo de energia,
o MSP430 necessita de 2 clocks

Um clock rápido e pouco preciso para a CPU,
que possa ser parado e reiniciado rapidamente

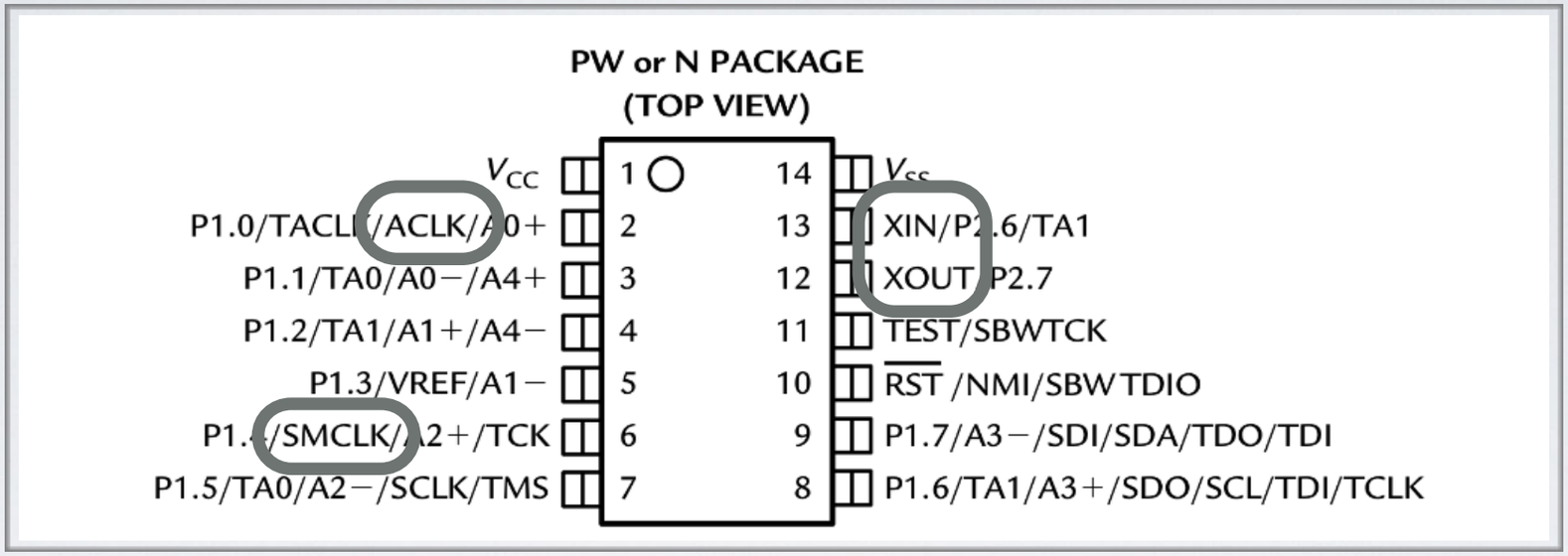
GERADOR DE CLOCK



Para trabalhar com baixo consumo de energia, o MSP430 necessita de 2 clocks

Um clock lento, de baixo consumo, preciso e que nunca pare, para monitorar o tempo real

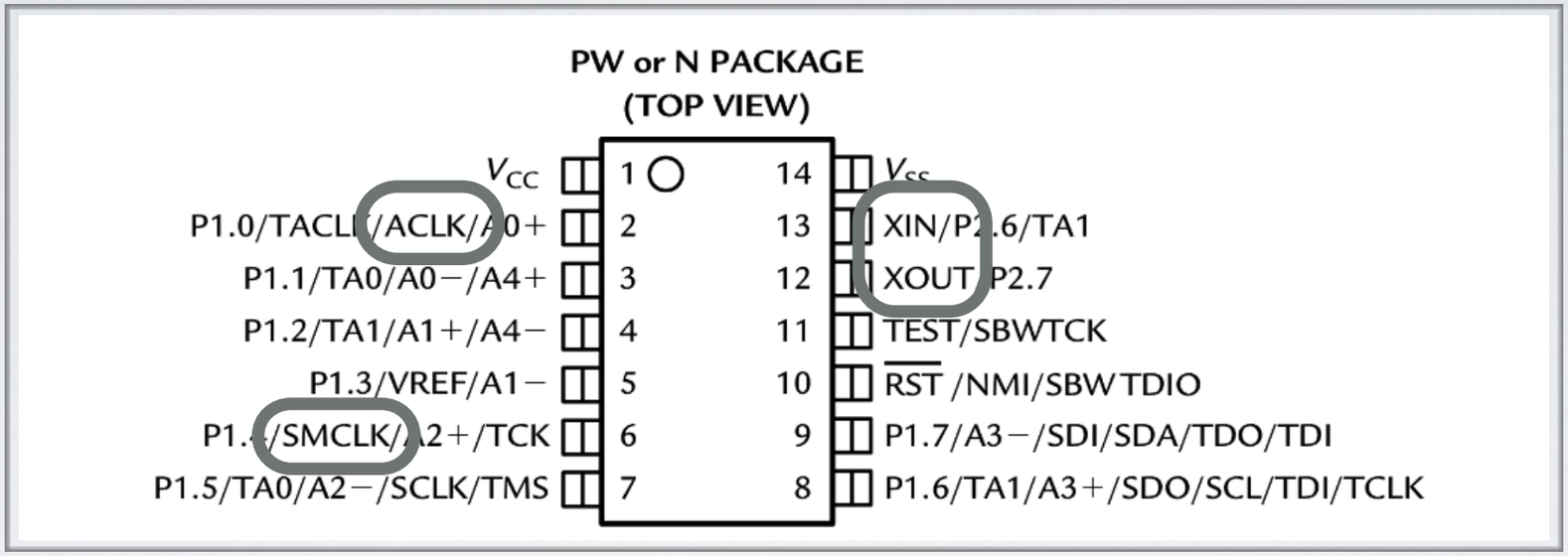
GERADOR DE CLOCK



Opção 1: cristal

Mais preciso e estável. Alguns MHz para o barramento principal, ou de 32768 Hz para tempo real.

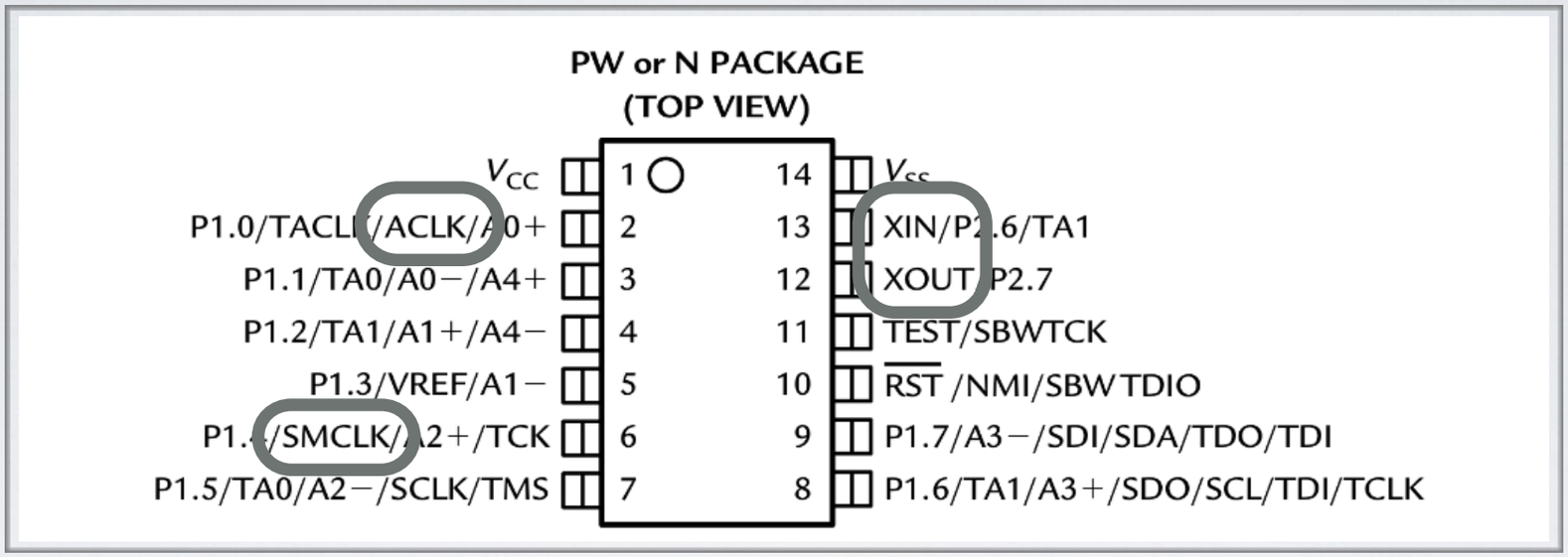
GERADOR DE CLOCK



Opção 1: cristal

Caros, delicados, ocupam mais espaço (podem necessitar de capacitores extra), consomem mais energia, e demoram para iniciar e estabilizar

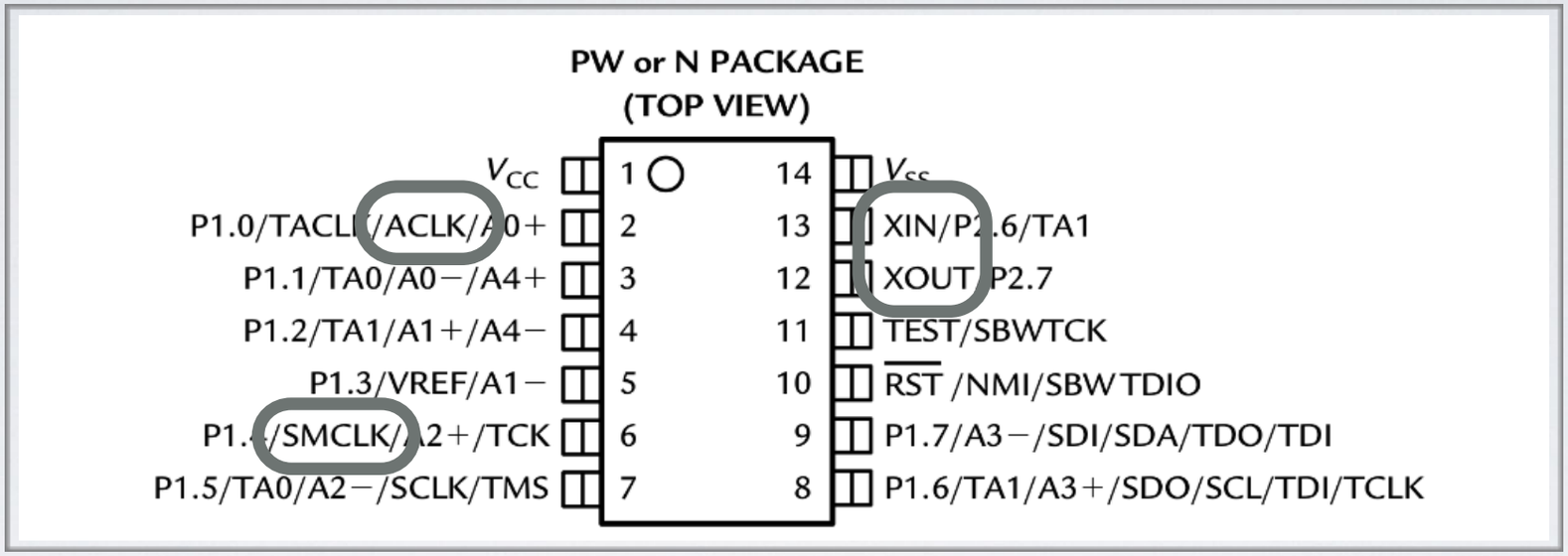
GERADOR DE CLOCK



Opção 2: circuito RC

Mais baratos e rápidos de usar. Dependendo dos componentes, podem ser mais precisos e estáveis

GERADOR DE CLOCK

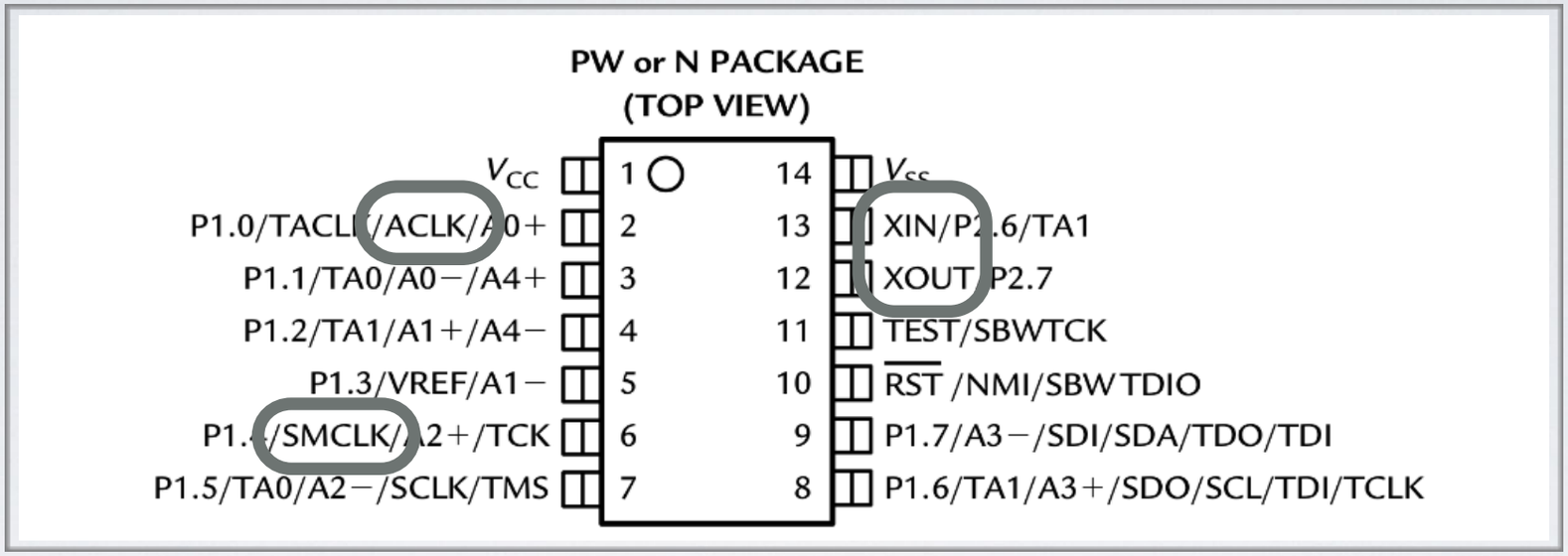


Sinais de clock no MSP430

Master clock (MCLK): CPU e alguns periféricos

Subsystem master clock (SMCLK) e
Auxiliary clock (ACLK): periféricos

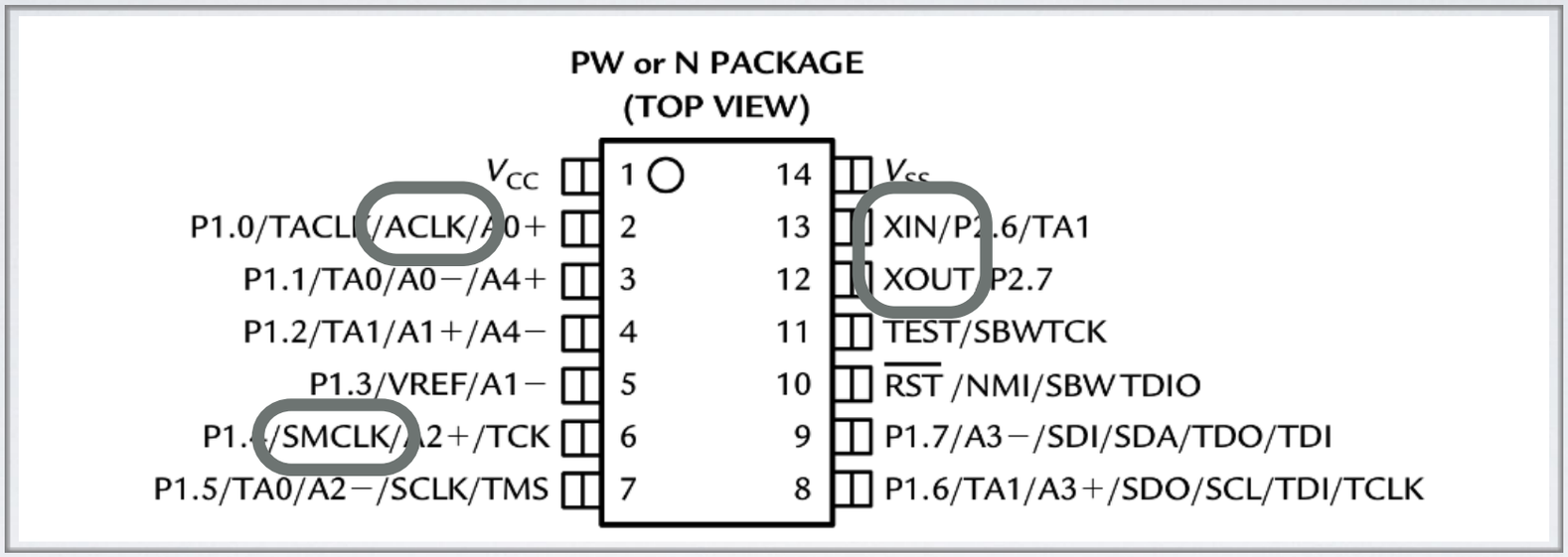
GERADOR DE CLOCK



ACLK é geralmente obtido de um cristal de 32768 Hz

MCLK e SMCLK são obtidos de um DCO (oscilador controlado digitalmente)

GERADOR DE CLOCK



O DCO pode rodar sozinho, em 0,8 ou 1,1 MHz, ou ser controlado por um FLL (frequency-locked loop) de 32 vezes o ACLK, em 1.048.576 Hz

EXCEÇÕES

Table 5. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
Timer1_A3	TA1CCR0 CCIFG(4)	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG(2)(4)	maskable	0FFF8h	28
Comparator_A+	CAIFG(4)	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG(4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5)(4)	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG(4)	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7(2)(4)	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See (7)			0FFDEh	15
See (8)			0FFDEh to 0FFC0h	14 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
(6) In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.
(7) This location is used as bootstrap loader security key (BSLSKEY). A 0xAA55 at this location disables the BSL completely. A zero (0h) disables the erasure of the flash if an invalid password is supplied.
(8) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

A execução de um programa segue normalmente, exceto quando ocorrem interrupções ou resets

EXCEÇÕES

Table 5. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
Timer1_A3	TA1CCR0 CCIFG(4)	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG(2)(4)	maskable	0FFF8h	28
Comparator_A+	CAIFG(4)	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG(4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5)(4)	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG(4)	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7(2)(4)	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See (7)			0FFDEh	15
See (8)			0FFDEh to 0FFC0h	14 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
(6) In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.
(7) This location is used as bootstrap loader security key (BSLSKEY). A 0xAA55 at this location disables the BSL completely. A zero (0h) disables the erasure of the flash if an invalid password is supplied.
(8) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

Interrupções:

Causadas por hardware, indicam eventos que devem ser tratados

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Table 5. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
Timer1_A3	TA1CCR0 CCIFG(4)	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG(2)(4)	maskable	0FFF8h	28
Comparator_A+	CAIFG(4)	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG(4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5)(4)	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG(4)	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7(2)(4)	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See (7)			0FFDEh	15
See (8)			0FFDEh to 0FFC0h	14 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
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(8) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

Interrupções:

O processador pára o que está fazendo, guarda o conteúdo do Program Counter e do Status Register, e executa a ISR correspondente

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Table 5. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
Timer1_A3	TA1CCR0 CCIFG(4)	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG(2)(4)	maskable	0FFF8h	28
Comparator_A+	CAIFG(4)	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG(4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5)(4)	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG(4)	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7(2)(4)	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See (7)			0FFDEh	15
See (8)			0FFDEh to 0FFC0h	14 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
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(8) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

Interrupções:

ISR é uma *interrupt service routine*, uma função ou subrotina chamada por hardware

EXCEÇÕES

Table 5. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
Timer1_A3	TA1CCR0 CCIFG(4)	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG(2)(4)	maskable	0FFF8h	28
Comparator_A+	CAIFG(4)	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG(4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5)(4)	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG(4)	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7(2)(4)	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See (7)			0FFDEh	15
See (8)			0FFDEh to 0FFC0h	14 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
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(8) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

Interrupções também podem "acordar" o processador de um estado de baixo consumo

EXCEÇÕES

Table 5. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
Timer1_A3	TA1CCR0 CCIFG(4)	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG(2)(4)	maskable	0FFF8h	28
Comparator_A+	CAIFG(4)	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG(4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5)(4)	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG(4)	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7(2)(4)	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0FFE4h	18
			0FFE2h	17
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See (7)			0FFDEh	15
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Resets:

Gerados por hardware ou pelo Watchdog Timer, reiniciam todo o sistema

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Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
Timer1_A3	TA1CCR0 CCIFG(4)	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG(2)(4)	maskable	0FFF8h	28
Comparator_A+	CAIFG(4)	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG(4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5)(4)	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG(4)	maskable	0FFEAh	21
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I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0FFE4h	18
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(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
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Endereços das ISRs (incluindo a de Reset) são guardados em uma vector table, ao final da memória de programa (0xFFC0-0xFFFF)

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Table 5. Interrupt Sources, Flags, and Vectors

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Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG(4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5)(4)	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG(4)	maskable	0FFEAh	21
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Se duas ou mais ISRs são chamadas, a ordem de execução é definida pela vector table, a partir do endereço mais alto