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Electronic setup for time-of-flight cross section measurements at GELINA

Brief description of the electronics used for time-of-flight experiments at GELINA

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Contents

1 Abstract

The GELINA facility is designed for high resolution neutron induced total and reaction cross section measurements using the time-of-flight (TOF) technique. This report describes the pulse processing electronics used at GELINA to treat the time and amplitude signals produced by the neutron detectors in transmission experiments and by the reaction product detectors in capture, fission or charged particle reaction measurements. The electronic modules and data acquisition hardware are described.

2 Introduction

The GELINA facility at the EC JRC-Geel is dedicated to accurate neutron cross section measurements using the time-of-flight (TOF) technique. A detailed description of the facility can be found in ref. [1]. It is a multi-user TOF facility, providing a white neutron source with a neutron energy range from 10 meV to 20 MeV. Up to 10 experiments can be performed simultaneously at measurement stations located between 10 m to 400 m from the neutron production target. The electron linear accelerator provides a pulsed electron beam with a maximum energy of 150 MeV and a repetition rate ranging from 50 Hz to 800 Hz. A compression magnet reduces the width of the electron pulses to less than 1 ns [2]. The electron beam hits a mercury-cooled uranium target producing Bremsstrahlung and subsequently neutrons via photonuclear reactions [3]. The total neutron intensity at the target is about 3.4×10^{13} s^{-1}. Two water-filled beryllium containers mounted above and below the neutron production target are used to moderate the neutrons and to produce a neutron spectrum ranging from 10 meV to 20 MeV. By applying different neutron beam collimation conditions, experiments can use either a fast or a thermalized neutron spectrum. The neutron production rate is constantly monitored by BF_3 proportional counters which are mounted in the ceiling of the target hall. The output of the monitors is used to normalize the time-of-flight spectra to the same neutron intensity. The measurement stations are equipped with air conditioning to reduce electronic drifts in the detection chains due to temperature changes and to keep the sample at a constant temperature. This report describes the electronics used for time-of-flight capture and transmission measurements at GELINA.

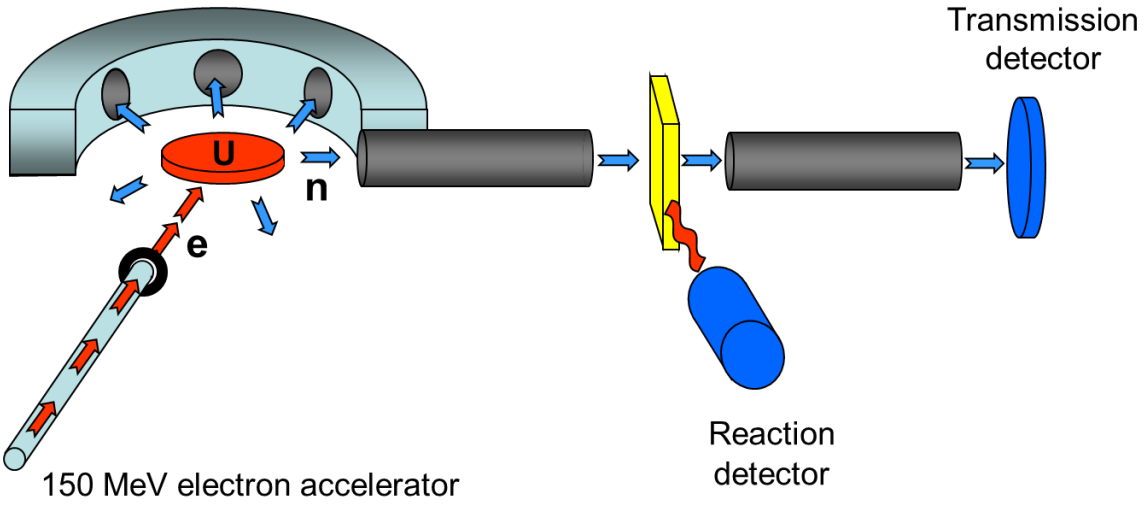
3 Time-of-flight technique

GELINA is optimised for cross section measurements (total, capture, fission, inelastic scattering and charged-particle production cross sections) in the resonance region with high energy resolution [4]. The time-of-flight technique is used to determine the velocity and the energy of a neutron from the time it needs to travel a given distance. The basic principle is illustrated in **Figure 1** and **Figure 2**. Experimentally this time is derived from the difference between a stop and a start signal, represented by T_S and T_0, respectively. At the GELINA facility the start signal is produced when the pulsed electron beam passes through a coil just before the beam enters the uranium target. This signal represents the time the neutron is produced. The stop signal in a transmission experiment is provided by the neutron detector. In a reaction cross section experiment the arrival time is obtained from the detection of the reaction products which are emitted in the neutron induced reaction. The observed TOF, t_m, becomes

$$t_m = (T_S - T_0) + t_0$$

where t_0 is a time offset. This time offset is mostly due to a difference in cable lengths.

Figure 1. Schematic representation of a time-of-flight facility.



The TOF t_m can be related to the velocity v of the neutron at the moment it leaves the target-moderator assembly and enters the detector or sample by [4]

$$v = \frac{L}{t} = \frac{L}{t_m - (t_t + t_d)},$$

where L is the distance between the outer surface of the neutron-producing target and the front face of the detector or sample, t_t is the time difference between the moment of neutron creation and the moment the neutron leaves the target and t_d is the difference between the moment the neutron enters the detector or sample and the time of detection. The kinetic energy of the neutron is given by

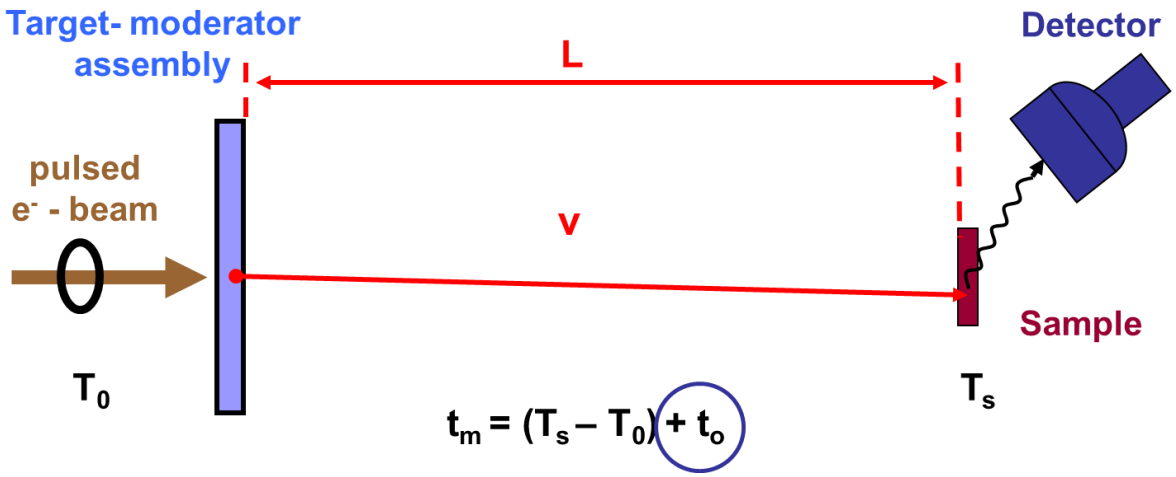
$$E = m_n c^2(\gamma - 1),$$

where m_n is the rest mass of the neutron and represents the Lorentz factor

$$\gamma = \frac{1}{\sqrt{1 - \left(\frac{v}{c}\right)^2}},$$

with c the speed of light.

Figure 2. Schematic representation of a time-of-flight technique.



4 Pulse processing electronics

Depending on the reaction to be investigated, different detector types are used to detect the reaction product resulting from the interaction of a neutron with the sample or, in the case of a total cross section measurement, to detect the neutrons passing through the sample. Mostly two signals, i.e. a time and an amplitude signal, are derived for each event that is detected. The time signal is used to determine the TOF of the neutron that was detected or that induced the reaction in the sample. The amplitude signal, providing information about the energy that is deposited in the detector, can be used to monitor the detector stability, to identify a specific reaction, to produce energy differential cross section data or to determine the detection efficiency e.g. by applying the pulse height weighting technique [5].

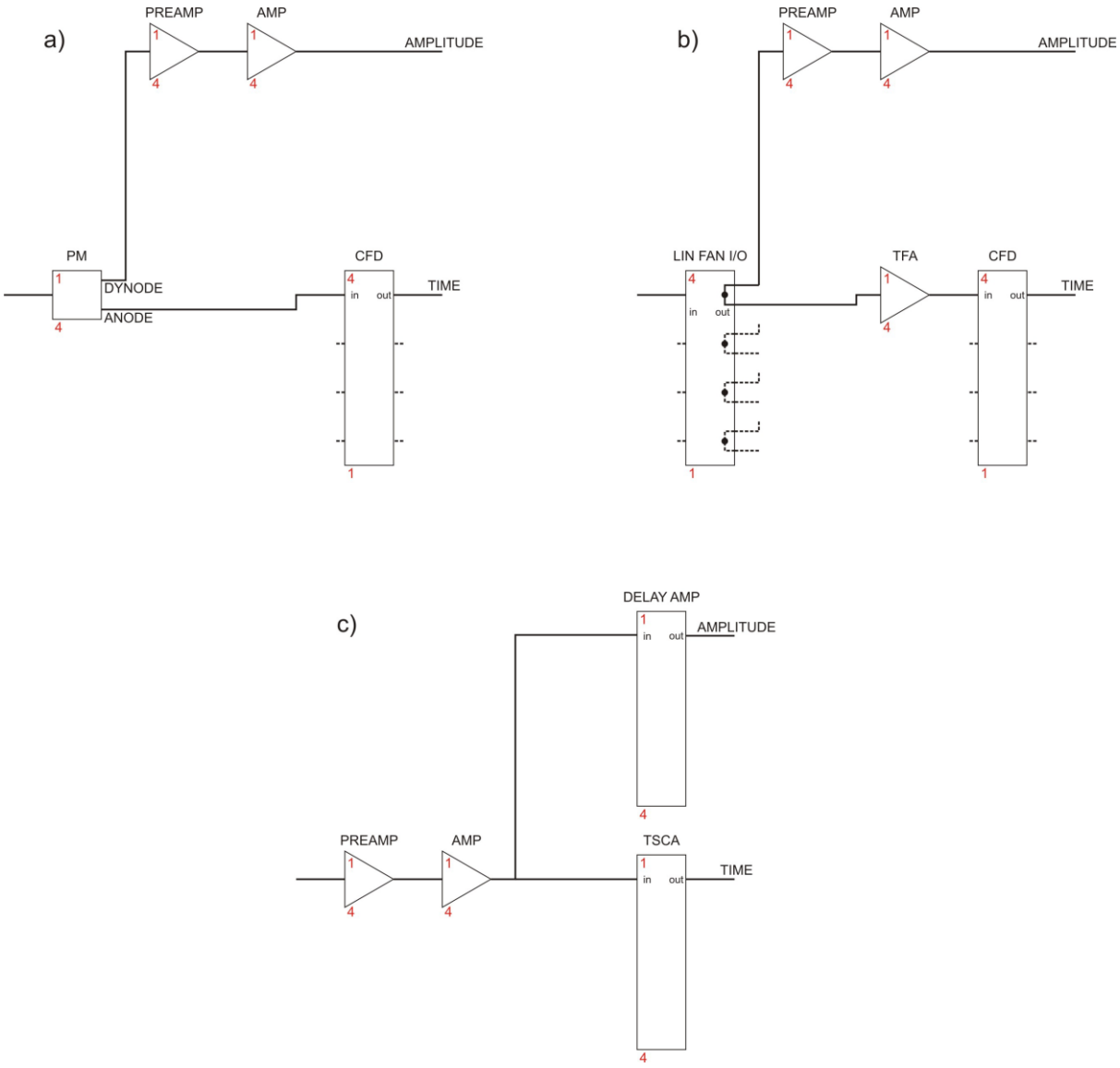
Both the time and amplitude signal can be determined by directly digitizing the signal that is produced in the detector [6][7] or by using more conventional methods based on analogue and logic NIM modules. Most of the transmission [8][9][10], capture [8][10][11] and fission cross section measurement [12][13] setups at GELINA are based on the use of NIM modules. The setups are very similar and the principles of the signal processing are discussed in this report. The full treatment of the signals is described in **Figure 3** and **Figure 4**. Most of the modules are used to create an acquisition system with a fixed dead time and to avoid large dead time corrections due to the γ-ray flash, which is characteristic of the GELINA facility. For a fixed dead time system, Moore's formula [14], which accounts for possible variations in the beam intensity, can be applied.

Figure 3a illustrates the production of the time and amplitude signal for a scintillator detector connected to a photomultiplier (PMT). The latter converts the extremely weak light output of a scintillation pulse into a corresponding electrical signal that is further processed by electronic modules. The fast anode signal of the PMT is directly transmitted to a constant fraction discriminator (CFD) which produces a logic signal at the time the leading edge of the pulse reaches a given fraction of its peak amplitude. For pulses with the same shape this time signal is independent of the amplitude. This technique eliminates or minimizes the time jitter, which affects the time resolution. The time signal is sent to the time-to-digital converter (TDC) to determine the time-of-flight of the detected event. If the anode signal is not strong enough it can be amplified by a timing-filter amplifier before it is processed by the CFD as shown in **Figure 3b**. The signal of a dynode (e.g. the 9th dynode for a 14 stage PMT) is proportional to the amount of light produced in the scintillator. After a first shaping by a pre-amplifier (PA), the signal is shaped and amplified by a spectroscopic amplifier (SA) to produce a signal that provides information about the energy deposited in the detector. The output of the amplifier is first sent to a linear gate which only transmits a signal when a valid time-of-flight signal produced by the corresponding detector is present. The analogue signal is then digitized in an analogue to digital converter (ADC) before it is sent to the data acquisition system. Hence, the ADC's do not process any event for which no valid time-of-flight output is produced by the same detector. For some applications, e.g. in the case of a Frisch-gridded ionization chamber [10]**Error! Reference source not found.**, the time signal (T_S) is produced by a timing single channel analyser (TSCA) at the moment the bipolar pulse of the SA crosses the zero level. To align the amplitude pulse in time with the timing signal, the bipolar pulse is delayed before it is sent to the ADC, as illustrated in **Figure 3c**.

The time-of-flight and amplitude signals of a detected event are recorded in list mode using a multi-parameter data acquisition system (DAQ) that has been developed at JRC-Geel. The system consists of a number of logic modules to handle the timing signal, dead time and coincidences, a TDC, an ADC for each detector, a scaler module, a modular multiparameter multiplexer (MMPM) and an I/O transmitter module (also referred to as transceiver), as shown in **Figure 4**. The TDC is a multi-hit time coder that has been developed at the EC-JRC-Geel [15]. The output of the TDC and each ADC are fed to the MMPM which is connected to the transceiver. The latter provides the communication with the DAQ PC through a PCI(e) card. The scaler module provides additional information from the linac and the neutron monitors via a second PCI(e) card in the PC. The DAQ software, which is based on Labview, is used for data acquisition, for data storage and for on-line monitoring of the data.

The main dead time in the whole pulse processing chain is due to the conversion of the analogue signal into a digital number by the ADC and the subsequent processing by the MMPM. It depends on the shaping time of the signal and the type of ADC. It is about 2.5 µs for a FAST ADC Model 7072 processing a signal with a 0.25 µs shaping time. For a signal from a Ge-detector processed with a high resolution Silena ADC the dead time reaches 10 µs.

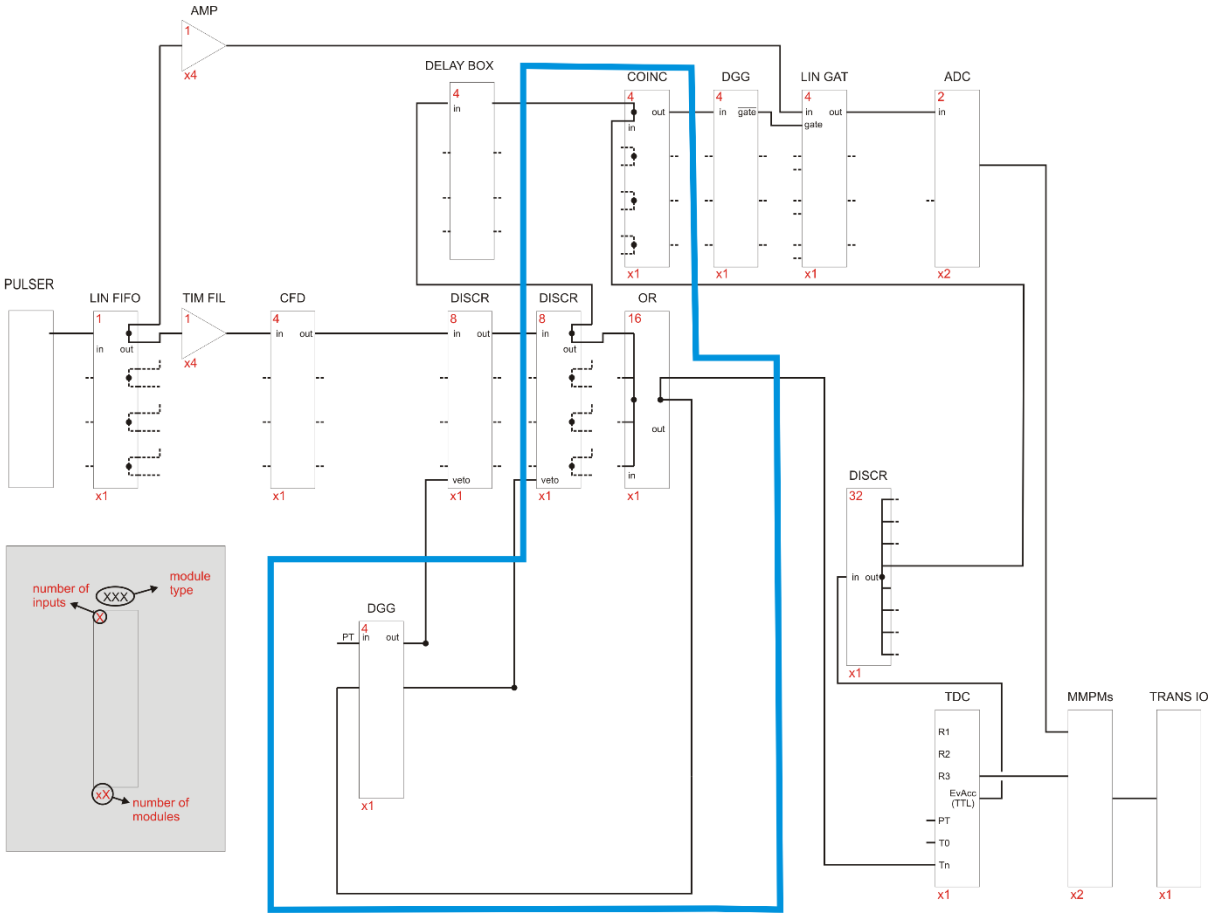
Figure 3. a) Detection set-up for cross section measurements based on the use of a scintillation detector with the time signal derived with a CFD. b) Detection set-up for cross section measurements based on the use of a timing-filter amplifier to amplify the fast time signal before it is processed by the CFD. c) Detection set-up for cross section measurements based on the use of an ionization chamber with the time signal derived from the zero crossing of the bipolar output of a spectroscopic amplifier.



The electronics to process the amplitude and time pulses from the detectors are shown in **Figure 4**. The setup is optimised to avoid the treatment of signals resulting from the detection of the γ-ray flash, to process signals with a fixed dead time and to produce a gate signal for the processing of the amplitude pulse. Two different systems can be used. One system is based on the use of separated standard logic NIM modules. The other relies on a FPGA programmable module developed by Wiener, a so-called NIMBox. The functionalities programmed in this module are shown in **Figure 6** and replace these of the NIM modules inside the blue line in **Figure 4**. Both schemes are intended for the use with up to 4 detectors.

When the detection system consists of different detectors, it is important to transfer the signals between modules using cables with the same lenght. Time differences between the fast time signals of the different detectors can be compensated by adjusting the length of the cables transmitting the signals from the CFD to the first discriminator. In case the NIM-box is used, time differences of a few ns have been observed between different output channels. These differences can also be compensated by adjusting the length of the cables at the entrance of the NIM-Box.

Figure 4. Electronic set-up used to process the time and amplitude signals. Most of the modules are used to avoid the processing of events resulting from the γ-flash, to produce a fixed dead time and to produce a gate signal for the amplitude signal. The blue line indicates the functions programmed in the NIM-box, as shown in Figure 6.



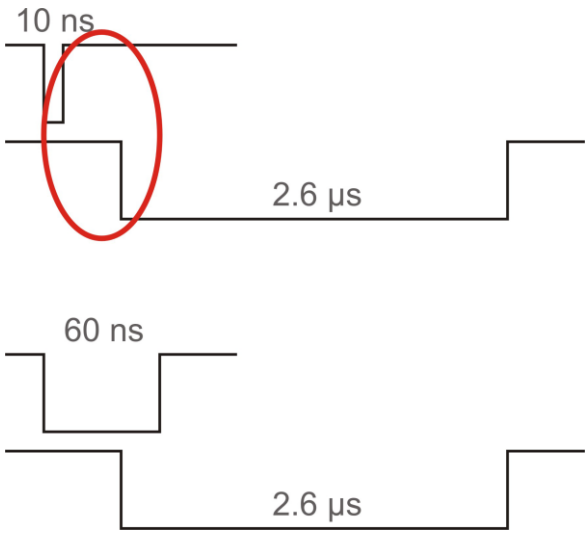
4.1 Standard logic NIM modules

The first leading edge discriminator avoids the processing of γ-ray flash events. Valid stop signals resulting from the CFD are not transmitted when a veto signal is present. The veto signal of the first leading edge discriminator is produced by a gate generator at the moment the pretrigger is produced. The length of the veto signal, in the order of 3 µs, is defined by the time difference between the time signal produced by the γ-ray flash and the pretrigger signal T_P, which is produced about 2.5 µs before the start of the pulsed electron beam. This discriminator also ensures that spurious signals due to electronic noise are not processed.

The second discriminator introduces the fixed dead time. Its veto signal prevents that any signal occurring within a fixed time after a previous signal is processed. The length of the veto signal is set to the longest dead time in the system. For each event that passes through the first discriminator this veto signal is produced by using the output of a logic OR-module (fan-in/fan-out). The width of the output signals of the first discriminator (about 60 ns) is adjusted to bridge the time-difference between the input signal and the leading edge of the veto signal as illustrated in **Figure 5**.

The second output of the OR-module is used by the time to digital converter (TDC) to determine the time-of-flight of the detected event. The start signal produced by the pulsed electron beam is the zero-point of the clock. The TDC is reset with the pretrigger signal of the next accelerator pulse. The TDC produces a logic pulse, so named as Event Accepted (EA), when a valid time-of-flight is produced.

Figure 5. Timing properties of the fast time pulse from the first discriminator and the veto signal for the second discriminator. The width of the output of the first discriminator is adjusted to overlap with the veto signal of the second discriminator. The width of the veto signal defines the fixed dead time.

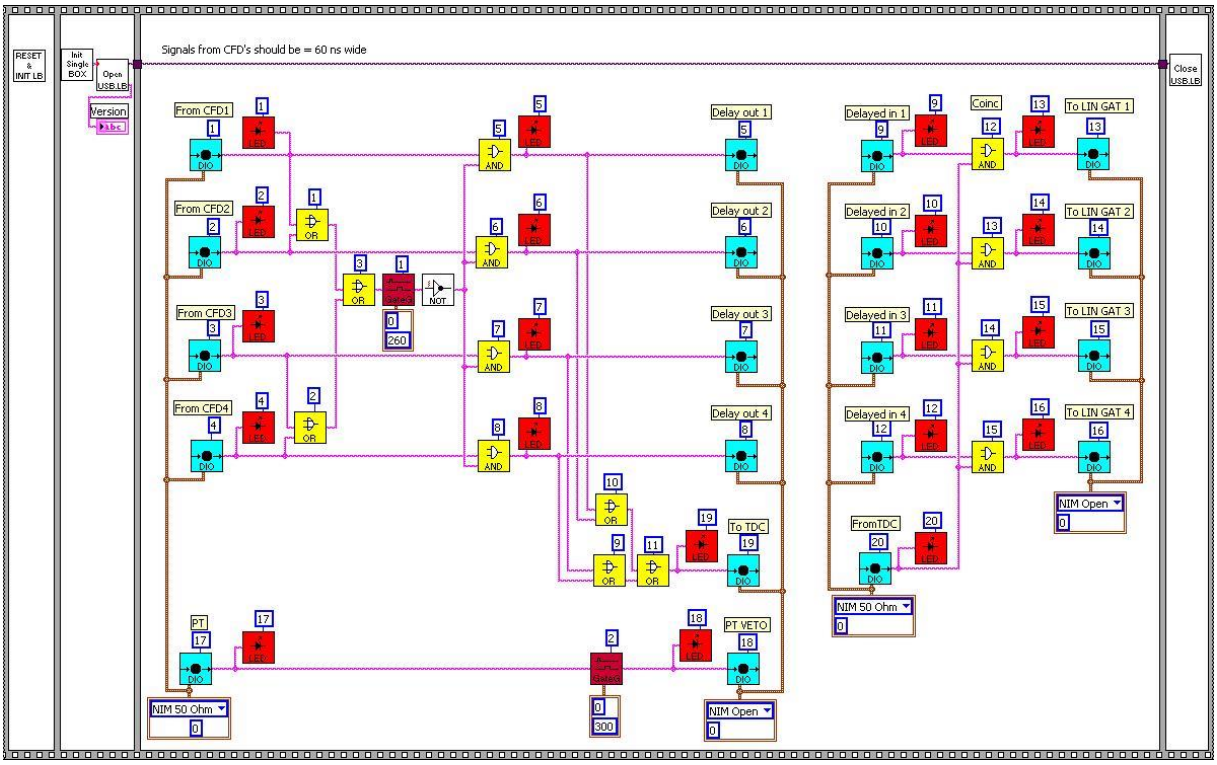


The EA signal produces a gate signal for the linear gate to allow the processing of the amplitude signal by the ADC. A coincidence unit ensures that the gate signal is only present when the EA originates from the time signal of the corresponding detector. The time difference between the output of the second discriminator and the EA is adjusted by a passive delay. Since the linear gate only accepts TTL signals as a gate input, the NIM signal from the coincidence unit is transformed into a TTL signal by a gate generator. At the same time the gate generator is used to adjust the time difference between the gate and amplitude signal.

4.2 FPGA programmable module (NIM-Box)

Most of the functionalities explained in the previous section can be performed by a Wiener FPGA programmable module, which is referred to as NIM-box. This module with a 1 NIM slot size replaces the modules within the blue line in **Figure 4**. The functions, which are programmed in Labview, are specified in **Figure 6**. The NIM-Box receives the pre-trigger signal (input #17, bottom part of the chart) to create a delayed gate of 3 µs (output #18) used as veto for the γ-ray flash signals. After being discriminated and vetoed by the TP gate, the detector signals are sent to the NIM-Box (inputs #1-#4) which creates a fixed internal gate to implement the fixed dead time. This is realized by means of the AND between each detector signal and the NOT of this gate. The resulting signals are sent to an external Delay Box (outputs #5-#8) while their OR produces the stop signal T_S (output #19) which is sent to the TDC. Moreover, the NIM-Box accepts the EA NIM output from the TDC, after passing through a discriminator (input #20) which is compared with every delayed detector signal (inputs #9-#12). It is worth mentioning that the NIM-Box introduces a 10 ns jitter on the width of the internally generated veto gates due to its 100 MHz internal clock. The stop signal T_S is not affected by this jitter.

Figure 6. Functionalities of the FPGA module (NIM-BOX).



5 Detailed description of the electronic modules

In this section the functionalities of the modules used in GELINA measurement systems are described in more detail. For most of them the data sheets are added in the Appendix and for some of them the dead time and delay they introduce on the output signal are reported in **Table 1**.

Table 1. Delay and dead time of NIM modules used for the set-up of **Figure 4**.

Module	Delay/ns	Dead time/ns	Comments
CAEN N454 Logic FI/FO	6	≈0	Not produced anymore
Lecroy 429 A Logic FI/FO	6	≈0	
PS704 Quad Discriminator	8	4 + Pulse width	
PS710 Octal Discriminator	8	4 + Pulse width	
PS755 Quad Fourfold logic unit	9	4 + Pulse width	
PS794 Quad Fourfold logic unit	> 30	25 + Pulse width	
GG8020 Octal gate generator	> 80	Pulse width + extended	

5.1 Constant Fraction Discriminator (CFD)

The time signal for each detector is mostly produced by a CFD. One-channel and four-channel modules produced by CANBERRA and ORTEC are used. The performance of the different models is very similar. For a scintillator a time signal independent of the pulse amplitude is produced. The CFD threshold and delay length need to be set for each particular detector. The delay length is adjusted by an external cable. Typically the delay corresponds to the time needed by the input signal to rise from 20% to 100% of its peak height.

5.2 Discriminator (DISCR)

A discriminator (Octal Discriminator Model 710 from Philips Scientific or equivalent) with a veto input option is used to prevent signal processing of events corresponding to the γ-ray flash. A similar unit avoids the processing of signals produced by this first discriminator within a fixed time period (dead time) after the start of a previous event. This fixed dead time is defined by the width of the veto signal. In the case of the NIM-Box the fixed deadtime is created by the FPGA using an internally generated gate in combination with AND operations. Another discriminator is used for reduction of the length of the EA signal which is produced by the TDC when a valid TOF signal is processed, and its distribution for the treatment of the signal amplitude. For each detector the EA signal is needed as an input to the coincidence unit. The EA output of the TDC is reduced to a length of 10 ns to minimize the number of random coincidences. Finally, another octal discriminator distributes the signals from the accelerator (T_P, T_0) and the counts from the neutron monitors (CM1, CM3) into the scaler module.

The threshold of all the discriminators is set to -250 mV. The width of the output signals of the first discriminator is set at 60 ns as illustrated in **Figure 5**. This is done to have an overlap in time between the output of the first discriminator and the veto signal of the second. The width of the output signals produced by the other discriminators is set to 10 ns.

5.3 Logic fan-in/fan-out (LOG FIFO)

A logic fan-in/fan-out unit is used as a logic OR gate to produce a stop signal T_S for the TDC in case at least one of the detectors has produced a time signal. In case of the NIM-Box this functionality is taken over by OR operations in the FPGA program.

5.4 Delay and Gate Generator (DGG)

A quad delay and gate generator (Gate & Delay Generator Model 794 from Philips Scientific) creates the veto to avoid processing of events due to the γ-ray flash and the veto that imposes a fixed dead time. This unit is chosen because of its small internal delay and the short fixed dead time it introduces. In case of the NIM-Box this is done by gates generated internally in the FPGA program.

Another gate and delay generator (Octal Gate and Delay Generator Model GG8020 from ORTEC) produces the input for the linear gate selecting the valid pulse height signals. For each detector a TTL signal defines the start of the gate in the linear gate. The TTL signal is delayed such that its leading edge corresponds to the start of the analogue input signal.

5.5 Passive delay (DELAY)

A passive delay box (ORTEC model DB463) aligns the stop signal of each detector with the EA signal of the TDC. The delay time can differ for each channel. For the traditional setup it is about 25 ns. The delay introduced by the NIM-Box is about 30 ns.

5.6 Logic unit (COINC)

A logic unit (Logic Unit Model 752 from Philips Scientific) accepts NIM signals and checks the coincidence between the EA signal from the time coder and the delayed stop signal of each detector. The module produces an output for the period the input signals overlap in time. In case of the NIM-Box this functionality is taken over by AND operations in the FPGA program. The NIM output is transformed into a TTL signal by a logic gate and delay generator which serves as the gate input to a linear gate module and also adjusts the time difference between the gate and the amplitude signal.

5.7 Time to Digital Converter (TDC)

The time-of-flight of a neutron is derived from the difference in time between a start signal T_0, given at each electron burst, and a stop signal T_S produced by the detector. This time difference is measured with a multi-hit fast time to digital converter (TDC) developed at the EC-JRC-Geel. Two types of TDC are in use. The 8514 and IE301 models with a time resolution of 0.5 and 1 ns, respectively. The TDC has three inputs, i.e. the pretrigger (T_P), the start (T_0) and the stop signal (T_S). The pre-trigger signal T_P resets the TDC and the T_0 signal is the zero-point of the clock. When a valid time difference ($T_S - T_0$) is processed an EA signal is produced. The digitized time information is sent to the multiplexer module (MMPM).

For a set-up including more than one detector, since the stop signal T_S is produced after an OR gate the identification of the detector creating the stop signal is lost. This information can be recovered in case the amplitudes produced by the detected events are also recorded or by the use of routing bits in the form of a TTL signal. The routing bit and the stop signal have to coincide in time within less than 5 ns. Routing bits can also be used to identify coincident or anti-coincident events or to specify the status of a sample changer.

5.8 Linear gate (LIN GAT)

A linear gate (ORTEC Model 426) blocks an input signal which is not accompanied by an enable pulse. The start of the enable pulse is defined by a TTL input signal and its duration can be adjusted on the linear gate module itself.

5.9 Analogue to digital converter (ADC)

An analogue to digital converter (ADC) transforms the amplitude signal into a digital number. For energy spectroscopic measurements Silena ADC's are preferred. Unfortunately they introduce a long dead time. When the dead time has to be kept as low as possible and no extreme amplitude resolutions are required, the dual 500 ns ADC Model 7072 from FAST is mostly used.

The Silena Model 7423/UHS is an ultra high speed, highly reliable analog to digital converter with excellent differential linearity. It has 8k ADC channels and 3 µs conversion time. There is the possibility to use a Silena ADC 7423 directly with DAQ2000 software (1ADC program) without using a TDC or a MMPM but this requires an internal hardware modification of the ADC. In this case a permanent +5V must be applied to the DataRequest line.

The ADC Model 7072 is used in Pulse Height Analysis (PHA) mode, converting the amplitude of the analogue signal to a numeric value. It accepts analogue signals between 0.025 and 10 V and processes only signals with an amplitude between the lower (LLD) and the upper-level discriminator (ULD). The ADC threshold is settable in the range of -781 mV and 1 V. This threshold is used to prevent triggering from noise and to adjust for small input offset voltages. In our case it has been set to about 30 mV, while the ULD is set to the maximum value and the LLD slightly above the ADC threshold. The ADC gate is not used in the setup, as its function is taken by the linear gate. The digitized pulse height information is sent to the MMPM.

5.10 Inhibitor (INH)

The MMPM has the possibility to stop taking data when it receives an inhibit signal. This signal can be produced by an inhibitor module developed at the EC-JRC-Geel. The inhibit signal is created when certain conditions are not fulfilled, e.g. when one of the crate power supplies is failing or when the accelerator frequency, the event rate or the rate measured by the neutron monitors drops below a given threshold.

5.11 Modular multiparameter multiplexer (MMPM) and tranceiver (TRANS IO)

The modular multiparameter multiplexer (MMPM) developed at the EC-JRC-Geel [16] is attached to the digital outputs of the TDC and ADC's through multiwire flatcables. The output of the TDC and/or ADC's is multiplexed to a single stream of data words and transmitted to the DAQ PC via the I/O module (transceiver). The data taking can be stopped by presenting a NIM signal at the inhibit input. The MMPM has been designed to accommodate data produced by most of the commercial ADC's (Canberra, Silena, FAST) and the TDC's developed at the EC-JRC-Geel. For each ADC one flatcable is required while the input of the TDC is provided by two flatcables. The TDC and most of the ADC's have a different protocol to transfer the data. With a set of internal dip switches the type of module transmitting the data to the MMPM can be specified (see MMPM manual [16]). Up to six MMPM modules can be daisychained via 25-pin D-type connectors on the front side on the module. The module having the female (left) front side chain connector free acts as the master and takes control of the synchronization bus. The MMPM can be operated in free mode or in coincidence mode. The mode can be changed with a jumper on the module's PCB.

For the set-up discussed in this report the MMPM operates in coincidence mode. In coincidence mode three time windows control the information produced by the same event: a coincidence window (ΔT_{CO}), a time out window (ΔT_{TO}) and a window to reset the MMPM (ΔT_{CL}). The length of these windows can be defined by a set of internal dip switches. The coincidence window is opened when one of the modules connected to the MMPM presents a signal. All other modules that start the conversion of a signal within a time frame ΔT_{CO} will add digital data to the same event. The conversion process has to be finished within the time $\Delta T_{CO} + \Delta T_{TO}$. At the end of the conversion the MMPM has to reset all the modules within a time ΔT_{CL}.

The total dead time introduced by the MMPM depends on the length of the coincidence window ΔT_{CO} and the reset window ΔT_{CL}. The MMPM dead time $\theta_{D,MMPM}$ for different settings of ΔT_{CL} and ΔT_{CO} can be approximated by

$\theta_{D,MMPM} = 650$ ns + ΔT_{CL}+ ΔT_{CO}

for ΔT_{CL} = 100 ns and

$\theta_{D,MMPM} = 600$ ns + ΔT_{CL}+ ΔT_{CO}

for $\Delta T_{CL} \geq 200$ ns.

The electronics scheme in **Figure 4** is designed such that for each event the information provided by the TDC arrives first. Therefore the TDC can be considered as a master and will always start the coincidence window and consequently also the windows ΔT_{CL} and ΔT_{TO}. Hence, when the length of the veto of the second discriminator is larger than the total dead time to treat the analogue signal, a fixed dead time is created. Special attention is required when using the ADC Model 7072 from Fast. This module produces no start signal but only a stop signal at the end of the conversion process. Therefore, the ADC has to finish the conversion within the time ΔT_{CO} after the TDC started its conversion. Under these conditions the window ΔT_{TO} is not relevant and can be put to a minimum. The length of the ΔT_{CL} window depends on the module type.

The MMPM produces several outputs to control the conversion processes, e.g. it produces a NIM signal for each processed event and when a module started a conversion within ΔT_{CO} but did not finish the conversion within the time ΔT_{CO}+ ΔT_{TO}. The MMPM also offers output signals to control the settings of the ΔT_{CO} and ΔT_{TO} windows.

5.12 Scaler

A scaler module developed at the EC-JRC-Geel registers the number of accelerator pulses (T_P and T_0), the number of events detected by the neutron beam monitors and logic signals to monitor the functioning of the data acquisition system, e.g. the number of valid events processed by the TDC and the number of events for which the processing was started but not completed. The total number of T_0 signals and monitor counts are required for the data reduction procedures. A gate signal delivered by the MMPM synchronizes the scaler with the data acquisition. Up to 8 different logic signals can be connected to the scaler module.

5.13 T_P, T_0 and T_S simulator

A pulse generator has been configured at the EC-JRC-Geel to test the DAQ system when the electron accelerator is not in operation. The module is also very convenient to determine the dead time of the system. It simulates T_P, T_0 and T_S signals. The T_p and T_0 signals, which are separated in time, can be produced at different frequencies. The stop signal can be random or at a fixed frequency.

6 Data acquisition and analysis software

6.1 DAQ2000

A Labview based application (DAQ2000) controls the data acquisition and stores the digital TOF and pulse height data of each ADC together with the information registered by the scaler module. During data taking various TOF and ADC histograms can be produced on-line to check correct operation of the measurement set-up and data acquisition. A measurement run can be subdivided in different cycles. The length of a cycle can be defined by either the number of registered events per cycle or by the measurement time per cycle. For each cycle the data can be stored in list mode and/or in histograms. The total number of cycles can be predefined or can increase indefinitely until the acquisition is stopped manually.

For each measurement run a report file is produced. This file specifies the type of TDC that was used and contains information about the measurement configuration and the data related to each measurement cycle. For each cycle the starting time, the measurement time, the number of events and the information recorded by the hardware scalers are reported. Additional information, such as the number of counts processed by the TDC and each ADC, are produced by the software. These data are referred to as software scalers. For each measurement cycle the histograms produced on-line can be stored together with a list mode data file. The list mode data file records for each event the values from the TDC and ADC's that are connected to the MMPM. The measured TOF can be stored in list-mode with or without predefined accordeon (i.e. the description of a number of zones in the TOF spectrum with a different time compression factor). It is recommended to store the data with the time resolution of the TDC without any additional time broadening due to an accordeon setting. The report and list mode data files are processed to produce TOF histograms which are used to derive the experimental observables (transmission or reaction yields).

Recent DAQ2000 versions include an option to control the slide sample changer used for transmission experiments or for the selection of black resonance and overlap filters. When used, the status of the slide sample changer is provided in the report file for each cycle.

6.2 Data sorting and analysis

To verify the stability of the detection systems and the accelerator operating conditions (i.e. frequency, current and neutron output) two Labview based applications have been developed. In case of transmission measurements, the Data Sorter code [18] selects the cycles for which the ratio between the total counts in the transmission detector and the neutron monitors deviates from the average of this ratio for the previous and next cycles by less than a predefined value (typically 1%). For reaction cross section measurements only cycles with a predefined operating frequency and for which the total neutron intensity and response of the detection systems are within a user defined range around a predefined value, are selected using the RoRF code [19].

The AGL software package [20] produces TOF spectra from the list mode data together with all necessary additional information to derive the experimental observables from the spectra. To derive these observables the AGS package developed at the EC-JRC-Geel is used and recommended [21]. The AGS code includes all arithmetic operations of spectra. In addition, more advanced operations as dead time correction, least squares background fitting, reading of data files in ENDF format, projection of spectra on different time axes and bin averaging can be executed. The code is based on a compact formalism to propagate all uncertainties starting from uncorrelated uncertainties due to counting statistics. It stores the full covariance information after each operation in a concise, vectorised way and ensures the resulting covariance matrix is always positive definite. The AGS formalism results in a substantial reduction of data storage volume and provides a convenient structure to verify the various sources of uncertainties through each step of the reduction process. The concept applied in AGS has been recommended by the Nuclear Data Section of the IAEA to store time-of-flight cross section data in the EXFOR data base [22].

7 Determination of the time offset and system dead time

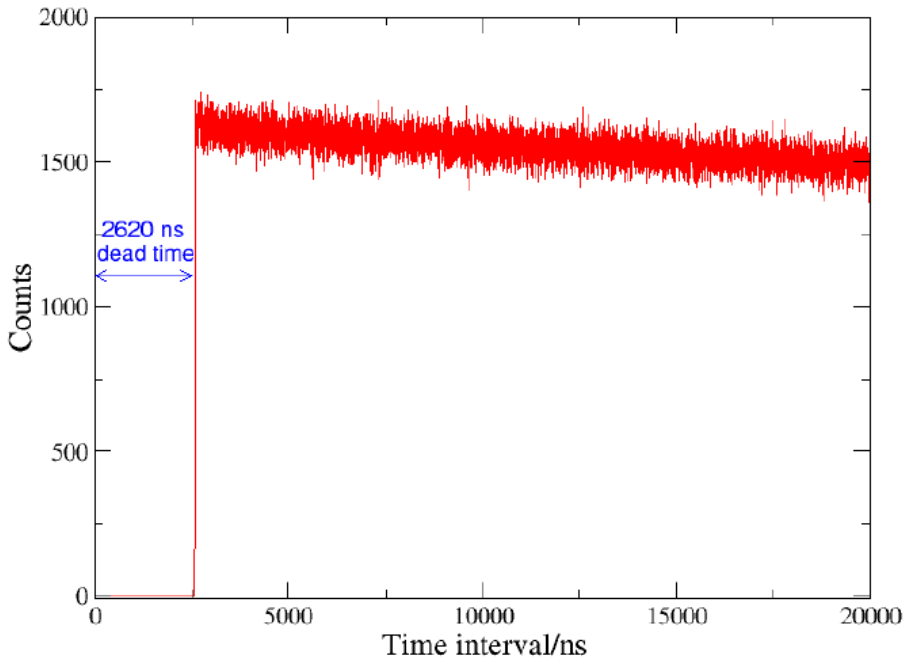
7.1 Time offset t_0

The time offset t_0 for a detection system consisting of scintillators detectors can be derived from the position of the γ-ray flash with an accuracy better than 1 ns. For other detectors, e.g. solid state or gaseous neutron or charged particle detectors, the time-offset derived from the γ-ray flash might be biased due to the difference between the energy loss process of a γ-ray and a charged particle. For neutron flux measurements with a ^{10}B loaded Frish-gridded ionization chamber and the T_S signal derived from the zero crossing of the bipolar output of a spectroscopic amplifier, the bias is in the order of 200 ns. The time resolution of such a system is around 40 ns and the time offset t_0 is best derived from transmission dips (e. g. 33 keV resonance due to a S filter) or resonance peaks of high energy resonances.

7.2 System dead time

The dead time of a detection set-up can be determined experimentally by a measurement of a time interval spectrum. That is, from the spectrum of the difference in arrival time of successive events originating from the emission of particles or γ-rays randomly distributed in time. The intensity of the source should be sufficiently high to guarantee that a significant amount of successive events occur within the dead time of the system. The two most convenient ways to determine the system dead time are to measure the time interval spectrum of events produced by the neutron beam during the accelerator operation or a pulse generator (simulator) or a strong calibration source while the accelerator is off. An example of such a time interval spectrum taken with a C_6D_6 liquid scintillator and a ^{137}Cs radionuclide source is shown in **Figure 7**. Within a time period corresponding to the dead time of the detection system no counts are observed.

Figure 7. Time-interval distribution resulting from measurements with a ^{137}Cs source and a detection system consisting of C_6D_6 detectors



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List of abbreviations and definitions

ADC	Analogue to Digital Converter
AGL	Analysis of Geel List mode
AGS	Analysis of Geel Spectra
C_6D_6	Deuterated benzene
CFD	Constant Fraction Discriminator
^{137}CS	Caesium-137
DAQ	Data Acquisition System
DGG	Delay and Gate Generator
DISCR	Discriminator
EA	Event Accepted
ENDF	Evaluated Nuclear Reaction Data File Format
EXFOR	Experimental Nuclear Reaction Database
FPGA	Field Programmable Gate Array
GELINA	Geel Linear Accelerator
IAEA	International Atomic Energy Agency
INH	Inhibitor
LIN GAT	Linear gate
LLD	Lower Level Discriminator
LOG FIFO	Logic fan-in/fan-out
MMPM	Modular Multi-Parameter Multiplexer
NIM	Nuclear Instrumentation Module
PA	Pre-Amplifier
PCI(e)	Peripheral Component Interface (Express)
PHA	Pulse Height Analysis
PMT	Photomultiplier Tube
RORF	Rejection of Report File
TDC	Time to digital Converter
TOF	Time-of-flight
TSCA	Timing Single Channel Analyser
TTL	Transistor-Transistor Logic
ULD	Upper Level Discriminator

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Annex

1. Phillips Scientific Octal Discriminator Model 710 Data Sheet Cover

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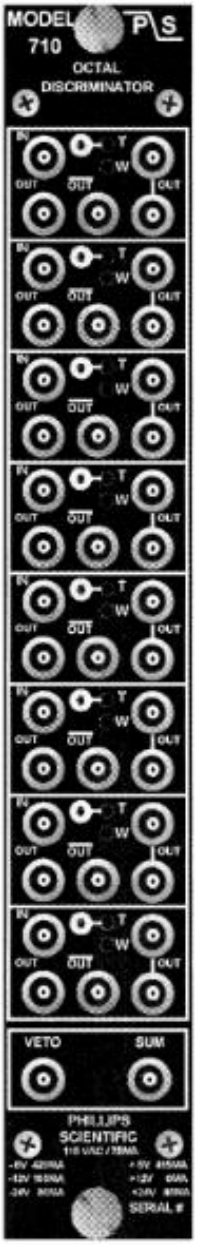
Phillips Scientific | Octal Discriminator | NIM MODEL 710

FEATURES

* 150 MHz Rate Capability
* Deadtimeless Updating Outputs
* Four Outputs Per Channel
* Fast Veto and Bin Gate Inhibiting
* Linear Summed Output



DESCRIPTION

The model 710 is a high-performance, eight channel, leading edge discriminator packaged in a single-width NIM module. It features independent threshold and width controls, a fast veto for inhibiting, a prompt linear summed output, and a versatile output configuration with four updating outputs per channel.

The 710 has high input sensitivity of -10mV variable to -1volt via a 15-turn front panel control. A front panel test point on each channel provides a DC voltage equal to ten times the actual threshold to insure accurate settings.

A unique summed output, common to all eight channels, delivers -1mA of current for each activated channel, thus allowing a fast decision to be made on the number of channels simultaneously hit. Up to 16 channels can be "OR'D" directly by cable to other summed outputs providing a versatile scheme to form a trigger.

Inhibiting of the discriminator can be accomplished in two ways. A front panel LEMO input accepts a NIM level pulse for fast simultaneous inhibiting of all eight channels. Secondly, a slow bin gate via the rear panel connector inhibits the module and is enabled or disabled from a rear panel slide switch.

Output durations are continuously variable via a front panel control over the range of 4nSec to 150nSec. The updating design permits deadtimeless operation which is desirable for fast coincidence applications at high rates. The 710 has four high-impedance current switching outputs per channel. They are configured as one pair of double amplitude bridged outputs, one normal NIM level and one complemented NIM level. When only one output from the bridged pair is used, a double amplitude NIM pulse (-32mA) is generated, useful for driving long cables with narrow pulses. Two normal NIM levels are produced when both of the bridged outputs operate into 50 ohm loads. The output risetimes and falltimes are typically 1.5nSec, and their shapes are unaffected by the loading conditions of the other outputs.

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2. Phillips Scientific Gate & Delay Generator Model 794 Data Sheet. Cover

Phillips Scientific

Quad Gate/Delay Generator

NIM MODEL 794

FEATURES

* Four Independent Gate/Delay Channels
* Wide Range, 50 nSec to over 10 Seconds
* NIM, TTL Inputs; NIM, TTL, ECL Outputs
* Deadtimeless Operation
* Set/Reset Flip-Flop Mode
* Remote Programming via a 0 Volt to 10 Volt Input
* Easily Configured as an Oscillator or a Pulser
* Provides Bin Gate for Host NIMBIN

GENERAL DESCRIPTION

The Quad Gate/Delay Generator, Model 794, complies fully with the NIM specification TID-20893 and is packaged in a single width module. In monostable mode, Gate/Delay periods may be adjusted either locally or remotely from less than 50nSec to more than 10 seconds. Each channel also operates in a Set/Reset flip-flop mode. A bright LED indicates an active gate condition. Versatile input and output structures provide compatibility with NIM, ECL, and TTL standards. Further flexibility is afforded by programming jumpers mounted on the printed circuit board. These jumpers allow selected inputs and outputs to be assigned alternate logic functions or polarities.

Time-Base Section

The model 794 time-base circuit is non-updating and exhibits essentially no deadtime. Monostable Gate/Delay periods are selected by a combination of the RANGE switch and an analog programming input. A monitor test point provides a 0 to 1 Volt output which is proportional to the Gate/Delay period. Setting the Gate/Delay period with an oscilloscope is easily accomplished by pushing the TRIGGER pushbutton. Depressing this switch for more than 0.5 seconds causes the time-base to retrigger at a 1 KHz rate. In the bistable mode, the Gate/Delay period is equal to the interval between the arrival of the trigger and reset functions. The DELAY output always occurs at the trailing edge of the GATE output and it's output width may be adjusted by a front panel potentiometer.

Input Section

There are three ways to trigger the Model 794: (1) TRIGGER Input; (2) OR Input; (3) TRIGGER pushbutton. These functions are enabled in both monostable and bistable modes.

(1), The TRIGGER input is compatible with both positive TTL levels and negative NIM logic. This input presents a high impedance to positive signals and 50 ohms to negative signals. The time-base triggers on the leading edge of the input pulse regardless of its logic type. The gate period is independent of the TRIGGER pulse width.

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3. ORTEC Octal Gate and Delay Generator Data Sheet.

ORTEC®

GG8020

Octal Gate and Delay Generator

- **For adjusting the delay and width of coincidence and gating pulses**
- **Eight, independent, duplicate channels in a compact package**
- **TTL outputs and NIM-standard fast-negative outputs**
- **Output delays independently adjustable from 70 ns to 10 µs**
- **Output widths independently adjustable from 70 ns to 10 µs**

The ORTEC model GG8020 Octal Gate and Delay Generator provides a compact and versatile solution for gating and coincidence logic requirements in large experiments, or in measurements requiring multiple delays and pulse widths. It contains eight independent channels of gate and delay generators in a single-width NIM module.

Each channel accepts NIM-standard, fast negative logic pulses at its input. The leading edge of the input signal triggers a delay period that can be adjusted separately for each channel. At the end of the delay period, an output pulse is generated. The width of this output pulse can be adjusted independently for each channel. Delay ranges from 70 to 1000 ns, or from 0.4 to 10 µs can be selected separately for each channel by one of eight jumpers on the printed wiring board. A second set of eight jumpers independently select ranges from 70 to 1000 ns, or 0.4 to 10 µs for the output pulse widths.

Each channel produces two NIM-standard, fast negative logic pulse outputs, and one positive TTL output. The fast negative outputs provide fan-out capability, and are particularly useful for driving overlap coincidence modules that require NIM-standard, fast negative logic levels. They can also be used as delayed inputs to timing instruments, or as gating signals on modules that require fast negative inputs. The TTL output is compatible with modules requiring either TTL inputs, or NIM-standard, slow positive logic pulses. The TTL output is ideal for gating ADCs and multichannel analyzers.

Specifications

PERFORMANCE

NUMBER OF DUPLICATE CHANNELS 8

OUTPUT DELAY Adjustable from <70 to >1000 ns, or from <0.4 to >10 µs. Temperature coefficient <0.04%/°C from 0 to 50°C.

OUTPUT PULSE WIDTH Adjustable from <70 to >1000 ns, or from <0.4 to >10 µs. Temperature coefficient <0.04%/°C from 0 to 50°C.

DEAD TIME Typically equal to the Delay plus the Output Pulse Width plus 20 ns.

DELAY JITTER <0.04% of the selected delay.

CONTROLS

DELAY, S OR L Eight jumpers on the printed wiring board permit independent selection of a Short (S) or Long (L) delay time range for each channel. The delay range is 70 to 1000 ns on the Short setting and 0.4 to 10 µs on the Long setting.

DELAY Eight front-panel, 12-turn, screwdriver adjustments provide independent fine adjustment of the delay within the range selected by the respective S OR L DELAY jumper.

WIDTH, S OR L Eight jumpers on the printed wiring board permit independent selection of a Short (S) or Long (L) width range for each channel. The width range is 70 to 1000 ns on the Short setting and 0.4 to 10 µs on the Long setting.

WIDTH Eight front-panel, 12-turn, screwdriver adjustments provide independent fine adjustment of the width within the range selected by the respective S OR L WIDTH jumper.

INPUTS

IN Eight front-panel LEMO connectors (one for each channel) accept NIM-standard fast negative logic signals to trigger the delayed output pulses. The input pulse minimum amplitude is –600 mV; minimum width is 10 ns. The input is dc-coupled with a 50-Ω input impedance.

OUTPUTS

OUT Two front-panel LEMO output connectors for each channel deliver NIM-standard, fast negative logic signals. The output delay relative to the input is set by the DELAY adjustment, and the output duration is set by the WIDTH control. The outputs are typically –16 mA (–800 mV into a 50-Ω load), with rise and fall times <4 ns.

TTL One front-panel LEMO connector for each channel delivers a TTL version of the signal from the OUT connectors. The TTL output provides <+0.4 V in the quiescent state, and nominally +4 V into a 50-Ω load during the output pulse. The rise time is <20 ns.

ELECTRICAL AND MECHANICAL

POWER REQUIRED The model GG8020 derives its power from a standard NIM bin and power supply. The required power is +6 V at 150 mA, and –6 V at 2 A.

WEIGHT
Net 1.3 kg (2.8 lb)
Shipping 2.2 kg (4.8 lb)

DIMENSIONS NIM-standard, single-width module, 3.43 x 22.13 cm (1.35 x 8.714 in.) front panel per DOE/ER-0457T.

Ordering Information

To order, specify:

Model	Description
GG8020	Octal Gate and Delay Generator

Specifications subject to change
080417

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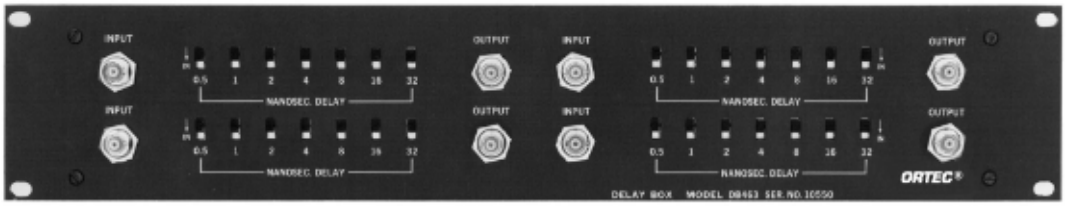
4. ORTEC Delay Box DB463

ORTEC®

DB463
Delay Box



- **Aligns fast-timing channels that incorporate coincidence circuits or TACs**
- **Four independent sections**
- **50-Ω calibrated cable delay for linear or logic signals**
- **0 to 63.5-ns delay in 0.5-ns steps**

The ORTEC Model DB463 furnishes a 50-Ω calibrated cable delay, providing relative delays from 0 to 63.5 ns with 0.5-ns increments in each of four identical sections. Longer delays may be achieved by cascading several Model DB463 Delay Box sections.

The Model DB463 is convenient for aligning fast-timing channels that incorporate coincidence circuits or time-to-amplitude converters.

Specifications

INPUTS (4) 50 Ω; either polarity; 1500 V maximum. BNC connectors.

OUTPUTS (4) 50 Ω; delay between In and Out is sum of delays. BNC connectors.

DELAY TIMES 0.5, 1, 2, 4, 8, 16, and 32 ns.

DELAY ACCURACY <±0.1 ns or ±1.0% for each switch, whichever is greater.

REFLECTIONS <3% at any delay setting for 1-ns rise time step.

CABLE RG-58A/U.

WEIGHT
Shipping 4.0 kg (9 lb).

DIMENSIONS 48.2 cm (19 in.) wide for relay rack mounting, 8.9 cm (3.5 in.) high, and 20.3 cm (8 in.) deep.

Ordering Information

To order, specify:

Model	Description
DB463	Delay Box

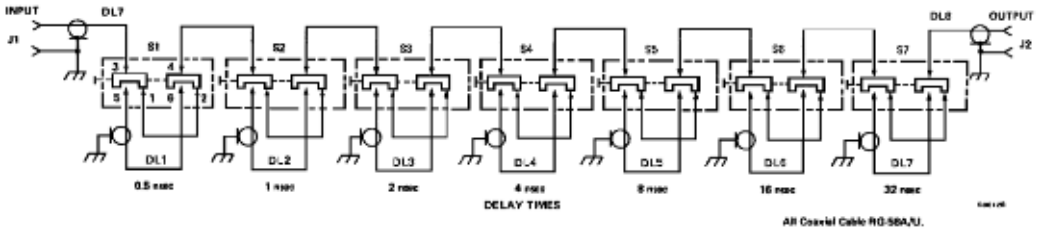


Fig. 1. Typical Schematic for One Section of Model DB463 (Four Sections Included).

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17-0720

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5. Phillips Scientific Quad Two-Fold Logic Unit Model 752 Data Sheet. Cover

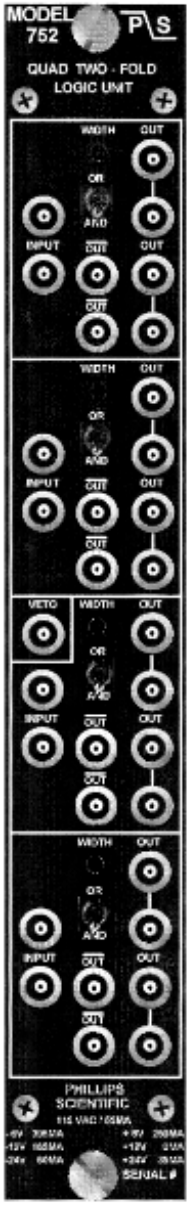
Phillips Scientific

Quad Two-Fold Logic Unit

NIM MODEL 752

FEATURES

- *150 MHz Rate Capability*
- *Four Independent Channels*
- *High Fan-Out with Six Outputs per Channel*
- *Deadtimeless Updating Operation*
- *One NanoSecond Input Overlap Width*
- *Fast Veto and Bin Gate Inhibiting*



DESCRIPTION

The model 752 is a high-performance, four channel, two-input logic unit packaged in a single width NIM module. It performs logical AND, OR, fan-in and fan-out functions.

Each channel has two logic inputs, a two position switch for selecting the logic function desired, an output width control, and six outputs. A fast veto is common to all four channels which permits anti-coincidence decisions. In addition, a bin gate applied via the rear panel connector inhibits the entire module and is enabled or disabled from a rear panel slide switch. After the inputs have satisfied the logic function desired, triggering of an updating regenerative stage produces a standardized output pulse, independent of the input pulse shapes or overlap times. Output durations are continuously variable over the range of 4nSec to 1μSec. The updating design ensures deadtimeless operation, while the double-pulse resolution is 6.5nSec for fast counting applications.

The 752 has six high-impedance current switching outputs per channel. They are configured as two pairs of double-amplitude bridged outputs and two complemented NIM levels. When only one output from the bridged pair is used, a double-amplitude NIM pulse (-32mA) is generated for driving long cables with narrow pulse widths. Two normal NIM levels are produced when both of the bridged outputs operate into 50 ohm loads. The output risetimes and falltimes are typically 1.5nSec, and their shapes are virtually unaffected by the loading conditions of the other outputs.

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6. ORTEC Linear Gate Model 426

ORTEC®

426
Linear Gate

- **For passing and blocking analog signals in the range from +0.2 to +10 V**
- **Ungated or gated with coincidence or anticoincidence gating**
- **External or internal control of gate pulse width**

The ORTEC Model 426 Linear Gate provides a variable gate duration with width controlled by a single-turn front-panel-mounted potentiometer. The nominal gate duration is from 0.3 to 4 µs. Operation of the linear gate is controlled by a positive enable pulse. It is useful for selecting or inhibiting linear signals according to chosen coincidence or timing requirements.

The ORTEC Model 426 has two operating modes: all input signals not accompanied by an enable pulse are blocked or all signals are passed unless accompanied by an inhibit signal. The inhibit signal can be fed into the front- panel Enable connector for Pulse Inhibit operation or into the DC Inhibit connector for dc or continuous inhibit operation. The DC Inhibit mode provides external control of the gating period.

Specifications

PERFORMANCE

GAIN Unity.

INTEGRAL NONLINEARITY <±0.15% from 0.2 to 10 V.

PULSE FEEDTHROUGH <10 mV with a 10-V input pulse.

TEMPERATURE INSTABILITY <±0.015%/°C, 0 to 50°C.

COUNTING RATE The gain shift of a 4-V reference pulse is <0.25% with the application of an additional count rate of 65,000 counts/s of 6-V random pulses.

CONTROLS

GATE WIDTH Continuously variable from 0.3 to 4 µs.

OUTPUT PEDESTAL Adjustable to <1 mV.

PULSE INHIBIT/NORM/DC INHIBIT 3-position mode switch permits selection of the function of any pulse or dc level furnished through the front-panel Enable Input connector, or the rear-panel DC Inhibit connector.
Norm Input pulse will be gated through to the output during a gate width interval following the leading edge of each Enable Input pulse.
Pulse Inhibit Input pulses will be inhibited from passing through the output during a gate width interval following each Enable Input pulse.
DC Inhibit Input pulses will be inhibited from passing through the output during intervals of pulses or dc levels through the rear-panel DC Inhibit connector.

INPUTS

LINEAR INPUT Unipolar or bipolar with positive portion leading. Rated range 0.2 to 10 V, 12 V maximum. Input impedance >5000 Ω; BNC connector. Input is ac-coupled with a passive symmetric baseline restorer. BLR can be bypassed for dc-coupling.

ENABLE OR INHIBIT INPUT Any positive input >2 V, maximum input 20 V. Enable impedance 1000 Ω, dc-coupled; Inhibit impedance 650 Ω, dc-coupled; BNC connector for each.

OUTPUT

Rated output range 0.2 to 10 V positive; 12 V maximum. Output impedance −2 Ω, dc-coupled, short-circuit protected; BNC connector.

ELECTRICAL AND MECHANICAL

POWER REQUIRED The Model 426 derives its power from a standard NIM bin/power supply. The power required is +24 V, 30 mA; −24 V, 49 mA; +12 V, 16 mA; −12 V, 4.9 mA.

WEIGHT
Net 0.96 kg (2.1 lb)
Shipping 1.82 kg (4.0 lb).

DIMENSIONS NIM-standard single-width module 3.43 X 22.13 cm (1.35 X 8.714 in.) per DOE/ER-0457T.

Ordering Information

To order, specify:

Model	Description
426	Linear Gate

Specifications subject to change
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