AN-1487 Current Mode Hysteretic Buck Regulators

ABSTRACT

Texas Instruments has developed a family of peak current mode hysteretic buck regulator controllers (such as the LM27212, the LM27213, and the LM27292, and so forth). This architecture has some characteristics that differ from its PWM counterpart. This application report highlights some of these unique characteristics and discusses the tradeoffs involved.

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1   Basic Architecture

Roughly speaking, hysteretic or PWM is just a matter of timing, that is, how the ON/OFF of the top switch is controlled for a given control signal (current command). In other words, the difference lies in how the inductor ripple current is generated.
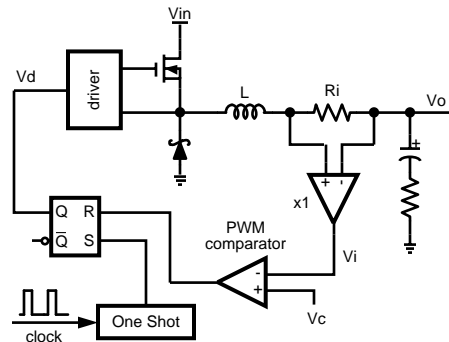

Figure 1.

For the falling edge PWM architecture shown in Figure 1, the timing of the rising edges (t1, t2, t3, and so forth) in Figure 1) is fixed while that of the falling edges is set by the control voltage Vc (also known as the "current command"). The appearance that the valley points in Vi are all sitting at the same level V2 is a result of steady state operation. The Vi ripple amplitude will change when any combination of V_{IN}, V_{OUT}, and inductance changes.
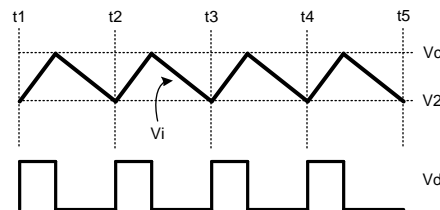

Figure 2. Falling Edge PWM Architecture

For the hysteretic architecture shown in Figure 3, timing of both edges varies, but both peak and valley of the inductor current are explicitly controlled (Vc and V2). The appearance that t1, t2, t3, and so forth are evenly spaced in time is a result of steady state operation. It is inherently a variable frequency architecture.
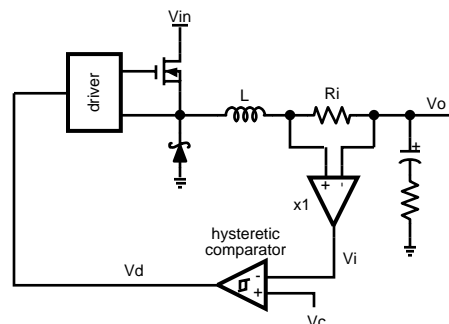

Figure 3. Hysteretic Architecture

So in a nutshell, the fundamental difference between the two approaches lies in how switching action is generated once the desired inductor current (Vc) is known. Is it by forcing the switching frequency (PWM) or is it by forcing the current ripple amplitude (hysteretic)? Another name for the hysteretic architecture is the "ripple regulator".

Both approaches provide near instant responses to changes in the control voltage. So in most cases of small signal analysis, the inductor can simply be replaced by a voltage controlled current source, resulting in a simple control-to-output model shown in Figure 4.
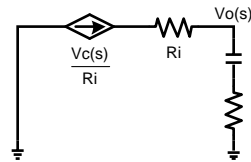

Figure 4. Voltage Controlled Current Source

To construct the circuit as a voltage regulator, the control voltage Vc should respond in some manner to the error voltage (difference between the properly ratioed output voltage and the reference voltage) so that inductor current is continuously adjusted to keep the output voltage regulated. The following figure shows such an example.
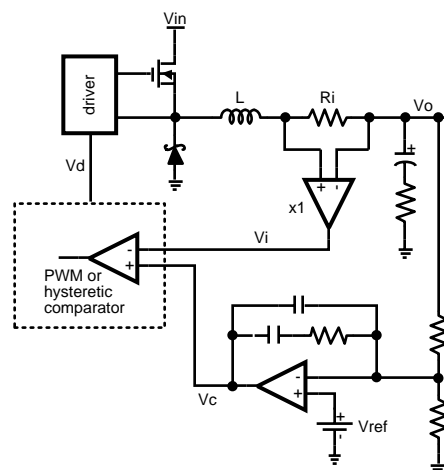

Figure 5.

One subtlety though, is that at half the switching frequency the PWM architecture has a peaking in its control-to-inductor-current frequency response. That is, when the frequency in question is close enough to the switching frequency, the inductor is no longer a 1-to-1 voltage controlled current source, instead it has significant gains.
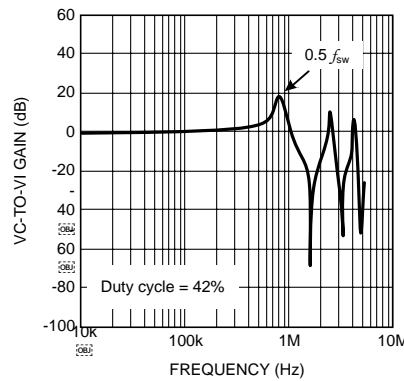
Figure 6.

This is because when Vc frequency approaches half the switching frequency, the valley (the "free end") of the inductor current can vary significantly from cycle to cycle, as shown in Figure 7. This peaking becomes infinite when the duty cycle exceeds 50%. But even if the duty cycle is below 50%, an improperly designed voltage loop can still make the peaking cross 0dB in the final loop gain, resulting in sub-harmonic oscillations.
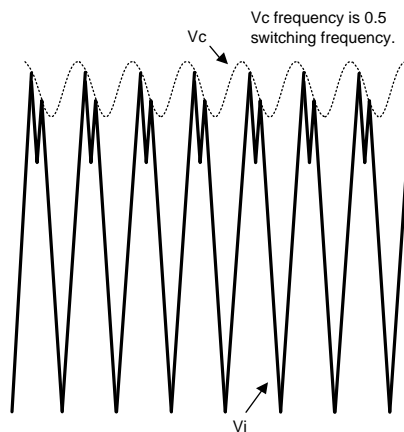
Figure 7. The Valley of the Inductor Current

The hysteretic architecture does not have this behavior. This is because the peak and valley are both bounded by the Vc and its hysteresis, therefore the gain is always close to 1 below the switching frequency. From the small signal point of view, the control-to-inductor-current characteristic is intrinsically nonlinear. So the voltage loop bandwidth can be designed to be close to the switching frequency, and the duty cycle can safely exceed 50% without the slope compensation needed by the PWM regulator.

Figure 8.

Figure 9.

2   Switching Frequency

To estimate the switching frequency of a hysteretic buck regulator in the continuous conduction mode (CCM) is not difficult. If the hysteresis window, the input and output voltages and the inductor value are given, the theoretical switching frequency should be:
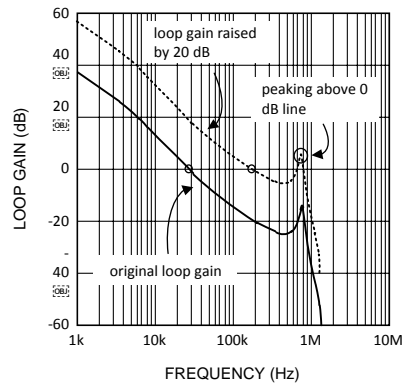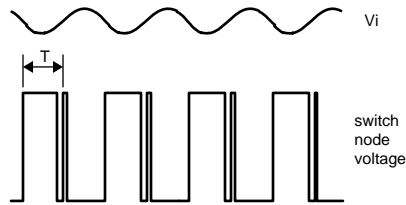
$$f = \frac{1}{\frac{2ih}{S_1} + \frac{2ih}{S_2}} = \frac{1}{2ih \cdot L \left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}} \right)}$$

(1)

For example, if V_{IN} = 12 V, V_{OUT} = 1.2V, L = 1 µH, total hysteresis window 2ih = 6A, then the theoretical switching frequency should be

$$f = \frac{1}{6A \cdot 1\,\mu H \left(\frac{1}{12V - 1.2V} + \frac{1}{1.2V} \right)} = 180\ kHz$$

(2)

In many applications, the allowed ripple voltage size is a fixed number (for example, ±10 mV). So one potential benefit of the hysteretic approach is the switching frequency only needs to be high enough to maintain a constant ripple size. In the above example, if V_{IN} goes down to 5V, switching frequency will drop to 152kHz, reducing the switching loss. This contrasts with the PWM architecture where the switching frequency is fixed and the size of the inductor current ripple varies as V_{IN}, V_{OUT} and L vary.
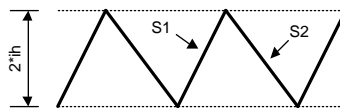

Figure 10.

Some applications require the switching frequency be set to a fairly narrow range so as to avoid certain sensitive frequencies. In those cases, the PWM is the better choice, especially if the V_{IN} range is large.

If a power supply design uses only ceramic capacitors at the output, output voltage ripple size will vary as the switching frequency varies. This is because the impedance of the capacitors changes over frequency with a rate of 20dB per decade. So use extra care when the impedance of the output capacitors is not dominated by the ESR over the intended switching frequency range.

Since the switching frequency of a hysteretic is inexplicitly controlled, some other factors may also contribute to the actual frequency. One such factor is system delay. The delay td in the figure below slows down the switching frequency. The degree by which the switching frequency is reduced may not be consistent across the entire V_{IN} and V_{OUT} ranges. But the impact of this delay is lower at lower frequencies. The delay itself may not be a constant duration, either. At least the delay introduced by the comparator has to do with how fast the two inputs to the comparator approach each other.
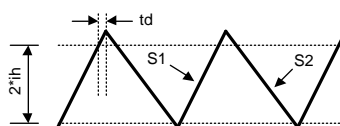

Figure 11.

Another factor is the self inductance of the current sense resistor. This is negligible if the main inductor or the sense resistance is large enough. This is clear in the following figure. The voltage between Vo and Vsw is a pulse train. The main inductor L and the self inductance of the sense resistor Lr form a voltage divider at the switching frequency and above. For a 2512 size current sense resistor, the Lr value is around 1 nH when mounted on a PCB. So if L = 1 µH and V_{IN} = 12 V, the mini pulse train across the Lr will have a magnitude of 12 mV peak-to-peak. This results in significant "jumps" in the voltage across the resistor, which will increase the switching frequency. If V_{IN} varies a lot such as in a battery powered circuit, it is desirable to eliminate this effect because it "distorts" the switching frequency differently at different V_{IN} levels.
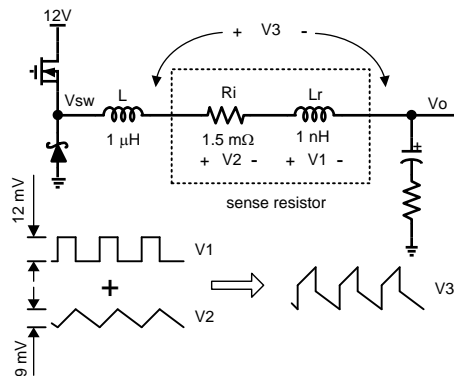

Figure 12.

This effect can be eliminated with an RC network as shown in Figure 13. The idea is if the time constant of the RC network is equal to that of the LR network, then the voltage across the capacitor will be exactly equal to that across the Ri. This effect is prominent in high current low voltage applications where the main inductor tends to be below 1µH. It is a good idea to use a C0G capacitor for this purpose to make sure the equation roughly holds over the entire temperature range.
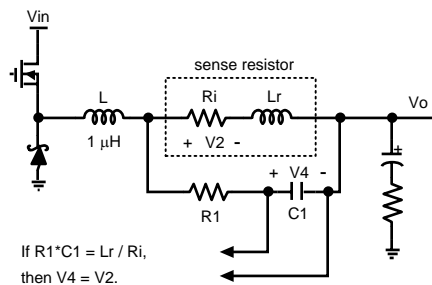
Figure 13. RC Network

3   Light Load Operation

If the inductor current is not allowed to go negative, such as in a non-synchronous buck regulator or in a synchronous buck regulator with the Diode Emulator feature, the switching frequency automatically droops as the load current goes below the critical conduction boundry. The lighter the load, the lower the switching frequency will be. The figure below is a case where the load current drops from 8A down to 0.3A. The benefit of this feature is improved efficiency at light loads due to reduced switching loss.
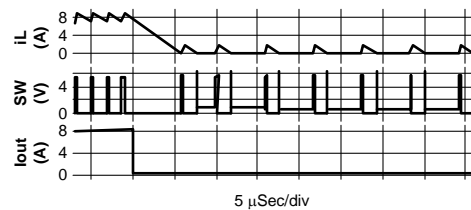
Figure 14.

The switching frequency in DCM can be estimated by Equation 3.

$$f = \frac{2I_O \bullet (V_{IN} - V_O) \bullet V_O}{(2ih)^2 \bullet L \bullet V_{IN}}$$

(3)

The PWM architecture can also achieve a similar mode with some additional circuitry. In the PWM terminology, that mode is called "pulse-skipping" mode. Without the pulse-skipping circuitry, the switching frequency will stay the same even in DCM.

4 Load Transient Response

Difference between the hysteretic architecture and its PWM counterpart in terms of load transient response only shows itself in large and fast load transients such as those of modern CPUs. For a falling edge modulation PWM, once the top switch has been turned 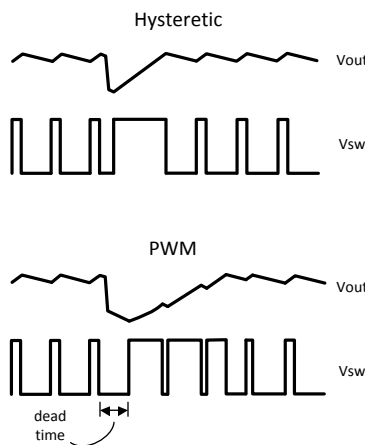off, it won't be turned on again until the next clock cycle comes. So there is a dead time during which the PWM does not respond to any transient event. For the hysteretic, there is no such a dead time. Figure 15 shows such a subtle difference between the two responses to the same load step.

Figure 15. Load Transient Response

5 Multiphase Operation

Since the hysteretic architecture does not have a clock, it is less obvious to achieve multiphase operations. One approach is the rotation scheme used in the two-phase controllers, the LM27212 and the LM27292. Figure 16 reveals the mechanism. The idea is instead of turning on the top switch in the same channel when the channel current hits the lower threshold of the hysteresis window, turn on the top switch in the other channel. That way the channels take turns to fire the top switch and because there is no "discrimination" against any particular channel, the channels should be evenly distributed in time.
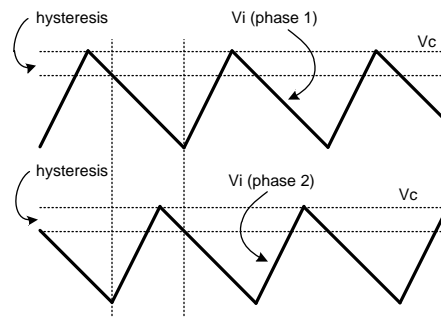
Figure 16. Multiphase Operation

One prominent feature of the LM27292 hysteretic controller is the phase shedding and restoration capability. The IC allows one of the two phases to be turned off and back on, on the fly, to achieve the highest efficiencies at different load levels. One of the challenges to achieve that feature is to ensure that the output voltage is not affected during the transition period. The peak current mode hysteretic architecture lends itself well to making the transitions smooth. In our tests, the output voltage does not move at all during the phase shedding and restoration transitions, other than a slight change in ripple voltage size due to the ripple cancelling effect or lack of it.

The phase rotation scheme mentioned above has a limitation on the achievable maximum duty cycle. That is, each phase has a theoretical maximum duty cycle of 1/n, where n is the number of phases in operation. So the application's voltage conversion ratio (V_{IN}/V_{OUT}) should not be less than n. For our single-phase hysteretic controllers, such as the LM27213, that limitation is nonexistent because n is 1. For the two-phase controllers, the maximum allowed duty cycle is 50%. Another consideration is the load transient response, since no two phases can be ramping up inductor currents simultaneously, the response to a large and ultra-fast step-up load transient may not be as good as what the power train could generate. But many a time this is not a concern, especially in modern CPU applications, because the load steps are of the same magnitude in both directions, making the step-down load transient more challenging due to lack of available voltage to ramp down the inductor currents. Roughly speaking, if the number of phases is less than half the conversion ratio, the step-down load transient will generate more excursion in the output voltage. For more details, see Appendix A. For our two-phase hysteretic controllers, if the voltage conversion ratio is greater than 4, the step-down load transient will generate more output voltage excursion than the step-up. In applications where the load transient is not as aggressive as that of modern CPUs, there's no need to consider this very subtle effect at all.

Appendix A Step-Down Load Transient Guidelines

To roughly determine whether a step-up load transient or a step-down load transient is the worse case in terms of output voltage excursion, the following derivation provides a guideline. The assumption is that at any instant only one phase is ramping up its inductor current, and the rest of the phases are ramping down their inductor currents.

For the step-up load transient, the slew rate of the total current supplied by all the inductors is

$$V_{IN}/L - Vo/L \times n \tag{4}$$

or

$$V_{IN}L \times (1-D \times n) \tag{5}$$

Where n is the number of phases and D is the duty cycle during steady state operation.

For the step-down load transient, the slew rate of the total current sucked by all the inductors is

$$Vo/L \times n \tag{6}$$

or

$$V_{IN}/L \times D \times n \tag{7}$$

So for the step-down load transient to be a worse case, the following needs to be true:

$$V_{IN}/L \times (1-D \times n) > V_{IN}/L \times D \times n, \tag{8}$$

or

$$n < 0.5 /D \tag{9}$$

or

$$n < 0.5 \times r, \tag{10}$$

where r is the conversion ratio, which is equal to 1/D.

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