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Oriental Institute of Science & Technology, Bhopal

Department of Computer Science AND Engineering

LAB MANUAL (CS404)

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Enroll no. → 0105CS203D03
course code → cs404
Course → Computer org. & Architecture.
Session → JAN-JUN 2021
Section → 'B'

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Experiment - 1

Objective :- Study of multiplexer and demultiplexer

Theory :-

1) multiplexer :-

A multiplexer is a network that has many inputs and one output, and the value of the o/p will be the value of one of inputs which will be decided by some select lines. The simplest Type of multiplexer is two to one line data multiplexer. Let A be one of the inputs and B is the other input and Y is the output as in fig. (1) and S is the select line then

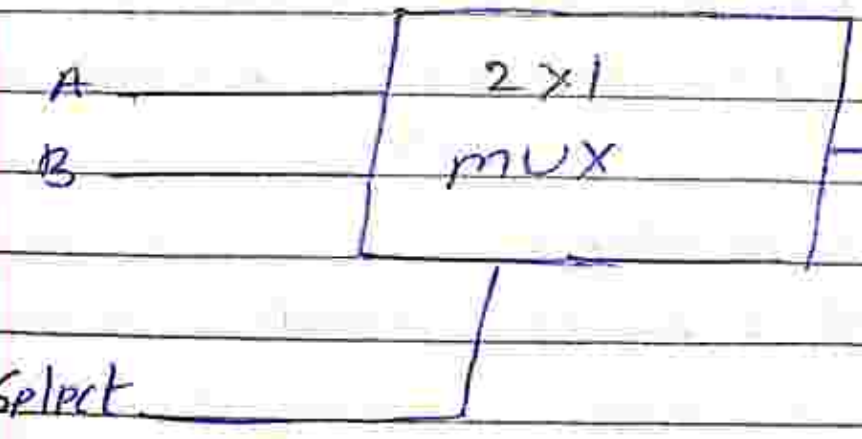

Fig. (1)
Two to one line multiplexer.

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$y = A$ if select $= 0$.
$y = B$ if select $= 1$.

The logic circuit diagram of the two to one line multiplexer is shown Fig. (2)

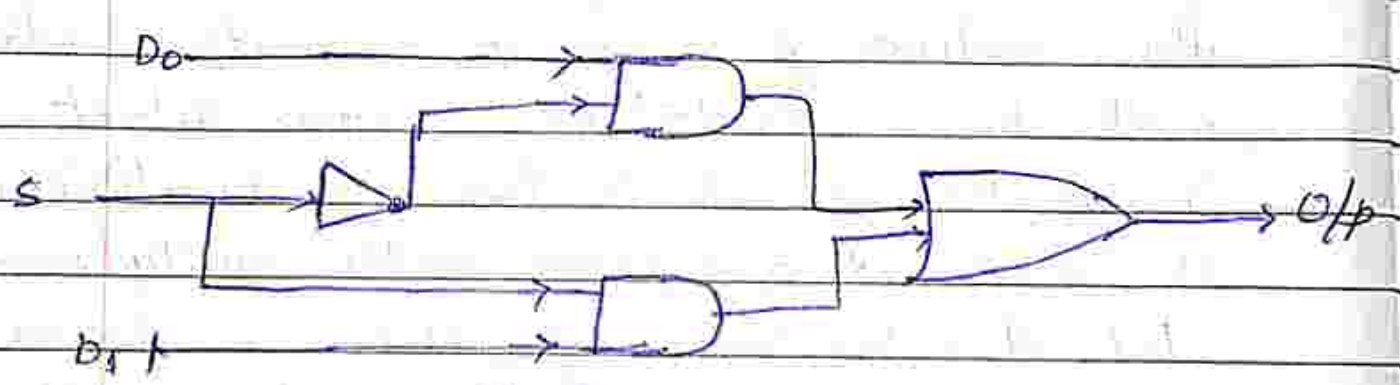

Fig (2)
logic circuit of two to one line mux.

⇒ Example: Design the following expression using multiplexer, i.e.

~~No of~~ variables = 3
$F = (A, B, C) = \bar{A}C + \bar{B}C + AB\bar{C}$

⇒ Solution:- No of variables = 3, It is better to use 4-to-1

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Line multiplex, i.e.
No of selection Lines = No of Variables - 1,

Truth Table

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

2.) Demultiplexer :-

A demultiplexer basically reverse of the multiplexer function. It is take data from one line and distribute them to given no. of output lines. Fig 13) Shown a one to four line demultiplexer circuit.

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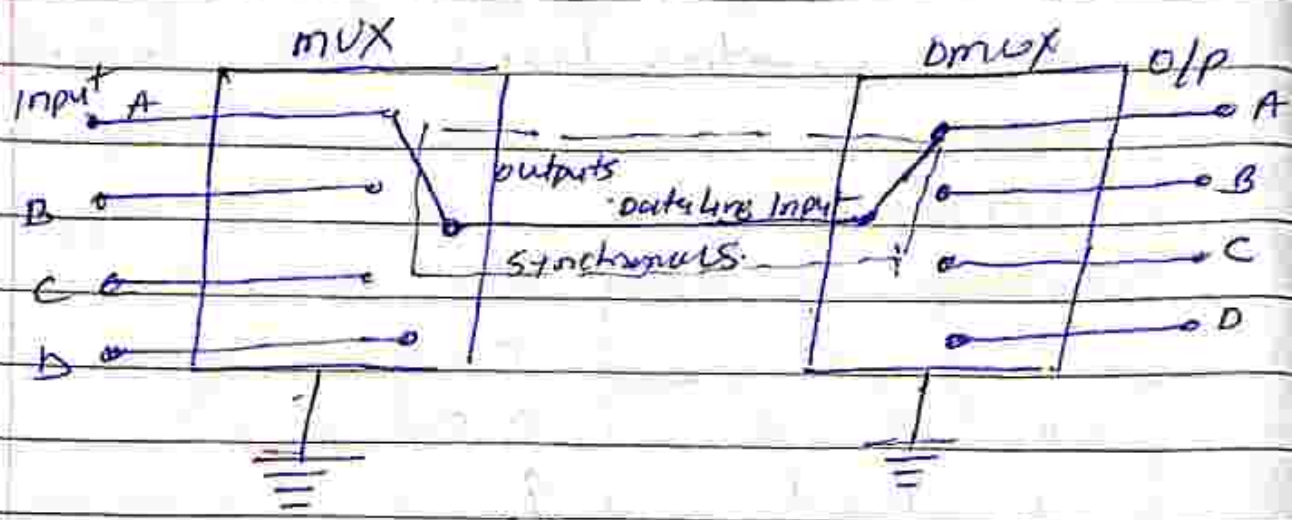

fig (3)

Experiment-2

⇒ study of Half Adder and Full adder

Theory:-

Half adder:-

A Half adder has two inputs for the two bits to be added and two outputs one from the sum 's' and other from the carry 'c' into the higher adder

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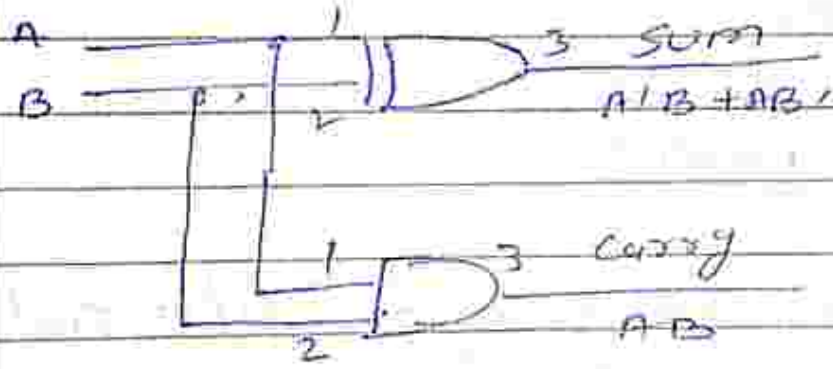
position. above circuit is called as a carry signal from the addition of the less significant bits sum from the X-OR Gate the carry out from the AND Gate.

⇒ Logic Diagram :-



Truth Table:

A	B	CARRY	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

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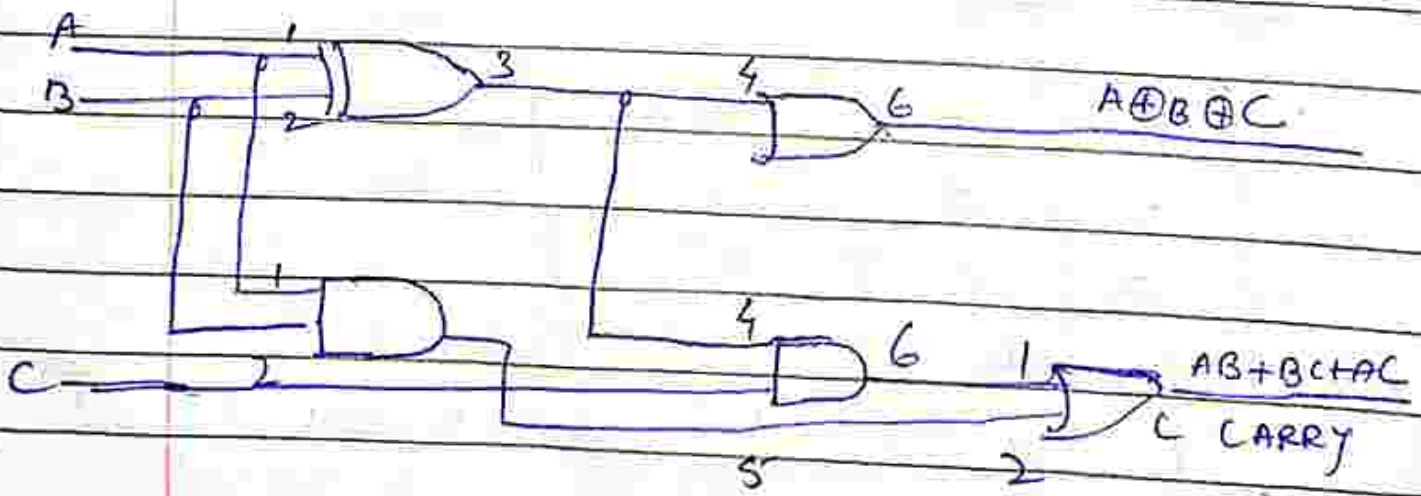
2) Full adder :-

A full adder is a combinational circuit that forms the arithmetic sum of input; it consists of three inputs and two outputs. In full adder sum o/p will be taken from X-OR gate, carry output will be taken from OR gate.

Logic diagram :-

Full adder using Two Half adder:-



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Truth Table :-

A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Experiment ⇒ 3

Objective :-

⊙ study of Half subtractor and full subtractor.

Theory :-

Half subtractor :-

The half subtractor is constructed using X-OR and AND gate. The half subtractor.

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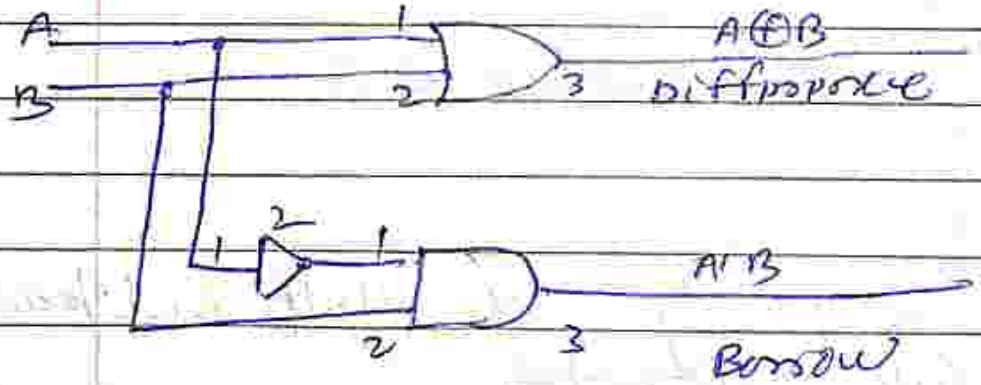
Has two input and two outputs. The outputs are difference and borrow. The difference can be applied using X-OR gate, borrow output can be implemented using an AND gate and an inverter.

→ Logic diagram :-

Half subtractor :-



⇒ Truth Table

A	B	Borrow	Difference
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

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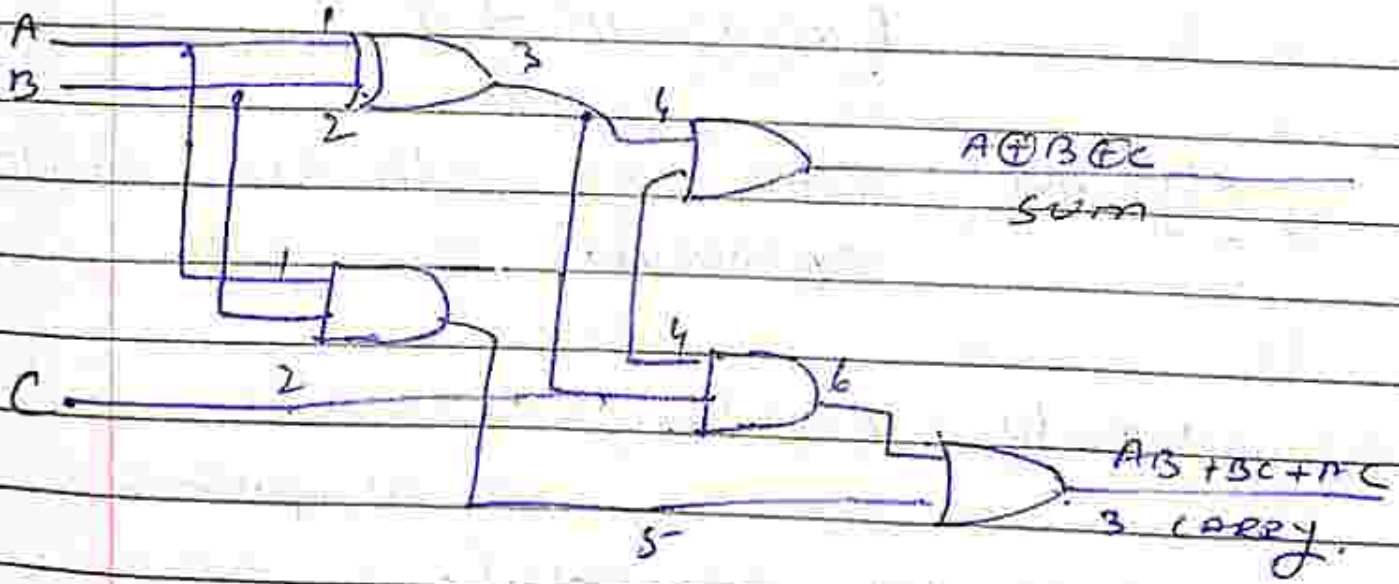
→ Full subtractor :-

The full subtractor is a combinational of XOR, AND, OR, NOT gates. In a full subtractor the logic circuit should have three inputs and two outputs. The two half subtractor put together give a full subtractor. The first half subtractor will be C and AB.

Logic diagram :-



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Truth Table:-

A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Experiment → 4

→ Objective: WAP To add two 16 bit operand.

→ Apparatus Required:- micro processor trainer kit, keyboard.

→ Program:

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Addition of two 8-bit Operands.

Address	OP code	MNEMONIC	comments
2000H	F8	CLC	Clear carry flg
2001-1	B0 10	MOV AL, 10H	Load AL with 8 bit data.
2003H	B3 20	MOV BL, 20H	Load BL with 8 bit data
2005H	00D8	ADD AL, BL	Add contents of AL and BL registers.
2007H	CC	INT 3	Interrupt Type3

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```
org     100h
mov     al, 11h
mov     bl, 11h
add     al, bl
mov     [2000h], al
```

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Experiment-5

Objective :- WAP To add two 16 bit operand.

(a)

program :-

memory	Address	MNEMONICS	comments
2000	LDA 2050		A ← 2050
2003	MOV B,A		B ← A
2004	LDA 2052		A ← 2052
2007	ADD B		A ← A+B
2008	STA 3050		A → 3050
200B	LDA 2051		A ← 2051
200E	MOV B,A		B ← A
200F	LDA 2053		A ← 2053
2012	ADC B		A ← A+B+CY
2013	STA 3051		A → 3051
2016	HLT		Stop execution

Explanation :-

LDA 2050 → stores the value at 2050 in A (accumulator)

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2) MOV B, A → stores the value of A into B registers.

3) LDA 2052 → stores the value at 2052 in A.

4) ADD B → adds the contents of B and A and store in A

5) STA 3050 → stores the value at 2051 in A

6) MOV B, A → stores the value of A into registers.

7) LDA 3053 → stores the value at 2053 in A

8) ADC B → adds the content of B, A and carry from the lower bit addition and store in A.

10) STA 3051 → store the result in memory location 3051

11) HLT → stop execution

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Experiment :- 6

⇒ Objective :- WAP to perform Arithmetic operation : Subtraction.

⇒ Apparatus Required :- Micro processor trained kit, Keyboard.

⇒ program :-

Subtraction of two 8-bit operands.

Address	op code	MNEMONIC	Comments.
2000H	F8	CLC	Clear carry flag
2001 H	B0 20	MOV AL, 20 H	Load AL with 8 bit data
2003 H	B3 10	MOV BL, 10 H	Load BL with 8 bit data
2005 H	29 D8	SUB AL, BL	Subtract content of AL and BL registers.
2007 H	CC	INT 3	Interrupt Type 3

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⇒ Subtraction of two 16-bit operands.

Address	Op code	MNEMONIC	comments
2000H	F8	CLC	Clear carry Flag
2001H	B8 00 20	MOV AX, 2000H	Load AX with 16 bit data.
2004H	BB 00 10	MOV BX, 1000 H	Load BX with 16 bit data
2007H	29 D8	sub AX, BX	Subtract content of AX & BX registers.
2009H	CC	INT 3	Interrupt Type 3.

Conclusion :-

All the programs are written and o/p are verified.

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Experiment - 7

Objective :- NAP to perform Arithmetic operation : multiplication, subtraction.

→ Apparatus Required :-

Micro processor trainer kit, keyboard.

multiplication of two 8-bit operands.

address	opcode	MNEMONIC	comments
2000H	F8	CLC	Clear carry flag
2001H	B0 20	MOV BL, 20H	load BL with 8 bit data
2003H	B0 10	MOV AL, 10H	load AL with 8 bit data
2005H	00 D8	ADD AL, BL	multi content of AL and BL registers.
2007H	CC	INTC	interrupt Type3

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org 100h
mov al, [2000h]
mov bl, [2001h]
mul bl
mov [2000h], ax.

Experiment :- 8

Objective :- WAP to perform Arithmetic operation : Division.

Apparatus required :-
Micro processor trainer kit, key board.

```
org 00h
mov [2000h], 02h;
mov [2001h], 08h;
mov [2002h], 0Fh;
mov al, [200h];
mov bl, [2002h];
mov cl, [2001h];
mov dl, [2000h];
ret
```

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Experiment :- 9

objective :- WAP to perform AND operation over two operands.

Apparatus Required :- micro processor trainer kit, keyboard.

program :-

```
org 00h
mov bx, 2000h;
mov si, 0h
mov cx, 10h
ll;
mov ax, [bx+si]
mov ax
mov [bx+si], ax;
inc si
dec cx;
Jnz ll
```

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Experiment - 10

Objective :- WAP to perform OR operation over two operands.

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Experiment :- 11

Objective :- Nap to store 16 Bit data information at 2000h and incrementing value by 01

APPARATUS REQUIRED :- Micro processor training kit, keyboard.

Program :-

```
org 100h

MOV AL, [2000H]
MOV CL, 08H
L1:
    ROL AL, 1
    JNC L2
    DEC CL
    JNZ L1
    JMP L3:

L2:
    MOV [2001H], 00H
    RET
L3:
    MOV [2001H], 00FFH
    RET
```

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Experiment :- 12

Objective :- WAP to perform more than one operation in one program.

APPARTUS Required :- Micro processor trainer kit, keyboard.

```
MOV  al, 10h
MOV  bl, 5h
AND  al, bl
MOV  [2000h], al

ADD  al, 20h
MOV  [2010h], bl
```

Thank you!!