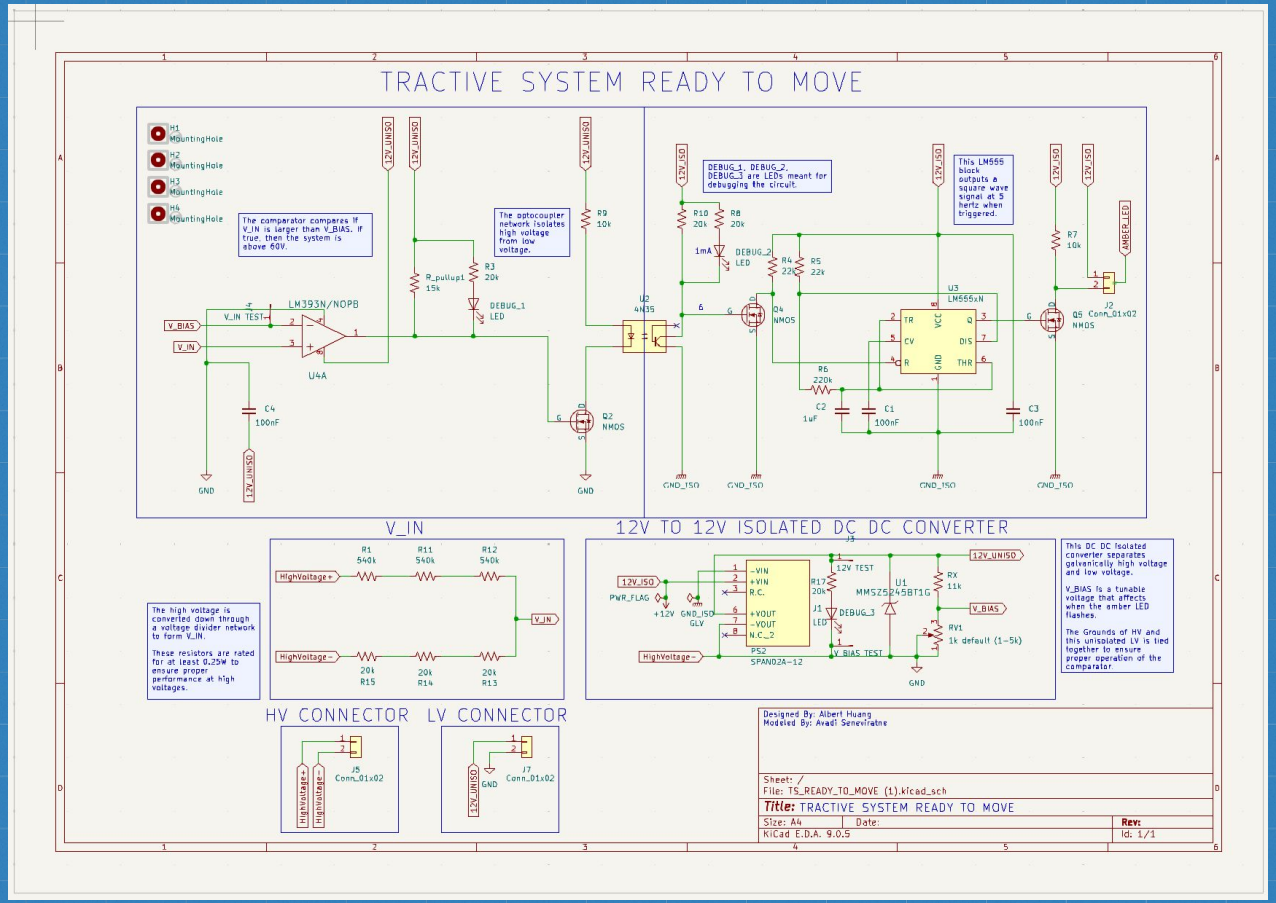
FSAE EV @ UCI
Anteater Electric Racing

RTM (Ready-To-Move) PCB Modifications

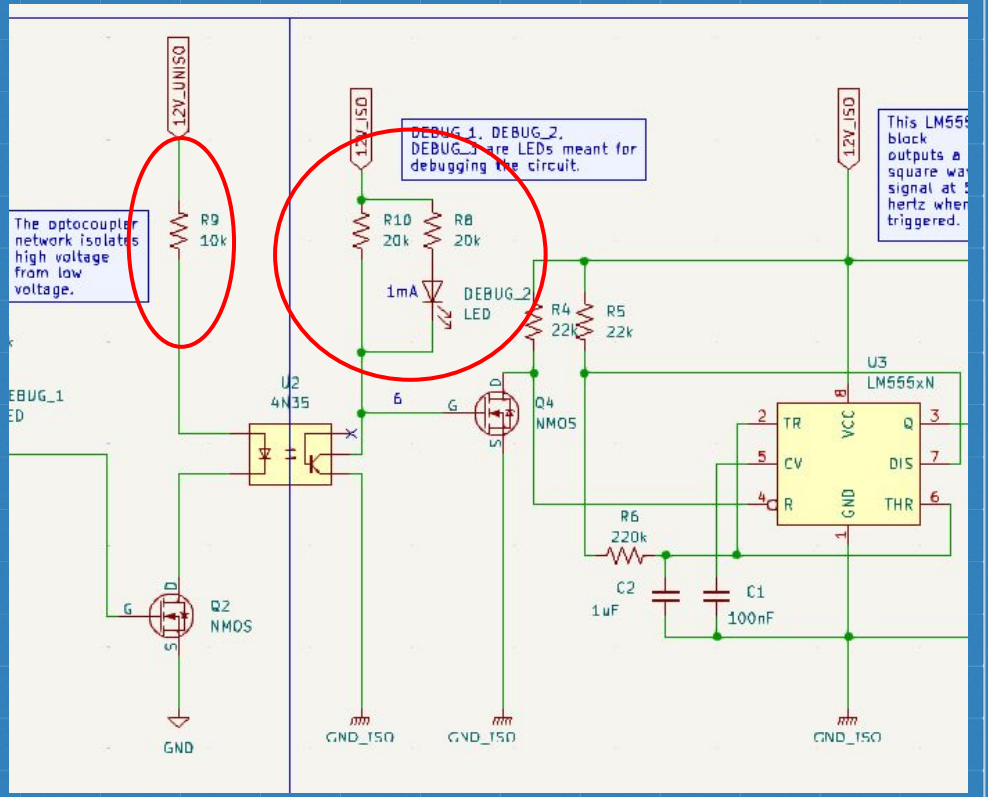
Andy Li

Current Schematic



Potential Issues

- Concern at the time was because I believed that the Q4 NMOS would always be on, leaving the Reset pin on the 555 timer always asserted (GND) -> LED signaling RTM never flashes



CTR of 4N35, Onsemi Datasheet

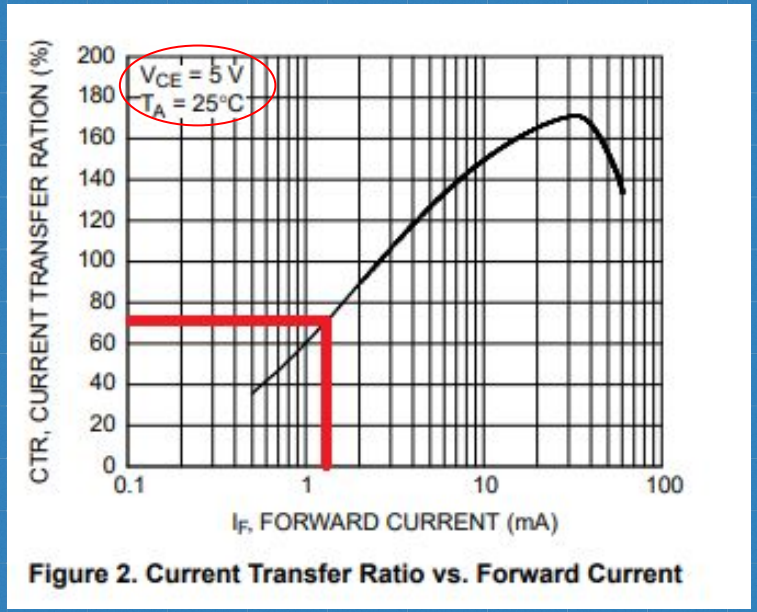
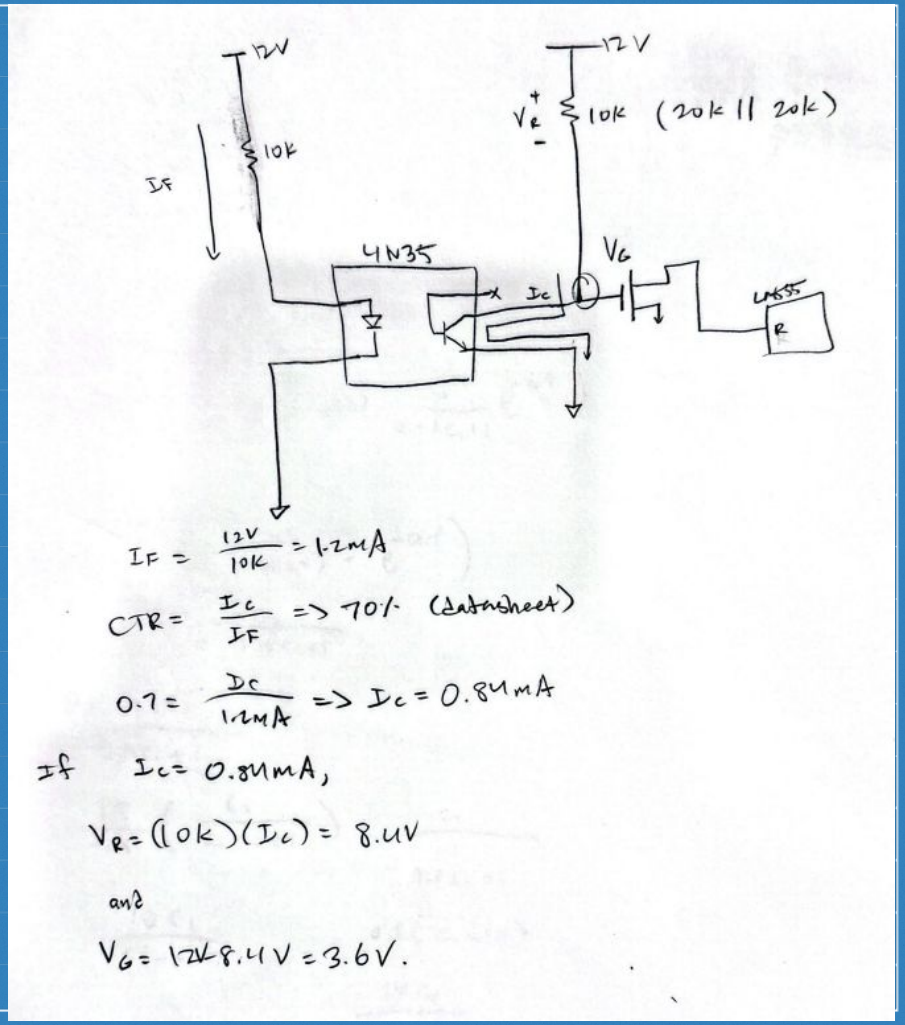


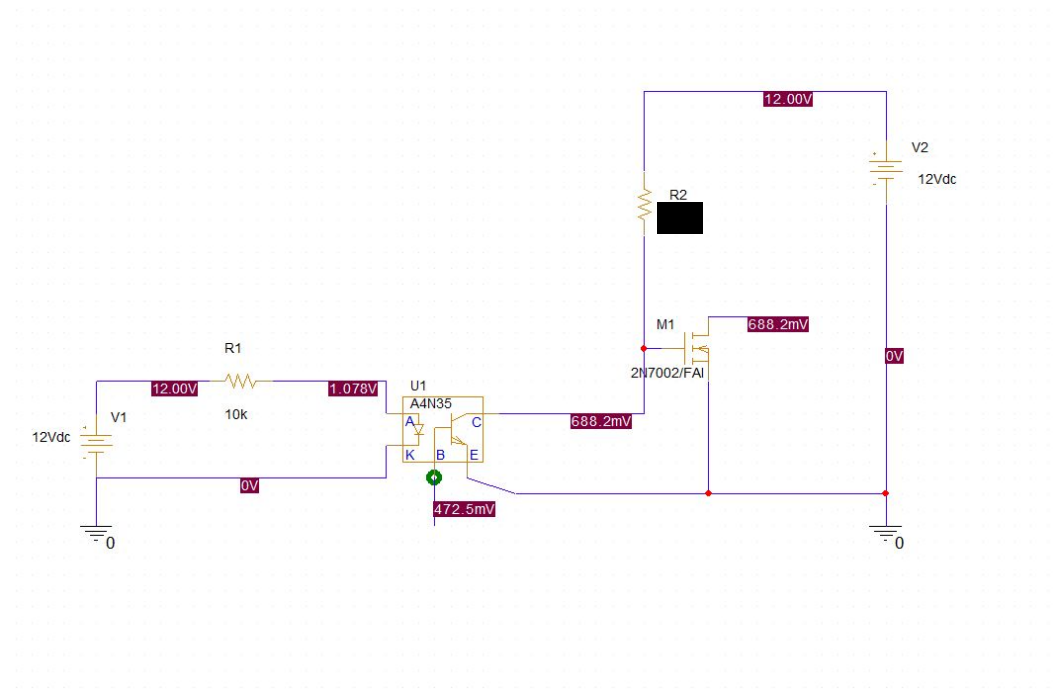
Figure 2. Current Transfer Ratio vs. Forward Current

https://www.onsemi.com/download/data-sheet/pdf/4n35-d.pdf

- If we take the onsemi datasheet to be true (V_{CE} = 5V), then CTR = 70% for I_F = 1.2mA
- When the system exceeds the predetermined 60V threshold voltage and the RTM LED should start blinking, the Q2 NMOS will turn on and the circuit should look like the one on the left
- The MOSFET needs to turn off to un-GND the Reset pin on the LM555, but it will not
- Hence my concern that the board does not work properly
    - However, because this CTR is for V_{CE} = 5V, and this may not be the case for the RTM, I decided to simulate the component in PSPICE, and this fortunately showed that the circuit will probably work



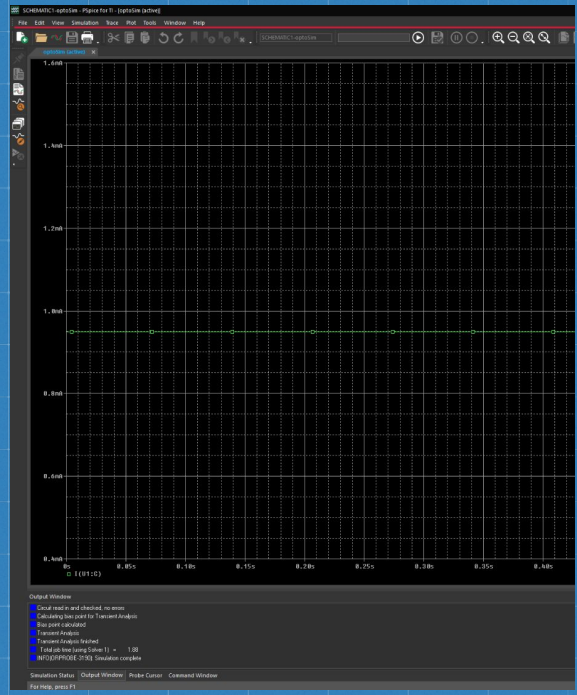
Simulation of Current Design



Circuit Being Used in PSPICE, generic MOSFET used

Simulation of Current Design

Q4 NMOS Gate-Source Voltage



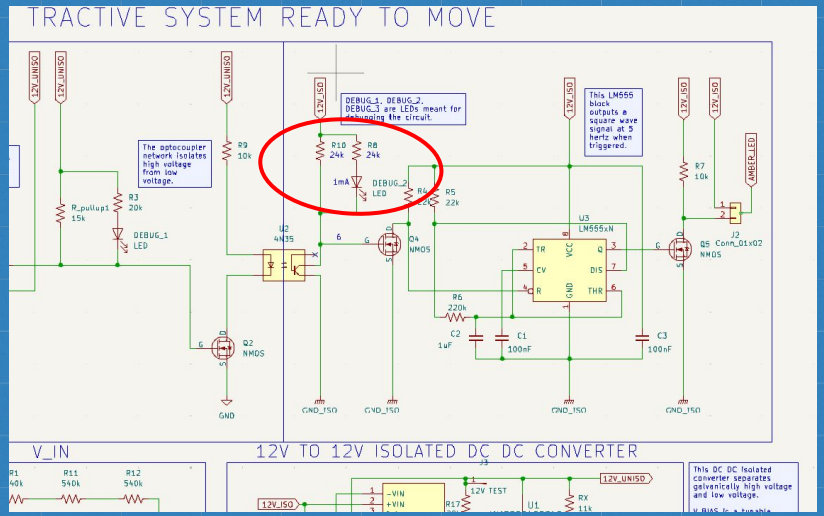
Current I_C Through 4N35 Optocoupler

Discussion

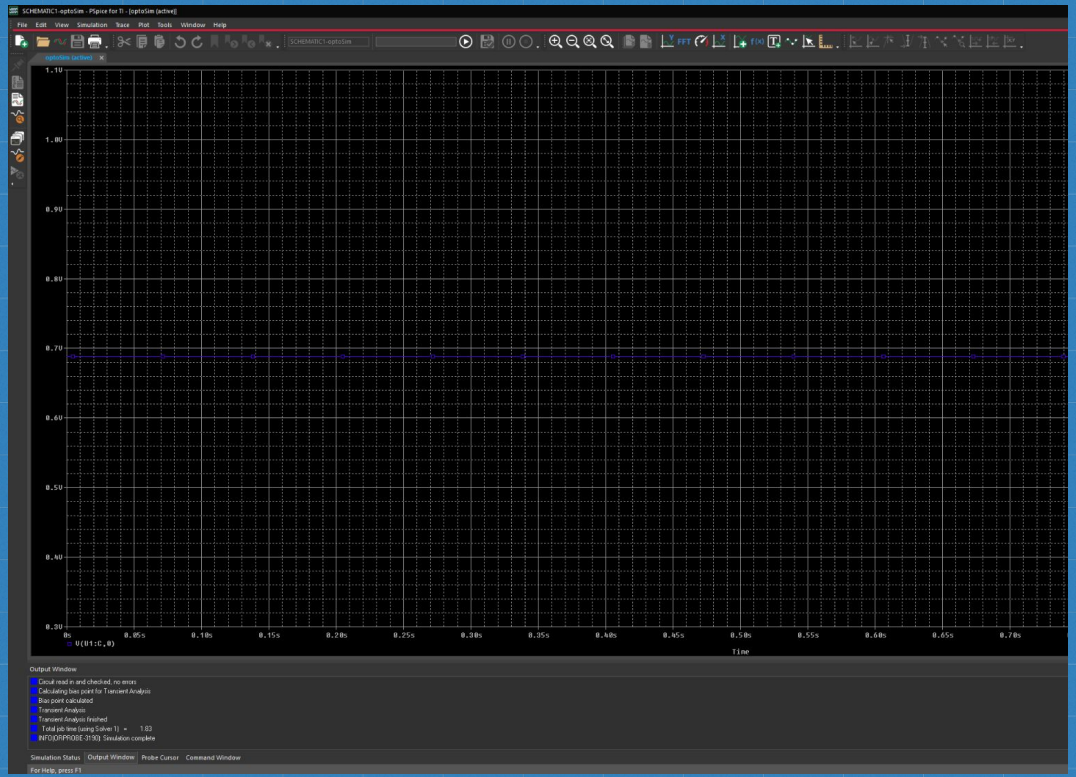
- Albert said that the V_{TH} of these MOSFETS is ~3V, so a 2.4V gate voltage should technically work for the MOSFET
  - This is probably why the PCB works right now
    - May also explain why Albert said that the board acted unusually without some additional components
  - This V_G = 2.4V leaves no margin for error; the MOSFET may not be fully off for V_{GS} = 2.4V, the true V_{TH} of the MOSFET may be lower, resistor tolerances could cause the gate voltage to increase beyond 3V, etc.

Improvements

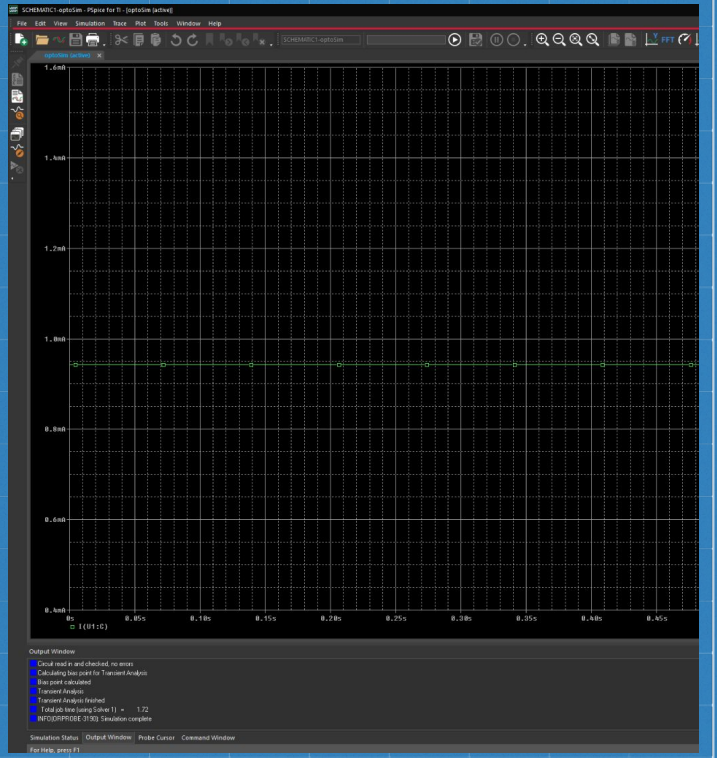
- Given that the PCB works as is, there is technically no need for any changes
- However, given that we've already come so far, I strongly suggest increasing the R10 and R8 resistors to 24kΩ each, giving an equivalent 12kΩ resistor
  - This will result in a much safer margin of error for V_{GS} of the Q4 NMOS
- Minimal change that requires little effort, so I don't believe there is a reason not to do this



Simulation of Proposed Changes



Q4 NMOS Gate-Source Voltage, not including diode voltage drop



Current I_C Through 4N35 Optocoupler

Discussion

- V_{GS} for the Q4 NMOS will be at most 0.7V when the Q2 NMOS turns on
  - Provides a significant margin of error for the 3V threshold voltage of the MOSFETs on the PCB, and will ensure that the PCB works properly every time it is needed