## Revision History

DATE	REV	
25/08/18	0.1	The first edition of board

PORTO
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文件: cover.kicad\_sch

文件: device.kicad\_sch

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文件: port0.kicad\_sch

文件: port0.kicad\_sch

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文件: port1.kicad\_sch

文件: port1.kicad\_sch

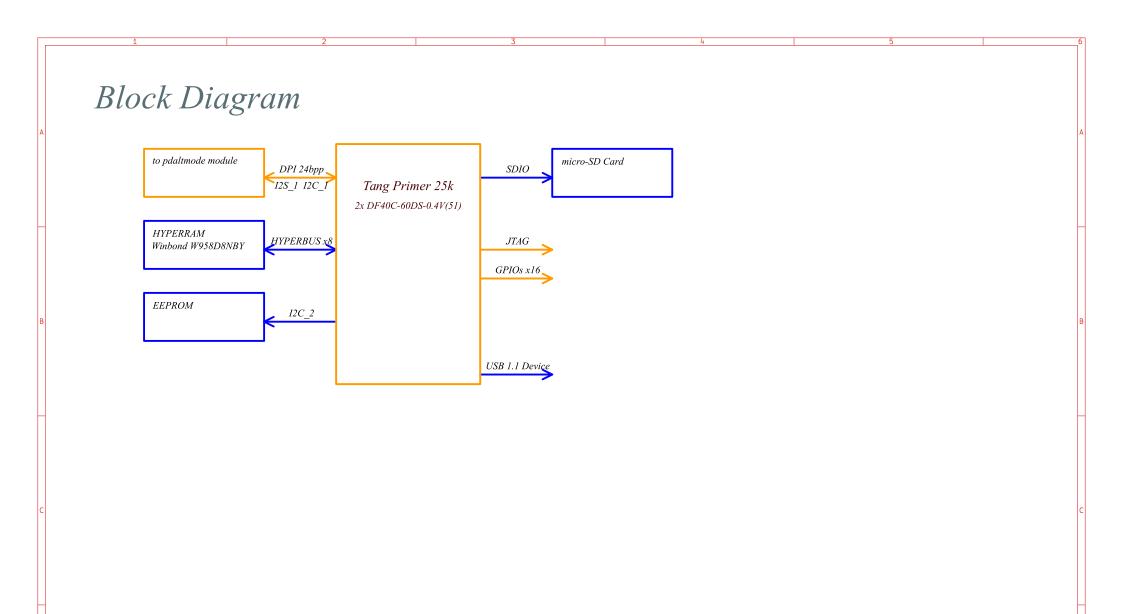
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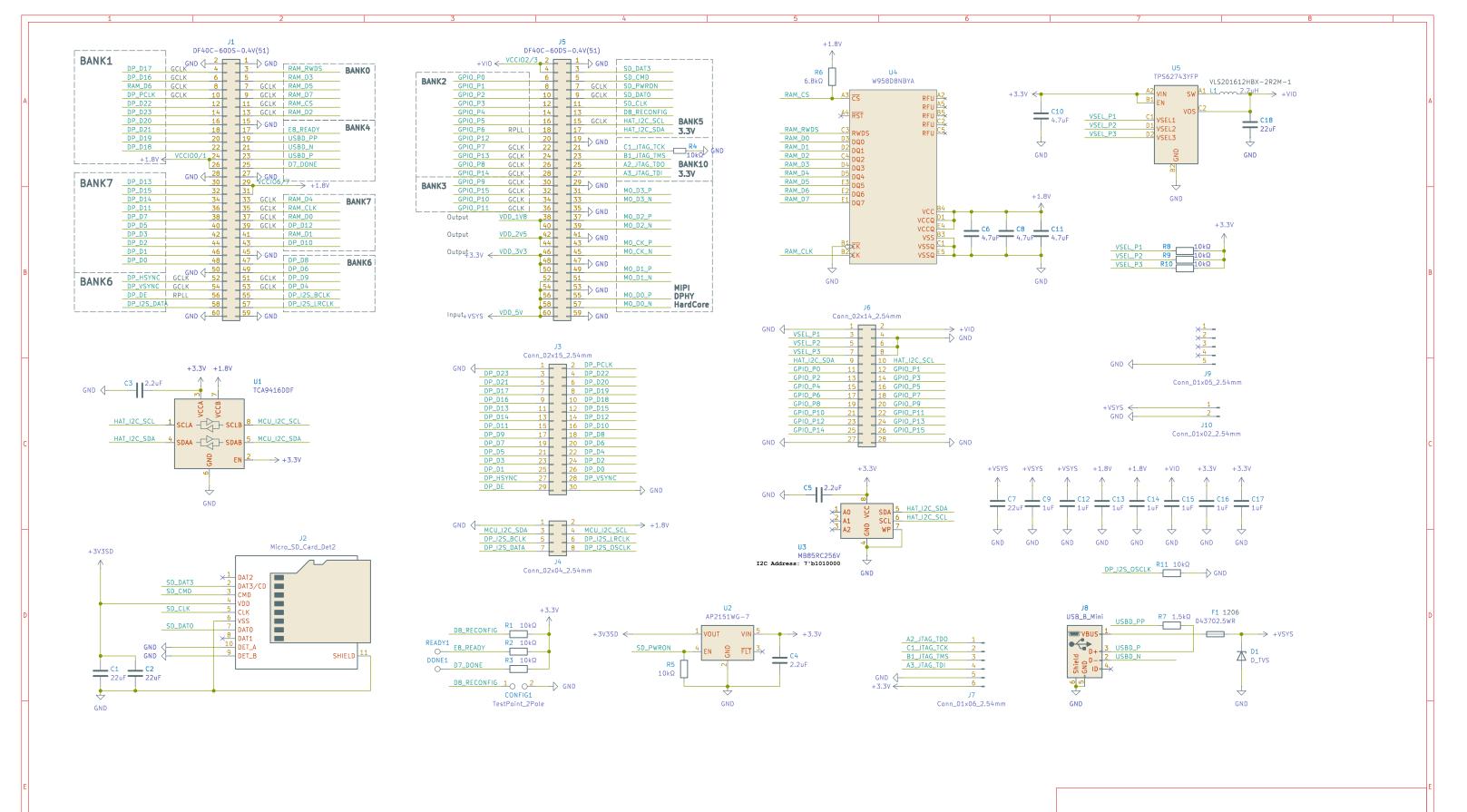
## CUBE FPGA Dev Kit

Schematic Document

2025-08-18

**REV:** 0.1





IO	PIN
DP_D0	L11_IOT11B
DP_D1	K11_IOT11A
DP_D2	K10_IOT15B
DP_D3	L10_IOT15A
DP_D4	C10_IOL5B
DP_D5	L8_IOT19B
DP_D6	D10_IOL9B
DP_D7	L7_IOT19A
DP_D8	D11_IOL9A
DP_D9	C11_IOL5A
DP_D10	G10_IOT7B
DP_D11	J7_IOT21B
DP_D12	H10_IOT3B
DP_D13	L6_IOT23A
DP_D14	K7_IOT21A

IO	PIN
DP_D15	K6_IOT23B
DP_D16	J5_IOT61B
DP_D17	H5_IOT61A
DP_D18	G5_IOT72B
DP_D19	F5_IOT72A
DP_D20	G7_IOT68A
DP_D21	G8_IOT68B
DP_D22	H8_IOT66A
DP_D23	H7_IOT66B
DP_I2S_LRCLK	B10_IOL12B
DP_I2S_BCLK	B11_IOL12A
DP_I2S_DATA	A10_IOL14B
USBFS_PP	B3_IOB56A
USBFS_N	C3_IOB56B
USBFS_P	E3_IOB60A

IO	PIN
RAM_D0	H11_IOT3A
RAM_D1	G11_IOT7A
RAM_D2	F6_IOT58B
RAM_D3	K9_IOT31B
RAM_D4	J11_IOT1A
RAM_D5	J8_IOT56A
RAM_D6	L5_IOT63A
RAM_D7	K8_IOT56B
RAM_RWDS	L9_IOT31A
RAM_CLK	J10_IOT1B
RAM_CS	F7_IOT58A
SD_DAT3	B2_IOB4A
SD_CMD	C2_IOB4B
SD_DAT0	F1_IOB26B
SD_CLK	A1_IOB24A

Sheet: /PORTO/ File: port0.kicad_sch			
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KiCad E.D.A. 9.0.2		ld: 5/6	

IO PIN L2\_IOR18A GP\_D0 GP\_D1 L1\_IOR18B K1\_IOR20A GP\_D2 K2\_IOR20B GP\_D3 J4\_IOR22A GP\_D4 K4\_IOR22B GP\_D5 G2\_IOR24A GP\_D6 GP\_D7 L4\_IOR31A J1\_IOR33A GP\_D8 GP\_D9 G4\_IOB89A H1\_IOB91A GP\_D10 H2\_IOB91B GP\_D11 GP\_D12 G1\_IOR24B GP\_D13 L3\_IOR31B GP\_D14 J2\_IOR33B

PIN
H4_IOB89B
F2_IOB26A
E1_IOB12B
D1_IOB14B

IO	PIN

Sheet: /PORT1/			
File: port1.kicad_sch			
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