Dual GigaEthernet HAT

Schematic Document

2025-12-08

REV: 0.1

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Title:

Size: A4 | Date: | **Rev:**
KiCad E.D.A. 9.0.2 | Id: 1/7

Revision History

DATE	REV	
25/12/08	0.1	The first edition

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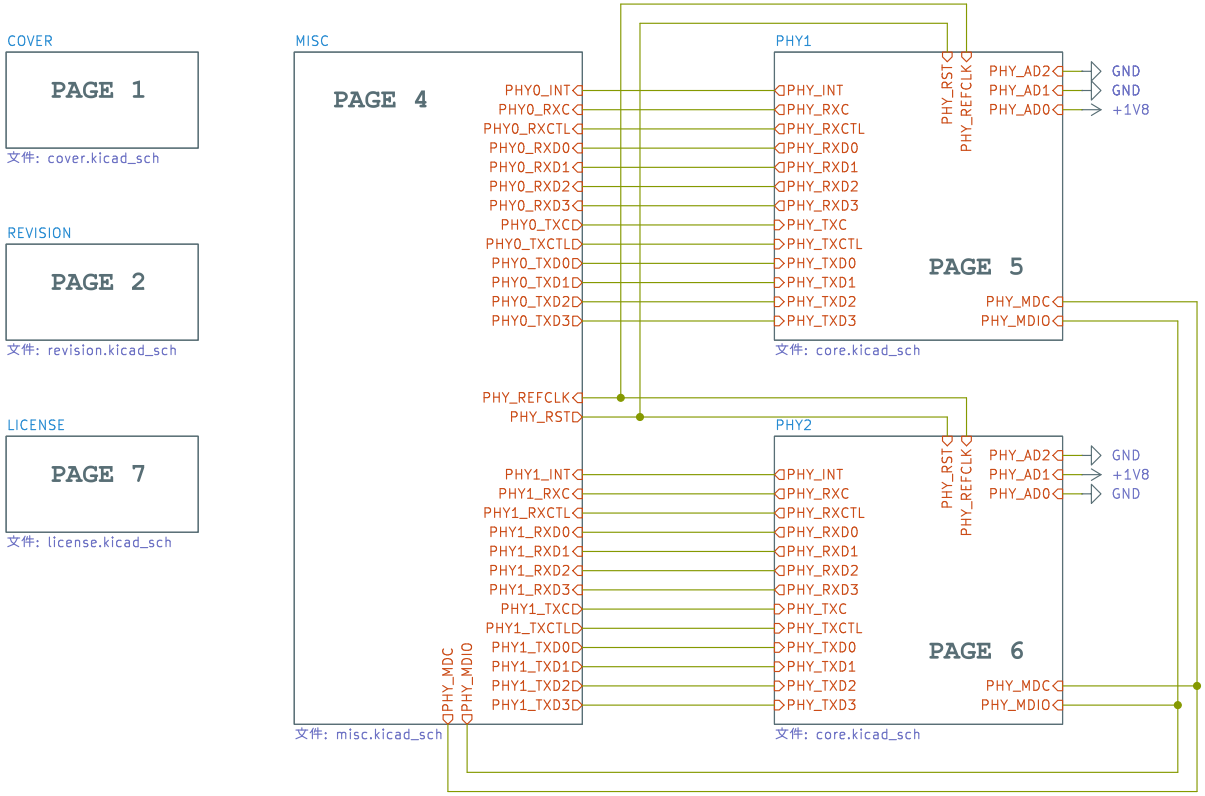
KiCad E.D.A. 9.0.2 | Id: 2/7



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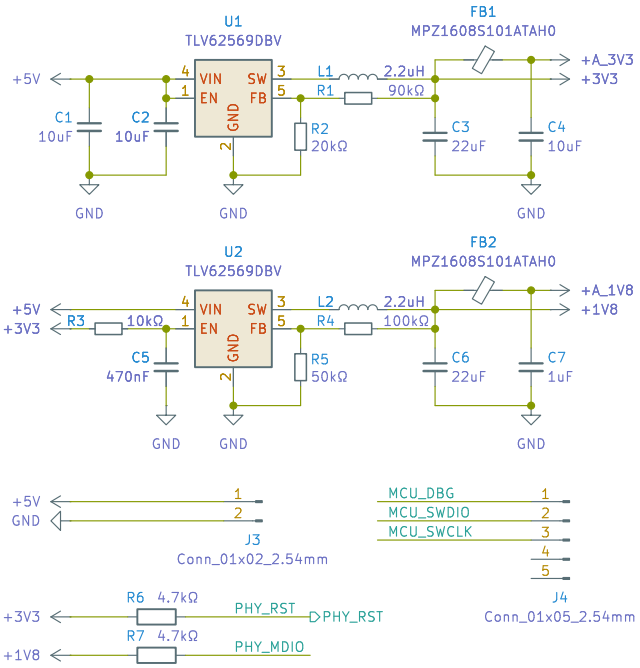

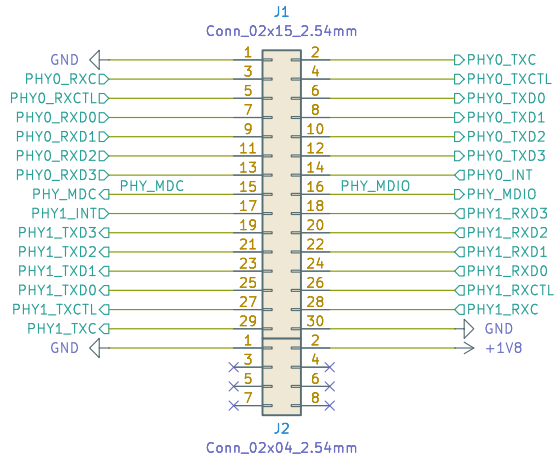

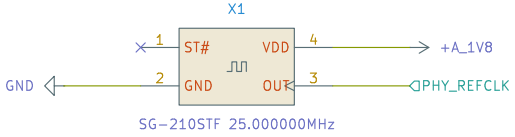

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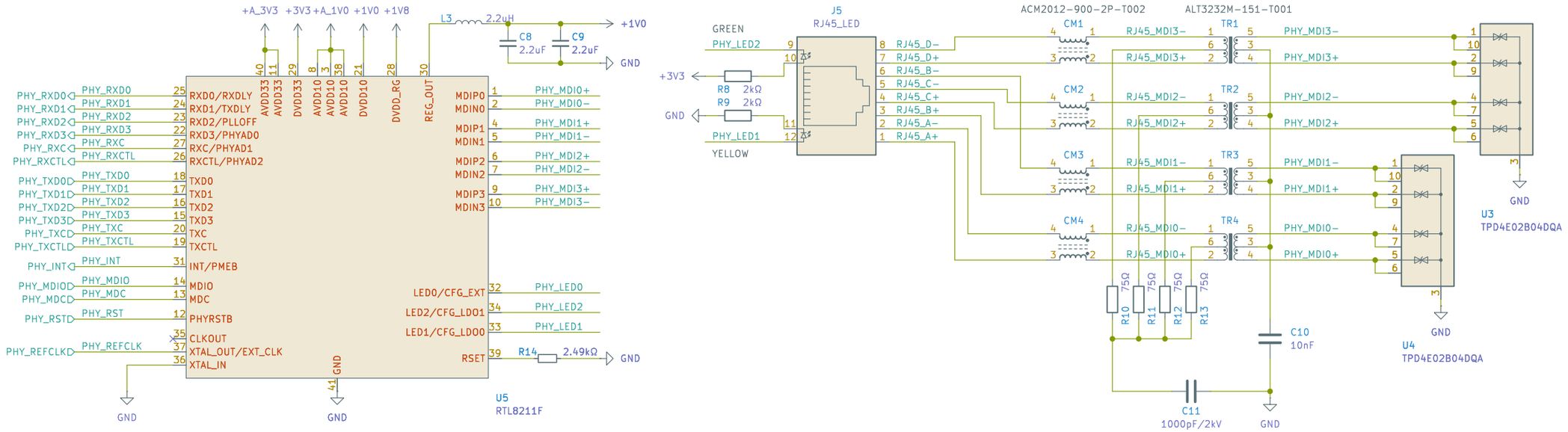
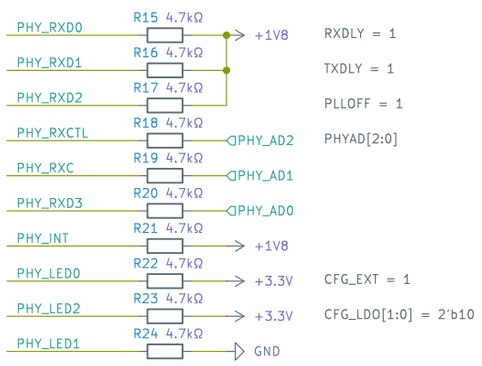


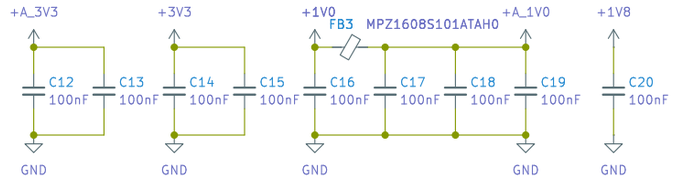
Table 10. CONFIG Pins vs. Configuration Register

CONFIG Pin	Configuration
RXD3	PHYAD[0]
RXC	PHYAD[1]
RXCTL	PHYAD[2]
RXD2	PLLOFF
RXD1	TXDLY
RXD0	RXDLY
LED0	CFG_EXT
LED1	CFG_LDO[0]
LED2	CFG_LDO[1]

Table 11. Configuration Register Definitions

Configuration	Description
PHYAD[2:0]	PHY Address. PHYAD sets the PHY address for the device. The RTL8211F(I)/RTL8211FD(I) supports PHY addresses from 0x01 to 0x07. *Note 1: An MDIO command with PHY address=0 is a broadcast from the MAC; each PHY device should respond. This function can be disabled by setting Page 0xa43, Reg24, bit[13]=0 (See section 8.5.16, page 41).* *Note 2: The RTL8211F(I)/RTL8211FD(I) with PHYAD[2:0]=000 can automatically remember the first non-zero PHY address. This function can be enabled by setting Page 0xa43, Reg24, bit[6]=1 (See section 8.5.16, page 41).*
PLLOFF	ALDPS Mode PLL Off Configuration. 1: Stop PLL when entering ALDPS mode (via 4.7k ohm to DVDD_RG) 0: PLL continue toggling when entering ALDPS mode (via 4.7k-ohm to GND)
TXDLY	RGMII Transmit Clock Timing Control. 1: Add 2ns delay to TXC for TXD latching (via 4.7k ohm to DVDD_RG) 0: No delay (via 4.7k ohm to GND)
RXDLY	RGMII Receive Clock Timing Control. 1: Add 2ns delay to RXC for RXD latching (via 4.7k ohm to DVDD_RG) 0: No delay (via 4.7k ohm to GND)
CFG_EXT	RGMII I/O Pad External Power Source Mode Configuration. 1: Use the external power source for the RGMII I/O pad (via 4.7k-ohm to 3.3V) 0: Use the integrated LDO to transform the desired voltage for the RGMII I/O pad (via 4.7k-ohm to GND)
CFG_LDO[1:0]	LDO Output Voltage Selection for the RGMII I/O pad. External Power Source Voltage Selection for the RGMII I/O pad. When pulling down CFG_EXT pin, CFG_LDO[1:0] represent LDO output voltage setting for the RGMII I/O pad; (via 4.7k-ohm to GND) 00: Reserved. 01: 2.5V 10: 1.8V 11: 1.5V When pulling up CFG_EXT pin, CFG_LDO[1:0] stand for external power voltage selection for the RGMII I/O pad; (via 4.7k-ohm to 3.3V) 00: 3.3V 01: 2.5V 10: 1.8V 11: 1.5V





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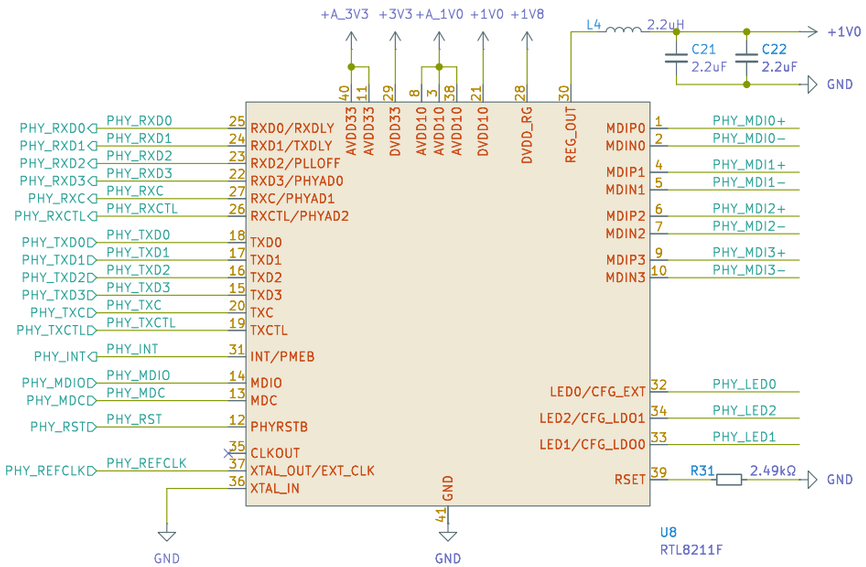
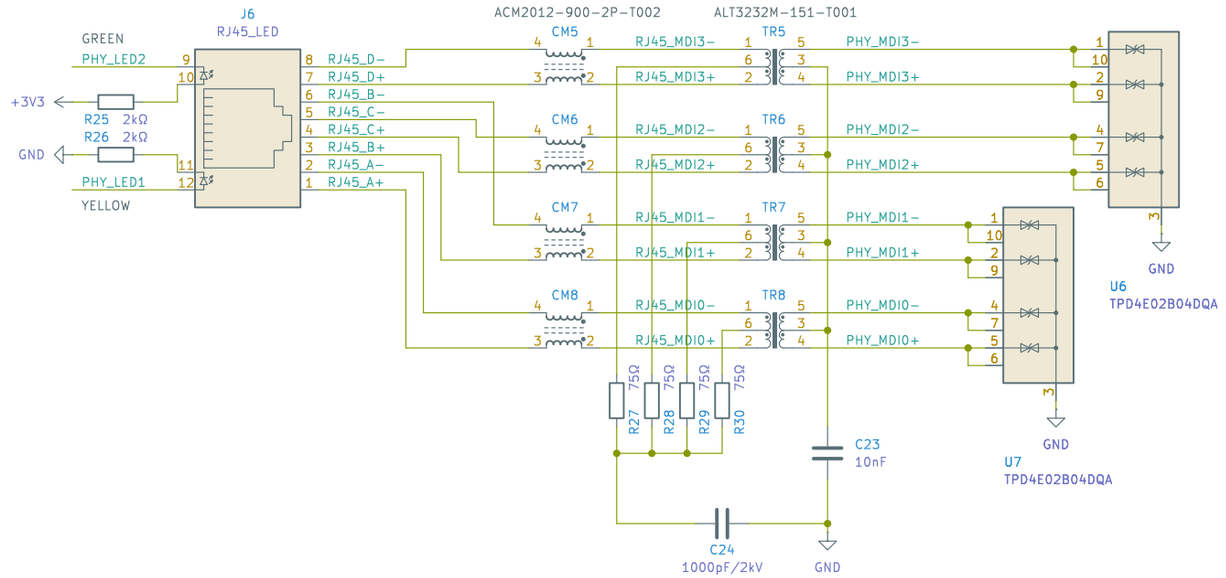
KiCad E.D.A. 9.0.2	Id: 5/7





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PLLOFF	ALDPS Mode PLL Off Configuration. 1: Stop PLL when entering ALDPS mode (via 4.7k ohm to DVDD_RG) 0: PLL continue toggling when entering ALDPS mode (via 4.7k-ohm to GND)
TXDLY	RGMII Transmit Clock Timing Control. 1: Add 2ns delay to TXC for TXD latching (via 4.7k ohm to DVDD_RG) 0: No delay (via 4.7k ohm to GND)
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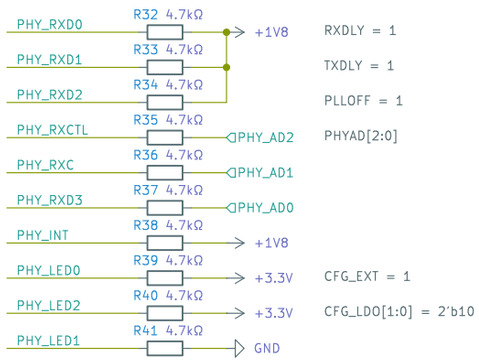

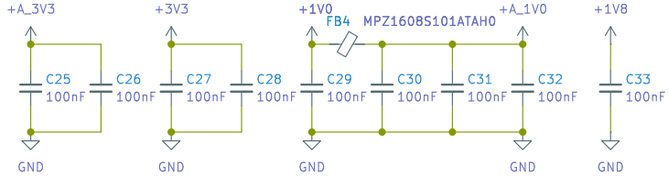

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