Type-C DP Alt-mode EVB

Schematic Document

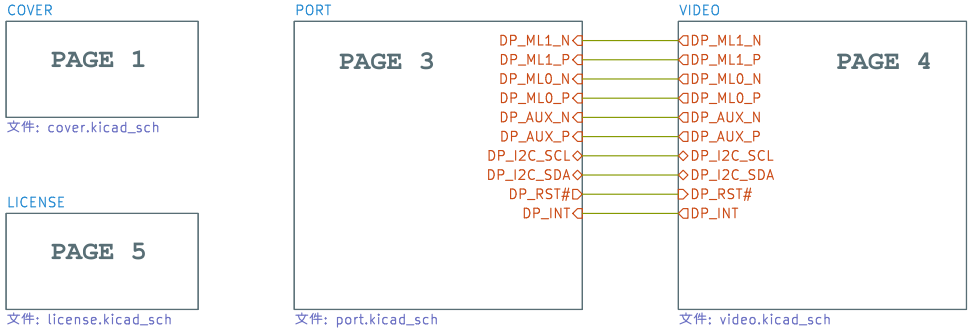
2025-02-20

REV: 0.1

Sheet: /COVER/		
File: cover.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 1/5

Type-C DP Alt-mode EVB

DATE	REV	
25/02/20	0.1	The first edition of EVB



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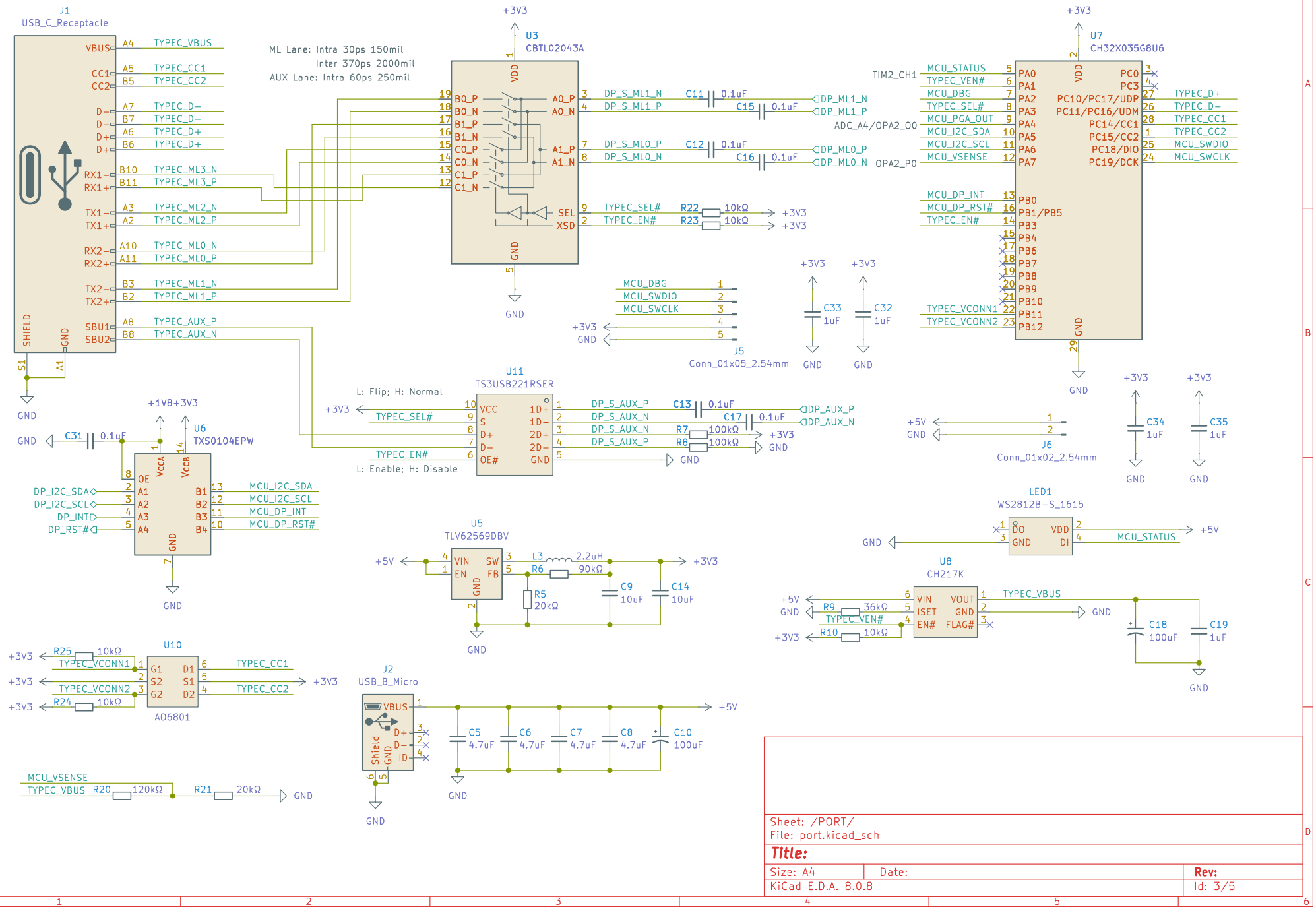
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 2/5



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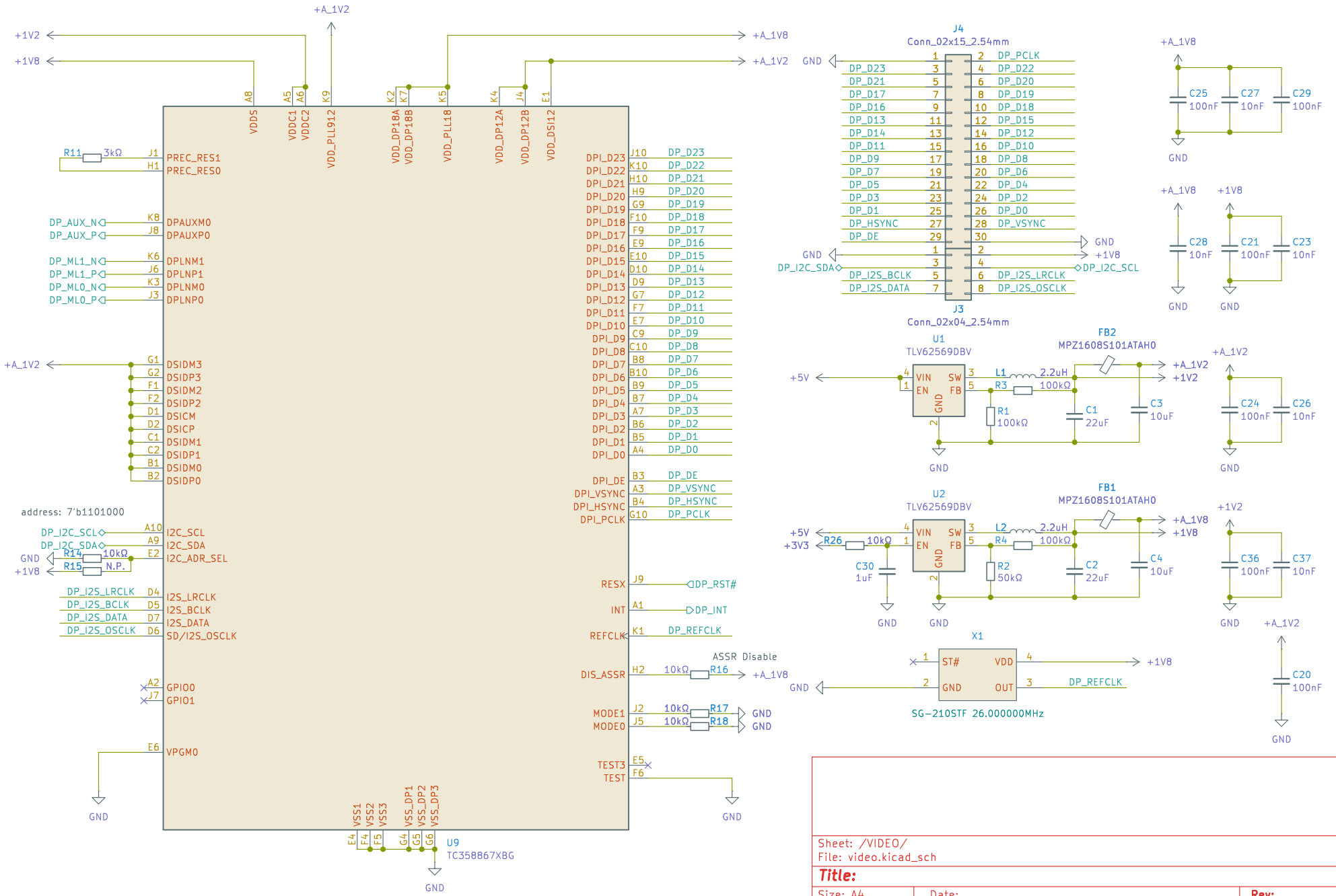
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 3/5


+A_1V2
+1V2
+1V8
+A_1V8
+A_1V2
VDDS
VDDC1
VDDC2
VDD_PLL912
VDD_DP18A
VDD_DP18B
VDD_PLL18
VDD_DP12A
VDD_DP12B
VDD_DSI12
R11 3kΩ
PREC_RES1
PREC_RES0
DP_AUX_N
DP_AUX_P
DPAUXM0
DPAUXP0
DP_ML1_N
DP_ML1_P
DP_ML0_N
DP_ML0_P
DPLNM1
DPLNP1
DPLNM0
DPLNP0
DSIDM3
DSIDP3
DSIDM2
DSIDP2
DSICM
DSICP
DSIDM1
DSIDP1
DSIDM0
DSIDP0
address: 7'b1101000
DP_I2C_SCL
DP_I2C_SDA
I2C_SCL
I2C_SDA
I2C_ADR_SEL
R14 10kΩ
R15 N.P.
DP_I2S_LRCLK
DP_I2S_BCLK
DP_I2S_DATA
DP_I2S_OSCLK
I2S_LRCLK
I2S_BCLK
I2S_DATA
SD/I2S_OSCLK
GPIO0
GPIO1
VPGM0
DPI_D23
DPI_D22
DPI_D21
DPI_D20
DPI_D19
DPI_D18
DPI_D17
DPI_D16
DPI_D15
DPI_D14
DPI_D13
DPI_D12
DPI_D11
DPI_D10
DPI_D9
DPI_D8
DPI_D7
DPI_D6
DPI_D5
DPI_D4
DPI_D3
DPI_D2
DPI_D1
DPI_D0
DPI_DE
DPI_VSYNC
DPI_HSYNC
DPI_PCLK
RESX
DP_RST#
INT
DP_INT
REFCLK
DP_REFCLK
ASSR Disable
DIS_ASSR
10kΩ R16
MODE1
MODE0
10kΩ R17
10kΩ R18
TEST3
TEST
VSS1
VSS2
VSS3
VSS_DP1
VSS_DP2
VSS_DP3
U9
TC358867XBG
GND
J4
Conn_02x15_2.54mm
DP_PCLK
DP_D22
DP_D20
DP_D19
DP_D18
DP_D15
DP_D12
DP_D10
DP_D8
DP_D6
DP_D4
DP_D2
DP_D0
DP_VSYNC
DP_I2C_SCL
DP_I2S_LRCLK
DP_I2S_OSCLK
J3
Conn_02x04_2.54mm
C25 100nF
C27 10nF
C29 100nF
C28 10nF
C21 100nF
C23 10nF
U1
TLV62569DBV
VIN
SW
EN
FB
GND
L1 2.2uH
R3 100kΩ
R1 100kΩ
C1 22uF
C3 10uF
FB2
MPZ1608S101ATAH0
C24 100nF
C26 10nF
U2
R26 10kΩ
C30 1uF
L2 2.2uH
R4 100kΩ
R2 50kΩ
C2 22uF
C4 10uF
FB1
C36 100nF
C37 10nF
X1
ST#
VDD
OUT
SG-210STF 26.000000MHz
C20 100nF
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Title:
Size: A4
Date:
Rev:
KiCad E.D.A. 8.0.8
Id: 4/5

Sheet: /LICENSE/
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Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.8		Id: 5/5