

DSI 2(to) Display Port Converter

TC358867XBG

Functional Specification

Revision 1.43

2019-04

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

NOTICE OF DISCLAIMER

The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled by any of the authors or developers of this material or MIPI. The material contained herein is provided on an "AS IS" basis and to the maximum extent permitted by applicable law, this material is provided AS IS AND WITH ALL FAULTS, and the authors and developers of this material and MIPI hereby disclaim all other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of negligence.

All materials contained herein are protected by copyright laws, and may not be reproduced, republished, distributed, transmitted, displayed, broadcast or otherwise exploited in any manner without the express prior written permission of MIPI Alliance. MIPI, MIPI Alliance and the dotted rainbow arch and all related trademarks, tradenames, and other intellectual property are the exclusive property of MIPI Alliance and cannot be used without its express prior written permission.

ALSO, THERE IS NO WARRANTY OF CONDITION OF TITLE, QUIET ENJOYMENT, QUIET POSSESSION, CORRESPONDENCE TO DESCRIPTION OR NON-INFRINGEMENT WITH REGARD TO THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT. IN NO EVENT WILL ANY AUTHOR OR DEVELOPER OF THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT OR MIPI BE LIABLE TO ANY OTHER PARTY FOR THE COST OF PROCURING SUBSTITUTE GOODS OR SERVICES, LOST PROFITS, LOSS OF USE, LOSS OF DATA, OR ANY INCIDENTAL, CONSEQUENTIAL, DIRECT, INDIRECT, OR SPECIAL DAMAGES WHETHER UNDER CONTRACT, TORT, WARRANTY, OR OTHERWISE, ARISING IN ANY WAY OUT OF THIS OR ANY OTHER AGREEMENT, SPECIFICATION OR DOCUMENT RELATING TO THIS MATERIAL, WHETHER OR NOT SUCH PARTY HAD ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

Without limiting the generality of this Disclaimer stated above, the user of the contents of this Document is further notified that MIPI: (a) does not evaluate, test or verify the accuracy, soundness or credibility of the contents of this Document; (b) does not monitor or enforce compliance with the contents of this Document; and (c) does not certify, test, or in any manner investigate products or services or any claims of compliance with the contents of this Document. The use or implementation of the contents of this Document may involve or require the use of intellectual property rights ("IPR") including (but not limited to) patents, patent applications, or copyrights owned by one or more parties, whether or not Members of MIPI. MIPI does not make any search or investigation for IPR, nor does MIPI require or request the disclosure of any IPR or claims of IPR as respects the contents of this Document or otherwise.

Questions pertaining to this document, or the terms or conditions of its provision, should be addressed to:

MIPI Alliance, Inc.
c/o IEEE-ISTO
445 Hoes Lane
Piscataway, NJ 08854
Attn: Board Secretary

This Notice of Disclaimer applies to all DSI input and processing paths related descriptions throughout this document.

Copyright © 2005-2010 MIPI Alliance, Inc. All rights reserved.

All rights reserved. This material is reprinted with the permission of the MIPI Alliance, Inc. No part(s) of this document may be disclosed, reproduced or used for any purpose other than as needed to support the use of the products of Toshiba Cooperation and its subsidiaries and affiliates.

Revision History

Revision	Date	Note
0.10	01/25/2018	<ul style="list-style-type: none">• Preliminary Version• Created based on TC358767AXBG Ver.1.31• Update "Overview"/"Features" description• Update Table 3-1 description• Modify typo in 4-15• Added descriptions about trademarks.
0.20	02/20/2018	<ul style="list-style-type: none">• Modified weight.• Added descriptions of the last page.
1.0	03/27/2018	<ul style="list-style-type: none">• Deleted descriptions of the last page.• Modified descriptions of the trademarks.• Modified Figure 1.1, Figure 1.2, Figure 1.3.• Corrected typos.• Modified descriptions in Features.• Officially released.
1.1	05/28/2018	<ul style="list-style-type: none">• Modified Table 2.2 and Table 2.3.• Corrected typos.
1.2	07/05/2018	<ul style="list-style-type: none">• Deleted unnecessary descriptions.• Modified register default value• Added description for test registers.• Corrected typos.
1.3	07/28/2018	<ul style="list-style-type: none">• Added Note to Table 3.1.• Adjusted frame of register table.
1.4	08/24/2018	<ul style="list-style-type: none">• Modified Table.3.1 REFCLK description.• Deleted 4.4.3.2.2, 4.4.3.2.3, 4.16.5.• Changed explanation in 4.4.1.1.1, 4.4.3, 4.16.1, 4.16.2.• Changed 0x01F0, 0x01F4, 0x0810, 0x0814, 0x0840, 0x0A04 to test registers.• Modified explanation of 0x0650.• Changed explanation of registers.• Corrected typos.• Revised the last page and added URL.
1.41	11/02/2018	<ul style="list-style-type: none">• Modified description of MIPI service mark and added service marks.• Modified Tables in section 5.
1.42	11/30/2018	<ul style="list-style-type: none">• Modified description and corrected typos.• Modified service marks.
1.43	04/23/2019	<ul style="list-style-type: none">• Added 0x07A0 register• Added explanation to section 4.4.3• Changed description of WXGA

REFERENCES

1. MIPI® DSISM, "MIPI Alliance Specification for DSI Version 1.01.00 - 21 February 2008"
2. MIPI® DPISM, "MIPI Alliance Standard for Display Pixel Interface (DPI-2) Version 2.00 – 15 September 2005"
3. MIPI® D-PHYSM, "DRAFT MIPI Alliance Specification for D-PHY Version 0.91.00 – r0.01 14-March-2008"
4. VESA® DisplayPort™ Standard (Version 1, Revision 1A January 11, 2008)
5. VESA® embedded DisplayPort™ (eDP) Standard (Version 1.1 October 23, 2009)
6. Digital Content Protection LLC, HDCP (Version 1.3 with DisplayPort™ amendment Revision 1.1, Jan. 15 2010)
7. I²C bus specification, version 2.1, January 2000, Philips Semiconductor
8. Draft CEA-861-C, A DTV Profile for Uncompressed High Speed Digital Interfaces (Doc. Number: CEA-861rCv9.pdf (PNXXX)) Date: 05/04/2005
9. DisplayPort™ PHY DFT Strategy Specification Rev 1.3

- MIPI® is a registered service mark of MIPI Alliance, Inc. DPISM, DSISM and D-PHYSM are service marks of MIPI Alliance, Inc.
- DisplayPort is trademark owned by the Video Electronics Standards Association (VESA®) in the United States and other countries.
- Other company names, product names, and service names may be trademarks of their respective companies.

Table of content

1. Overview	12
2. Features	16
3. External Pins.....	21
3.1. TC358867XBG External Pins	21
3.2. TC358867XBG Ball Mapping.....	23
4. Function of Major Blocks	24
4.1. MIPI DSI Rx	25
4.1.1. Video Streaming.....	25
4.1.2. DSI Write/Read accesses to Chip Configuration Registers	27
4.1.3. Exit/Enter chip power-down state using DSI interface	30
4.1.4. Reverse Low Power Transmission	30
4.1.5. DSI Packet Type Support	31
4.2. MIPI DPI Rx	33
4.2.1. Video Streaming.....	33
4.3. I2S Audio Rx.....	36
4.3.1. Audio Transmission & Alignment modes.....	36
4.3.2. Channel slots, Sample bit-width and bit clock	37
4.3.3. I2S Rx to DisplayPort™ Tx Interface	38
4.3.4. Audio Stream Start / Stop Procedure	39
4.4. DisplayPort™ Tx.....	40
4.4.1. Main Channel Overview	40
4.4.2. Aux Channel Overview.....	41
4.4.3. DisplayPort™ Link Establishment.....	43
4.5. Parallel Output Mode.....	46
4.6. GPIO Interface	47
4.7. I ² C Slave Interface.....	47
4.7.1. Providing Register Address over I ² C Bus	48
4.7.2. I ² C Write Access Translation	49
4.7.3. I ² C Read Access Translation	49
4.8. Interrupt Interface	50
4.8.1. Interrupt Assertion.....	50
4.8.2. Interrupt Handling.....	50
4.9. Internal Test Pattern (Color Bar) Generator	51
4.10. HDCP Support (Optional)	52
4.10.1. HDCP encryption modules (Optional).....	52
4.11. Reset	53
4.12. Boot-Strap & State of TC358867XBG chip after Reset.....	54
4.12.1. MODE[0]: Clock Source Selection.....	54
4.12.2. MODE[1]: DSI Reference Clock Source Division Selection	54
4.12.3. I ² C Slave Address Selection	54
4.12.4. Miscellaneous	54

4.13. Clocks	55
4.13.1. Updating PLL parameters	57
4.13.2. Down-spreading of Link Frequency (Spread Spectrum)	58
4.14. Power on/off Procedure	59
4.15. Register Accesses from Host.....	62
4.15.1. TC358867XBG register space accesses.....	62
4.15.2. DP Sink register space accesses	63
4.16. Video Transmission over DP link	65
4.16.1. DSI to DisplayPort™ Tx	65
4.16.2. DPI to DisplayPort™ Tx	65
4.16.3. Pixel Format Translation	66
4.16.4. Magic Square Algorithm.....	66
4.16.5. TC358867XBG transfer paths.....	67
4.17. Power Management	68
4.17.1. Power State transitions	68
5. RegFile Block (Reg).....	70
5.1. Register Map	70
5.1.1. Address Map Summary.....	70
5.1.2. Register Map	71
5.2. Register access protocol	76
5.2.1. Register Write	76
5.2.2. Register Read	76
5.3. DSI Registers	77
5.3.1. DSI PHY Layer Registers	77
5.3.2. DSI PPI Layer Registers	89
5.3.3. DSI Protocol Layer Registers.....	99
5.3.4. DSI General Registers	111
5.3.5. DSI Application Layer Registers	112
5.4. DPI Registers	114
5.4.1. DPIPXLFMT	114
5.5. Parallel Output Registers.....	115
5.5.1. POCTRL.....	115
5.6. Video Path0 Configuration Registers	116
5.6.1. Video Path0 Control (VPCTRL0)	116
5.6.2. Horizontal Timing Control0 Register 1 (HTIM01)	118
5.6.3. Horizontal Timing Control0 Register 2 (HTIM02)	119
5.6.4. Vertical Timing Control0 Register 1 (VTIM01)	120
5.6.5. Vertical Timing Control0 Register 2 (VTIM02)	121
5.6.6. Video Frame Timing Upload Enable0 (VFUEN0)	122
5.7. System register description	123
5.7.1. Chip ID and Revision Register.....	123
5.7.2. SYS BOOT Register	124
5.7.3. SYS Status Register	125
5.7.4. SYS Reset_Enable Register.....	126

5.7.5. SYS Control Register	127
5.7.6. DisplayPort™ Clock Registers	128
5.8. I ² C Registers	134
5.8.1. I ² C Timing Control and Enable Register	134
5.9. GPIO Registers	135
5.9.1. GPIO Mode Register	135
5.9.2. GPIO Control Register	136
5.9.3. GPIO Output Register	137
5.9.4. GPIO Input Register	138
5.10. Interrupt Registers	139
5.10.1. INTCTL_G Register	139
5.10.2. INTSTS_G Register	140
5.10.3. INT_GP0_LCNT Register	141
5.10.4. INT_GP1_LCNT Register	142
5.11. DP – DisplayPort™ Registers	143
5.11.1. DisplayPort0 Control Registers	143
5.11.2. DisplayPort0 Main Channel Registers	145
5.11.3. DisplayPort0 AUX Channel Registers	153
5.11.4. DisplayPort0 Link Training Control & Status Registers	165
5.11.5. DisplayPort™ Audio Registers	176
5.11.6. DisplayPort™ PHY Registers	182
5.12. I2S Registers	185
5.12.1. I2SCfg	185
5.12.2. I2SCH0Stat0	186
5.12.3. I2SCH0Stat1	186
5.12.4. I2SCH0Stat2	187
5.12.5. I2SCH0Stat3	187
5.12.6. I2SCH0Stat4	188
5.12.7. I2SCH0Stat5	188
5.12.8. I2SCH1Stat0	189
5.12.9. I2SCH1Stat1	189
5.12.10. I2SCH1Stat2	190
5.12.11. I2SCH1Stat3	190
5.12.12. I2SCH1Stat4	191
5.12.13. I2SCH1Stat5	191
5.13. DP1 Source Control Register	192
5.13.1. DP1_SrcCtrl Register	192
5.14. PLL Registers	194
5.14.1. DP0_PLLCTRL Register	194
5.14.2. PXL_PLLCTRL Register	195
5.14.3. PXL_PLLPARAM Register	196
5.14.4. SYS_PLLPARAM Register	198
5.15. HDCP Block Registers (Optional)	199
5.16. Debug Registers	199

5.16.1. Test control register (TestCtl)	199
5.16.2. PLL_DBG Debug Register.....	200
6. Package.....	201
7. Electrical Characteristics	202
7.1. Absolute Maximum Ratings	202
7.2. Operating Condition.....	202
7.3. DC Electrical Specification.....	203
7.4. Power Consumption (Typical value based on estimation).....	203
8. Timing Definitions	204
8.1. MIPI DSI Timings.....	204
8.1.1. LP Transmitter DC Specifications.....	204
8.1.2. HS Receiver DC Specifications	204
8.1.3. LP Receiver DC Specifications	204
8.2. DPI Interface Timings	205
8.3. Parallel Output Interface Timings.....	206
8.4. I2S Audio Interface Timings	207
8.5. DisplayPort™ Timings	208
8.6. I ² C Timings	209
RESTRICTIONS ON PRODUCT USE.....	210

List of Figures

Figure 1.1 System Overview with TC358867XBG in MODE_S21 Configuration	14
Figure 1.2 System Overview with TC358867XBG in MODE_P21 Configuration	15
Figure 1.3 System Overview with TC358867XBG in MODE_S2P Configuration.....	15
Figure 3.1 TC358867XBG 80-Ball Layout.....	23
Figure 4.1 Block Diagram of TC358867XBG	24
Figure 4.2 DSI Long Generic Write Packet.....	28
Figure 4.3 DSI Generic Short Read Request Packet	29
Figure 4.4 DSI Generic Long Read Response packet	29
Figure 4.5 Control Flow of Reverse_link Transactions.....	30
Figure 4.6 DPI Timing parameters.....	34
Figure 4.7 DPI Interface color coding	35
Figure 4.8 I2S Interface timing.....	37
Figure 4.9 AUX transaction initiators to DP Tx.....	42
Figure 4.10 DisplayPort™ initialization – a high level overview	44
Figure 4.11 DPI Timing parameters.....	46
Figure 4.12 Register Write Transfer over I ² C Bus	48
Figure 4.13 Random Register Read Transfer over I ² C Bus	48
Figure 4.14 Continuous Register Read Transfer over I ² C Bus.....	48
Figure 4.15 I ² C Write Transfers Translated to Register Write Accesses	49
Figure 4.16 I ² C Read Transfers to Register Read Accesses	49
Figure 4.17 Reset System	53
Figure 4.18 Clock Mode Selection and Clock Sources	57
Figure 4.19 Timing diagram for updating PLL parameters	58
Figure 4.20 Power On Sequence	60
Figure 4.21 Power Off Sequence	61
Figure 4.22 Magic Square Algorithm Effect	67
Figure 4.23 Power State Transition Diagram	68
Figure 5.1 Register Write Access from I ² C Slave.....	76
Figure 5.2 Register Read Access from I ² C Slave.....	76
Figure 6.1 80 ball TC358867XBG package	201
Figure 8.1 DPI Interface timing	205
Figure 8.2 Parallel output Interface timing (shown for inverted clock polarity)	206
Figure 8.3 I2S timing	207
Figure 8.4 I ² C timing	209

List of Tables

Table 2.1	TC358867XBG operational modes summary with panel size support information	19
Table 2.2	Panel Size v/s Data link required by TC358867XBG in DSI input case	20
Table 2.3	Panel Size v/s Data link required by TC358867XBG in DPI input case	20
Table 3.1	TC358867XBG Functional Signal List for 80-ball Package	21
Table 4.1	DSI Packets pertaining to Video Transmission	26
Table 4.2	Forward-Link DSI Packets Support	31
Table 4.3	Reverse-Link DSI Packets Support	32
Table 4.4	TC358867XBG clocks relationships in different Modes	56
Table 4.5	Power On Sequence Timing	60
Table 4.6	Power Off Sequence Timing	61
Table 4.7	Pixel Translation Paths	66
Table 4.8	TC358867XBG Video Transfer Paths	67
Table 4.9	Component Power State summary	69
Table 5.1	Register Map	70
Table 5.2	Register Map	71
Table 5.3	D0W_DPHYCONTTX Register	77
Table 5.4	CLW_DPHYCONTRX Register	78
Table 5.5	D0W_DPHYCONTRX Register	79
Table 5.6	D1W_DPHYCONTRX Register	80
Table 5.7	D2W_DPHYCONTRX Register	81
Table 5.8	D3W_DPHYCONTRX Register	82
Table 5.9	COM_DPHYCONTRX Register	83
Table 5.10	CLW_CNTRL Register	84
Table 5.11	D0W_CNTRL Register	85
Table 5.12	D1W_CNTRL Register	86
Table 5.13	D2W_CNTRL Register	87
Table 5.14	D3W_CNTRL Register	88
Table 5.15	PPI_STARTPPI Register	89
Table 5.16	PPI_BUSYPPI Register	89
Table 5.17	PPI_LINEINITCNT Register	90
Table 5.18	PPI_LPTXTIMECNT Register	91
Table 5.19	PPI_LANEENABLE Register	92
Table 5.20	PPI_TX_RX_TA Register	93
Table 5.21	PPI_D0S_CLRSIPOCOUNT Register	94
Table 5.22	PPI_D1S_CLRSIPOCOUNT Register	95
Table 5.23	PPI_D2S_CLRSIPOCOUNT Register	96
Table 5.24	PPI_D3S_CLRSIPOCOUNT Register	97
Table 5.25	DSI_STARTDSI Register	99
Table 5.26	DSI_BUSYDSI Register	100
Table 5.27	DSI_LANEENABLE Register	101
Table 5.28	DSI_LANESTATUS0 Register	102
Table 5.29	DSI_LANESTATUS1 Register	103
Table 5.30	DSI_INTSTATUS Register	104
Table 5.31	DSI_INTMASK Register	106
Table 5.32	DSI_INTCLR Register	108
Table 5.33	DSI_LPTXT0 Register	110
Table 5.34	DSIERRCNT Register	111
Table 5.35	Application Layer Control Register	112
Table 5.36	DSI Read Packet Length Register	113
Table 5.37	DPIPXLFMT Register	114

Table 5.38	POCTRL Register	115
Table 5.39	Video Path0 Control (VPCTRL0) Register	116
Table 5.40	Horizontal Timing Control0 Register 1 (HTIM01) Register	118
Table 5.41	Horizontal Timing Control0 Register 2 (HTIM02) Register	119
Table 5.42	Vertical Timing Control0 Register 1 (VTIM01) Register	120
Table 5.43	Vertical Timing Control0 Register 2 (VTIM02) Register	121
Table 5.44	Video Frame Timing Upload Enable0 (VFUEN0) Register	122
Table 5.45	Chip ID and Revision ID Register	123
Table 5.46	SYS Boot Register	124
Table 5.47	SYS Status Register	125
Table 5.48	SYS Reset Register	126
Table 5.49	SYS Control Register	127
Table 5.50	DP0_VidMNGen0 Register	128
Table 5.51	DP0_VidMNGen1 Register	129
Table 5.52	DP0_VMNGenStatus Register	130
Table 5.53	DP0_AudMNGen0 Register	131
Table 5.54	DP0_AudMNGen1 Register	132
Table 5.55	DP0_AMNGenStatus Register	133
Table 5.56	I ² C Timing Control and Enable Register	134
Table 5.57	GPIO Control Register	135
Table 5.58	GPIO Control Register	136
Table 5.59	GPIO Output Register	137
Table 5.60	GPIO Input Register	138
Table 5.61	INTCTL_G Control Register	139
Table 5.62	INTSTS_G Control Register	140
Table 5.63	INT GPIO0 Low Count Register	141
Table 5.64	INT GPIO1 Low Count Register	142
Table 5.65	DP0Ctl Register	143
Table 5.66	Effect of dp_en and vid_en controls on DP0 link Register	144
Table 5.67	DP0_SecSample Register	145
Table 5.68	DP0_VidSyncDelay Register	146
Table 5.69	DP0_TotalVal Register	147
Table 5.70	DP0_StartVal Register	148
Table 5.71	DP0_ActiveVal Register	149
Table 5.72	DP0_SyncVal Register	150
Table 5.73	DP0_Misc Register	151
Table 5.74	DP0_AuxCfg0 Register	153
Table 5.75	DP0_AuxCfg1 Register	154
Table 5.76	DP0_AuxAddr Register	155
Table 5.77	DP0_AuxWData0 Register	156
Table 5.78	DP0_AuxWData1 Register	157
Table 5.79	DP0_AuxWData2 Register	157
Table 5.80	DP0_AuxWData3 Register	158
Table 5.81	DP0_AuxRData0 Register	159
Table 5.82	DP0_AuxRData1 Register	160
Table 5.83	DP0_AuxRData2 Register	160
Table 5.84	DP0_AuxRData3 Register	161
Table 5.85	DP0_AuxStatus Register	162
Table 5.86	DP0_AuxI2CAdr Register	164
Table 5.87	DP0_SrcCtrl Register	165
Table 5.88	DP0_LTStat Register	167
Table 5.89	DP0_SnkLTChgReq Register	169
Table 5.90	DP0_SnkLTLoopCtrl Register	170

Table 5.91 DP0_SnkLTCtrl Register	171
Table 5.92 DP0_TPatDat0 Register	172
Table 5.93 DP0_TPatDat1 Register	173
Table 5.94 DP0_TPatDat2 Register	174
Table 5.95 DP0_TPatDat3 Register	175
Table 5.96 AudCfg0 Register	176
Table 5.97 AudCfg1 Register	177
Table 5.98 AudIFData0 Register	178
Table 5.99 AudIFData1 Register	179
Table 5.100 AudIFData2 Register	179
Table 5.101 AudIFData3 Register	180
Table 5.102 AudIFData4 Register	180
Table 5.103 AudIFData5 Register	181
Table 5.104 AudIFData6 Register	181
Table 5.105 DP_PHY_Ctrl Register	182
Table 5.106 DP0_AUX_PHY_Ctrl Register	184
Table 5.107 I2SCfg Register	185
Table 5.108 I2SCH0STAT0 Register	186
Table 5.109 I2SCH0STAT1 Register	186
Table 5.110 I2SCH0STAT2 Register	187
Table 5.111 I2SCH0STAT3 Register	187
Table 5.112 I2SCH0STAT4 Register	188
Table 5.113 I2SCH0STAT5 Register	188
Table 5.114 I2SCH1STAT0 Register	189
Table 5.115 I2SCH1STAT1 Register	189
Table 5.116 I2SCH1STAT2 Register	190
Table 5.117 I2SCH1STAT3 Register	190
Table 5.118 I2SCH1STAT4 Register	191
Table 5.119 I2SCH1STAT5 Register	191
Table 5.120 DP1_SrcCtrl Register	192
Table 5.121 DP0_PLLCTRL Register	194
Table 5.122 PXL_PLLCTRL Register	195
Table 5.123 PXL_PLLPARAM Register	196
Table 5.124 SYS_PLLPARAM Register	198
Table 5.125 TC358867XBG Test Control Register	199
Table 7.1 Absolute Maximum Ratings	202
Table 7.2 Operating Condition	202
Table 7.3 DC Electrical Specification	203
Table 8.1 DSI LP Transmitter DC Specifications	204
Table 8.2 DSI HS Receiver DC Specifications	204
Table 8.3 DSI LP Receiver DC Specifications	204
Table 8.4 DPI timing	205
Table 8.5 Parallel output interface timing	206
Table 8.6 I2S timing	207
Table 8.7 DisplayPort™ Main Link Transmitter (Main TX) Specifications	208
Table 8.8 I ² C Timing	209

1. Overview

The DSI / DPI to DisplayPort™ converter (TC358867XBG) is a bridge device that enables video streaming from a Host (application or baseband processor) over MIPI DSI or DPI link to drive DisplayPort™ display panels. TC358867XBG also supports audio streaming from the host via I2S interface to the Display panels. TC358867XBG provides a low power bridge solution to efficiently translate MIPI DSI or DPI transfers to DisplayPort™ transfers. As the DisplayPort™ uses fewer wires compared to other existing display panel standards, it simplifies the LCD connectivity. The effect of using TC358867XBG is to enable existing baseband devices supporting DSI or DPI streaming to connect to new panels supporting DisplayPort™ interface and also to connect to existing panels over longer distance using DisplayPort™ adaptors at far-end.

The chip can be configured through the DSI link by sending write/read register commands through DSI Generic Long Write packets. It can also be configured through the I²C Slave interface.

The DSI-RX receiver supports from 1 to 4-Lane configurations at bit rate up to 1 Gbps per lane. Host can transmit video in continuous video streaming mode. Host controls video timing by sending video frame and line sync events together with video pixel data; video data transmission can be burst or non-burst. Since the chip integrates only a small video buffer, Host still has to take care of transmitting pixel data at appropriate video line time in order to avoid buffer overflow (or underflow).

The DPI-Rx receiver supports 16, 18 or 24 bits parallel interface along with the required control signals for the Pixel clock and HSync/VSync/DE.

The TC358867XBG also supports content protection using HDCP copy protection (Optional).

The DisplayPort™ transmitter supports data throughput at 1.62 Gbps or 2.7 Gbps per lane of main link.

TC358867XBG supports three configuration modes. These modes mainly differ based on the source of input stream and output interface.

- Mode_S21: A system configuration where TC358867XBG may typically be used is shown in Figure 1.1. In this configuration, the TC358867XBG can support displays with resolution up to WUXGA (1920x1200) at 24bit, 60 fps or WUXGA (1920x1200) at 18bit, 60 fps. Video stream source is from DSI Host.
- Mode_P21: A system configuration where TC358867XBG may typically be used is shown in Figure 1.2. This is similar to the Mode_S21 except that the video stream source is from DPI Host. In this configuration, the TC358867XBG can support displays with resolution up to WUXGA (1920x1200) at 24bit, 60 fps.
- Mode_S2P: A system configuration where TC358867XBG may typically be used is shown in Figure 1.3. In this mode, DisplayPort™ output is not used and the chip rather behaves as a DSI to RGB convertor. In this system, TC358867XBG could be connected to a single display. In this configuration, the TC358867XBG can support displays with resolution up to WXGA (1280x800). Maximum output PCLK is 100 MHz. Video stream source is from DSI Host.

The chip supports power management to conserve power when its functions are not in use. Host manages the chip's power consumption modes by using ULPS messages over DSI link during DPI input mode.

The following figures show all these modes, where TC358867XBG, display panels and a Host are connected in target Reference system for mobile large display panel applications.

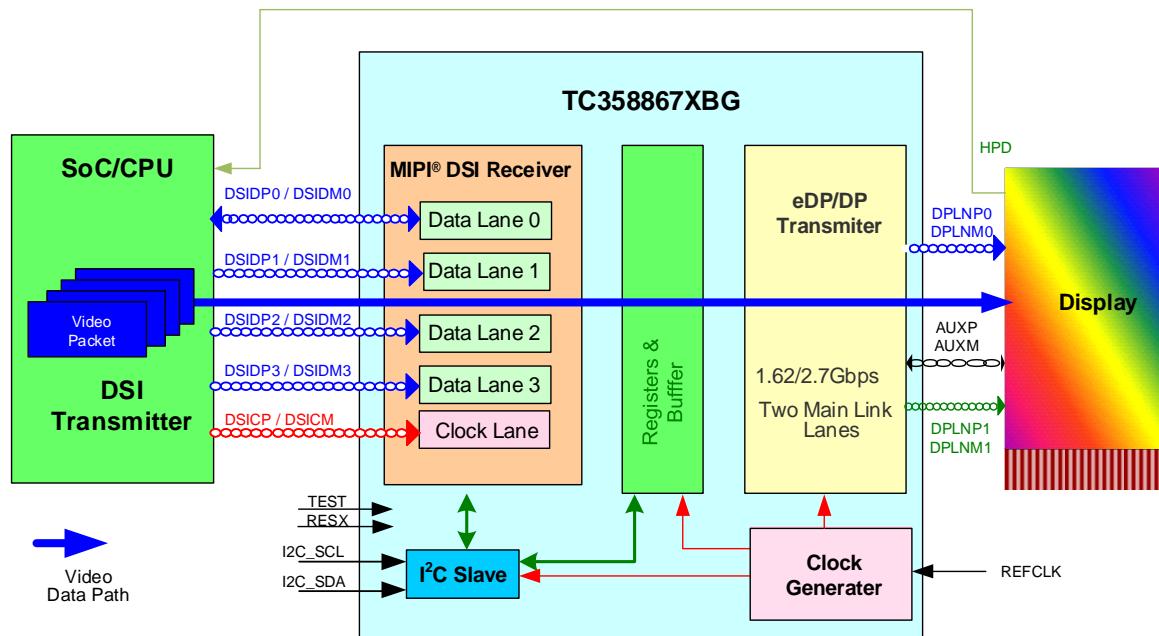


Figure 1.1 System Overview with TC358867XBG in MODE_S21 Configuration

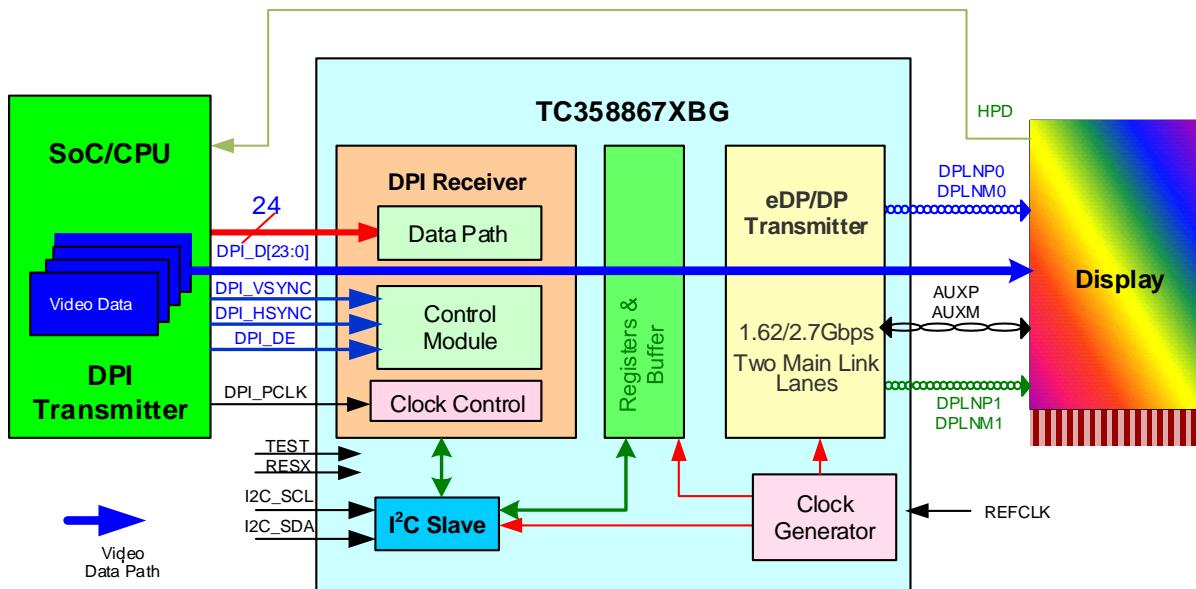


Figure 1.2 System Overview with TC358867XBG in MODE_P21 Configuration

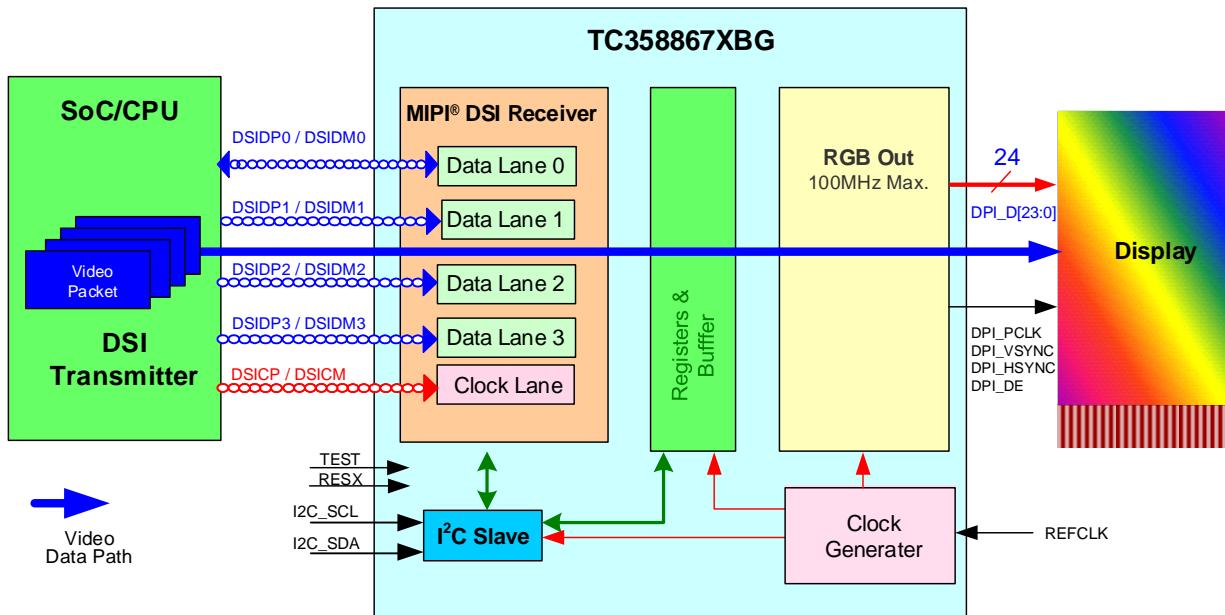


Figure 1.3 System Overview with TC358867XBG in MODE_S2P Configuration

2. Features

Below are the main features supported by TC358867XBG.

- Translates MIPI DSI/DPI Link video stream from Host to DisplayPort™ Link data to external display devices.
- The inputs are driven by a DSI Host with 4-Data Lanes, upto1 Gbps/lane or DPI Host with 16/18/24 bit interface upto154 MHz parallel clock.
- (Optional) Supports HDCP Digital Content Protection version 1.3 (DisplayPort™ amendment Rev1.1).
- Embeds audio information from the I2S port into the DisplayPort™ data stream.
- The output Interface consists of a DisplayPort™ Tx with a 2-lane Main Link and AUX-Ch.
- Register Configuration: From DSI link or I²C interface.
- Interrupt to host to inform any error status or status needing attention from Host.
- Internal test pattern (color bar) generator for DP o/p testing without any video (DSI/DPI) i/p.
- Debug/Test Port: I²C Slave
- **DSI Receiver**
 - ◊ MIPI DSI: v1.01 / MIPI D-PHY: v0.90 Compliant.
 - ◊ Up to four (4) Data Lanes with Bi-direction support on Data Lane 0.
 - ◊ Maximum speed at 1 Gbps/lane.
 - ◊ Supports Burst as well as Non-Burst Mode Video Data.
 - Video data packets are limited to one row per Hsync period.
 - ◊ Supports video stream packets for video data transmission.
 - ◊ Supports generic long packets for accessing the chip's register set.
 - ◊ Video input data formats:
 - RGB-565, RGB-666 and RGB-888.
 - New DSI V1.02 Data Type Support: 16-bit YCbCr 422
 - ◊ Interlaced video mode is not supported.
- **DPI Receiver**
 - ◊ Up to 16 / 18 / 24 bit parallel data interface.
 - ◊ Maximum speed at 154 MPs (MPixel per sec.).
 - ◊ Video input data formats: RGB-565, RGB-666 and RGB-888.
 - ◊ Only Progressive mode supported.

- **I2S Audio Interface:** Supports one I2S port for audio streaming from the host to TC358867XBG.
 - ✧ Supports slave mode (BCLK, LRCLK & over-sampling clock input from Host).
 - ✧ Supports sampling frequencies of 32, 44.1, 48, 88.2, 96, 176.4 & 192 kHz.
 - ✧ Supports up to 2 audio channels.
 - ✧ Supports 16, 18, 20 or 24bits per sample.
 - ✧ Optionally inserts IEC60958 status bits and preamble bits per channel.
- **DisplayPort™ Interface:** Supports a DisplayPort™ link from TC358867XBG to display panels.
 - ✧ High speed serial bridge chip using VESA® DisplayPort™ 1.1a Standard.
 - ✧ Supports one dual-lane DisplayPort™ port for high bandwidth applications
 - ✧ Support 1.62 or 2.7 Gbps/lane data rate with voltage swings @0.4, 0.6, 0.8 or 1.2V
 - ✧ Support of pre-emphasis levels of 0, 3.5dB and 6dB.
 - ✧ Supports Audio related Secondary Data Packets.
 - ✧ AUX channel supported at 1 Mbps.
 - ✧ HPD support through GPIO based interrupts
 - ✧ Enhanced mode supported for content protection.
 - ✧ (Optional) Support HDCP encryption Version 1.3 with DisplayPort™ amendment Revision 1.1.
 - ✧ Secure ASSR (Alternate Scrambler Seed Reset) support.
 - ✧ Stream Policy Maker is assumed handled by the Host (software/firmware).
 - Start Link training in response to HPD & read final Link training status
 - Configure DP link for actual video streaming & start video streaming
 - ✧ Link Policy maker is assumed shared between the Host and TC358867XBG chip.
 - In auto_correction = 0 mode, control link training
 - Initiate Display device capabilities read and configure TC358867XBG accordingly.
 - ✧ Video timing generation as per panel requirement.
 - ✧ SSCG with ~30 kHz modulation to reduce EMI.
 - ✧ Built in PRBS7 Generator to test DisplayPort™ Link.

- **RGB Parallel Output Interface:**
 - ✧ RGB888 output (DisplayPort™ disabled) with only DSI input supported in this mode
 - ✧ PCLK max. = 100 MHz
 - ✧ Polarity control for PCLK, VSYNC, HSYNC & DE.
- **I²C Interface:**
 - ✧ I²C slave interface for chip register set access enabled using a boot-strap option.
 - ✧ I²C compliant slave interface support for normal (100 kHz) and fast mode (400 kHz).
- **GPIO Interface:**
 - ✧ 2 bits of GPIO (shared with other digital logic).
 - ✧ Direction controllable by Host I²C accesses.
- **Clock Source:**
 - ✧ DisplayPort™ clock source is from an external clock input or clock from DSI interface (13, 26, 19.2 or 38.4 MHz) – generates all internal & output clocks to interfacing display devices.
 - ✧ Built-in PLLs generate high-speed DisplayPort™ link clock requiring no external components. These PLLs are part of the DisplayPort™ PHY.
- Clock and power management support to achieve low power states.
- **Possible modes of Operation:**
 - ✧ MODE S21: TC358867XBG uses DisplayPort™ Tx as single 2-lane DisplayPort™ link to interface to single DisplayPort™ display device. Video stream source is from MIPI DSI Host.
 - ✧ MODE P21: TC358867XBG uses DisplayPort™ Tx as single 2-lane DisplayPort™ link to interface to single DisplayPort™ display device. Video stream source is from MIPI DPI Host.
 - ✧ MODE S2P: TC358867XBG uses only Parallel output port and disables DisplayPort™ Tx to interface to single RGB display device. Video stream source is from MIPI DSI Host.
- **Power supply inputs**
 - ✧ Core and MIPI D-PHY: 1.2V \pm 0.06V
 - ✧ Digital I/O: 1.8V \pm 0.09V
 - ✧ DisplayPort™: 1.8V \pm 0.09V
 - ✧ DisplayPort™: 1.2V \pm 0.06V

- **Power Consumptions (Typical value based on estimations)**

- ◊ Power-down mode (DSI-Rx in ULPS, DP PHY & PLLs disabled, clocks stopped):
 - DSI Rx: 0.01 mW
 - DP PHY: 2.34 mW
 - PLL9: 0.01 mW
 - Core: 0.96 mW
 - Rest: 0.01 mW
- ◊ Normal operation (1920 x 1080 resolution with DSI-Rx in 4-lane @925 Mbps per lane, DP PHY in dual lane link @2.7 Gbps per lane):
 - DSI Rx: 21.79 mW
 - DP PHY: 142.70 mW
 - PLL9: 2.42 mW
 - Core: 87.64 mW
 - IOs: 1.68 mW

- **Package**

- 0.65mm ball pitch, 80 balls, 7 x 7 mm BGA package

Note: Attention about ESD. This product is weak against ESD. Please handle it carefully.

Table 2.1 TC358867XBG operational modes summary with panel size support information

Mode	Input Configuration		Register Access Method	Max Panel size example
	DSI input	DPI input		
S21	Active	X	DSI or I ² C	WUXGA 18bpp @ 60fps WUXGA 24bpp @ 60fps
P21	X	Active	I ² C	WUXGA 24bpp @ 60fps

Tables below provide an idea of different panel sizes that can be supported by using different data link lane configurations.

Table 2.2 Panel Size v/s Data link required by TC358867XBG in DSI input case

Frame Size			FPS	Pixel Clock (MHz)	RGB666				RGB888					
-	-	With OverHead			Bit Rate (Gbps)	# DSI Data lanes	# DP Main links		Bit Rate (Gbps)	# DSI Data lanes	# DP Main links			
							1.62 G	2.7 G			1.62G	2.7G		
XGA	1024x768	1184x790	60	56	1.01	2	1	1	1.34	2	2	1		
WXGA+/WSXGA	1440x900	1600x926	60	89	1.60	2	2	1	2.13	3	2	1		
SXGA+	1400x1050	1560x1080	60	89	1.82	2	2	1	2.43	3	2	2		
WSXGA+	1680x1050	1840x1080	60	119	2.15	3	2	1	2.86	3	—	2		
UXGA	1600x1200	1760x1235	60	130	2.35	3	2	2	3.13	4	—	2		
WUXGA	1920x1200	2080x1235	60	154	2.77	3	—	2	3.70	4	—	2		

Table 2.3 Panel Size v/s Data link required by TC358867XBG in DPI input case

Frame Size			FPS	Pixel Clock (MHz)	DPI Support 154 MHz PCLK	RGB666				RGB888						
-	-	With OverHead				Bit Rate (Gbps)	# DP Main links		Bit Rate (Gbps)	# DP Main links		1.62G	2.7G			
							1.62G	2.7G		1.62G	2.7G					
XGA	1024x768	1184x790	60	56	Yes	1.01	1	1	1.34	2	1	—	—			
WXGA+/WSXGA	1440x900	1600x926	60	89	Yes	1.60	2	1	2.13	2	1	—	—			
SXGA+	1400x1050	1560x1080	60	89	Yes	1.82	2	1	2.43	2	2	—	—			
WSXGA+	1680x1050	1840x1080	60	119	Yes	2.15	2	1	2.86	—	2	—	—			
UXGA	1600x1200	1760x1235	60	130	Yes	2.35	2	2	3.13	—	2	—	2			
WUXGA	1920x1200	2080x1235	60	154	Yes	2.77	—	2	3.70	—	2	—	2			

Note: These are the formats commonly used by displays. Support for other sizes is possible as long as they satisfy the maximum data rate constraints on the DSI and DisplayPort™ link interfaces.

Note: Throughout the rest of the document, “DP” is used to denote “DisplayPort™”. Both these words have been used interchangeably and refer to the VESA® DisplayPort™ specification as mentioned in the references.

3. External Pins

3.1. TC358867XBG External Pins

TC358867XBG uses 80 ball package. Following table gives the signals of TC358867XBG and their function.

Table 3.1 TC358867XBG Functional Signal List for 80-ball Package

Group	Pin Name	I/O	Type	Function	Note
System: Reset, Clock, Mode select, Test (9)	RESX	I	Sch	System Reset – active Low 0: Reset 1: Normal operation	—
	REFCLK	I	Sch	13, 26, 19.2 or 38.4 MHz 50 ps peak to peak jitter/ WC duty cycle 40 - 60%	—
	INT	O	N	Interrupt to Host – active High 0: No interrupt is generated 1: Interrupt is generated	4mA
	DISABLE_ASSR	I	N	ASSR control 0: Enable ASSR 1: Disable ASSR	—
	MODE[1:0]	I	N	Mode Selection pins MODE_0: 0: REFCLK is source of internal DP PLL 1: When REFCLK = "0", DSI clock is source of internal DP PLL. When REFCLK = "1", DPI PCLK is source of internal DP PLL. MODE_1: When MODE_0 = "1" & REFCLK = "0" this pin will be effective. 0: DSI clock/2/7 is source of internal DP PLL. 1: DSI clock/2/9 is source of internal DP PLL.	—
	TEST	I	N	Test Pin - active high 0: Normal operation 1: Test mode	—
	TEST3	O	N	Test Pin, Open	—
	VPGM0	NA	—	eFUSE programming voltage. Connect to GND	—
	DSICP	I	MIPI-PHY	MIPI-DSI Rx Clock Lane Pos.	—
DSI Rx (Note2) (10)	DSICM	I	MIPI-PHY	MIPI-DSI Rx Clock Lane Neg.	—
	DSIDP0	I/O	MIPI-PHY	MIPI-DSI Rx Data Lane Pos.	—
	DSIDM0	I/O	MIPI-PHY	MIPI-DSI Rx Data Lane Neg.	—
	DSIDP[3:1]	I	MIPI-PHY	MIPI-DSI Rx Data Lane Pos.	—
	DSIDM[3:1]	I	MIPI-PHY	MIPI-DSI Rx Data Lane Neg.	—
	DPLNP[1:0]	O	DP-PHY	embedded DisplayPort™ Output Main Link Pos.	—
DP Out (8)	DPLNM[1:0]	O	DP-PHY	embedded DisplayPort™ Output Main Link Neg.	—
	DPAUXP	I/O	DP-PHY	embedded DisplayPort™ Output AUX Channel Pos.	—
	DPAUXM	I/O	DP-PHY	embedded DisplayPort™ Output AUX Channel Neg.	—
	PREC_RES[1:0]	I	DP-PHY	Precision Resistance (3 kΩ @ 1%) connection	—
	DPI_PCLK	I/O	N	DPI Pixel Clock (max 154 MHz) (default: Input)	4mA
DPI Tx/Rx (Note3) (28)	DPI_VSYNC	I/O	N	DPI Vertical Sync (default: Input)	4mA
	DPI_HSYNC	I/O	N	DPI Horizontal Sync (default: Input)	4mA
	DPI_DE	I/O	N	DPI Data Enable (default: Input)	4mA
	DPI_D [23:0]	I/O	N	DPI Parallel Data (default: Input)	4mA

I ² C (3)	I ² C_SCL	OD	Sch	I ² C Clock	—
	I ² C_SDA	OD	Sch	I ² C Data	4mA
	I ² C_ADR_SEL	I	N	I ² C Slave Address Select 0: Slave address = 7'b1101_000 1: Slave address = 7'b0001_111	—
I ² S (4) (Note4)	SD/I ² S_OSCLK	I	N	I ² S Over Sampling Clock	—
	I ² S_BCLK	I	N	I ² S Bit Clock (max 12.5 MHz)	—
	I ² S_LRCLK	I	N	I ² S sample clock (max 192 kHz)	—
	I ² S_DATA	I	N	I ² S Data	—
GPIO (Note5) (2)	GPIO[1:0]	OD	5T-OD	GPIO or Test Control (Note1) GPIO[1:0] can be used for HPD support	4mA
POWER (10)	VDDC (1.2V)	NA	—	VDD for Internal Core (2)	—
	VDDS (1.8V)	NA	—	VDDS for IO Ring power supply (1)	—
	VDD_PLL18 (1.8V)	NA	—	VDD for DP PHY PLLs (1)	—
	VDD_DP18 (1.8V)	NA	—	VDD for DP PHY Main Channels (2)	—
	VDD_PLL912 (1.2V)	NA	—	VDD for PLL9 (1)	—
	VDD_DP12 (1.2V)	NA	—	VDD for DP PHY (2)	—
	VDD_DSI12 (1.2V)	NA	—	VDD for the MIPI DSI PHY (1)	—
GROUND (6)	VSS	NA	—	Ground (Core, DSI, I/O) (3)	—
	VSS_DP	NA	—	Ground (DP) (3)	—

Note 1: Pins with multiplexed Functional mode functions.

Note 2: When DSI-RX pins are not used, pull-up to VDD_DSI12 (1.2V).

Note 3: When DPI-TX/RX pins are not used for DPI-RX case, pull-down to GND.

Note 4: When I²S pins are not used, pull-down to GND.

Note 5: When GPIO pins are not used, pull-down to GND.

N: Normal IO

PHY: Either DP analog front end or MIPI D-PHY

Sch: Schmitt trigger input

OD: Open drain

5T-OD: 5 V tolerant bi-direction buffer with Open drain

3.2. TC358867XBG Ball Mapping

The mapping of TC358867XBG signals to the external pins is given in the following figure. (BGA array)

Top View											
	1	2	3	4	5	6	7	8	9	10	
A	INT	GPIO0	DPI_VSYNC	DPI_D0	VDDC	VDDC	DPI_D3	VDDS	I2C_SDA	I2C_SCL	
B	DSIDM0	DSIDP0	DPI_DE	DPI_HSYNC	DPI_D1	DPI_D2	DPI_D4	DPI_D7	DPI_D5	DPI_D6	
C	DSIDM1	DSIDP1							DPI_D9	DPI_D8	
D	DSICM	DSICP		I2S_LRCLK	I2S_BCLK	SD/ I2S_OSCLK	I2S_DATA		DPI_D13	DPI_D14	
E	VDD_DSI12	I2C_ADR_SEL		VSS	TEST3	VPGM0	DPI_D10		DPI_D16	DPI_D15	
F	DSIDM2	DSIDP2		VSS	VSS	TEST	DPI_D11		DPI_D_17	DPI_D_18	
G	DSIDM3	DSIDP3		VSS_DP	VSS_DP	VSS_DP	DPI_D12		DPI_D19	DPI_PCLK	
H	PREC_RES0	DISABLE_ASSR							DPI_D20	DPI_D21	
J	PREC_RES1	MODE1	DPLNPO	VDD_DP12	MODE0	DPLNP1	GPIO1	DPAUXP	RESX	DPI_D23	
K	REFCLK	VDD_DP18	DPLNM0	VDD_DP12	VDD_PLL18	DPLNM1	VDD_DP18	DPAUXM	VDD_PLL912	DPI_D22	

Figure 3.1 TC358867XBG 80-Ball Layout

4. Function of Major Blocks

TC358867XBG converts MIPI DSI / DPI Rx Link inputs to DP Link outputs. It consists of the following major blocks: MIPI Rx D-PHY, DSI Rx Protocol layer, DPI Rx Module, DP Tx Link Logic and DP PHY. The data format conversion of these two interfaces is handled in the FIFO block and the DP Link.

TC358867XBG also embeds the audio data from I2S Rx into the DisplayPort™ streaming. There is also an I²C slave block which can be used by the Host to access TC358867XBG registers. RegFile block consists of control/status registers that can be accessed through either I²C slave block or DSI link by Host. High level block diagram of TC358867XBG is shown in figures below.

The following sections describe each block in detail. The blocks discussed follow the data flow sequence, from MIPI DSI or DPI Rx (left) to DP Tx (right). I²C slave block is discussed last. Clock generation, including PLL, is also described later.

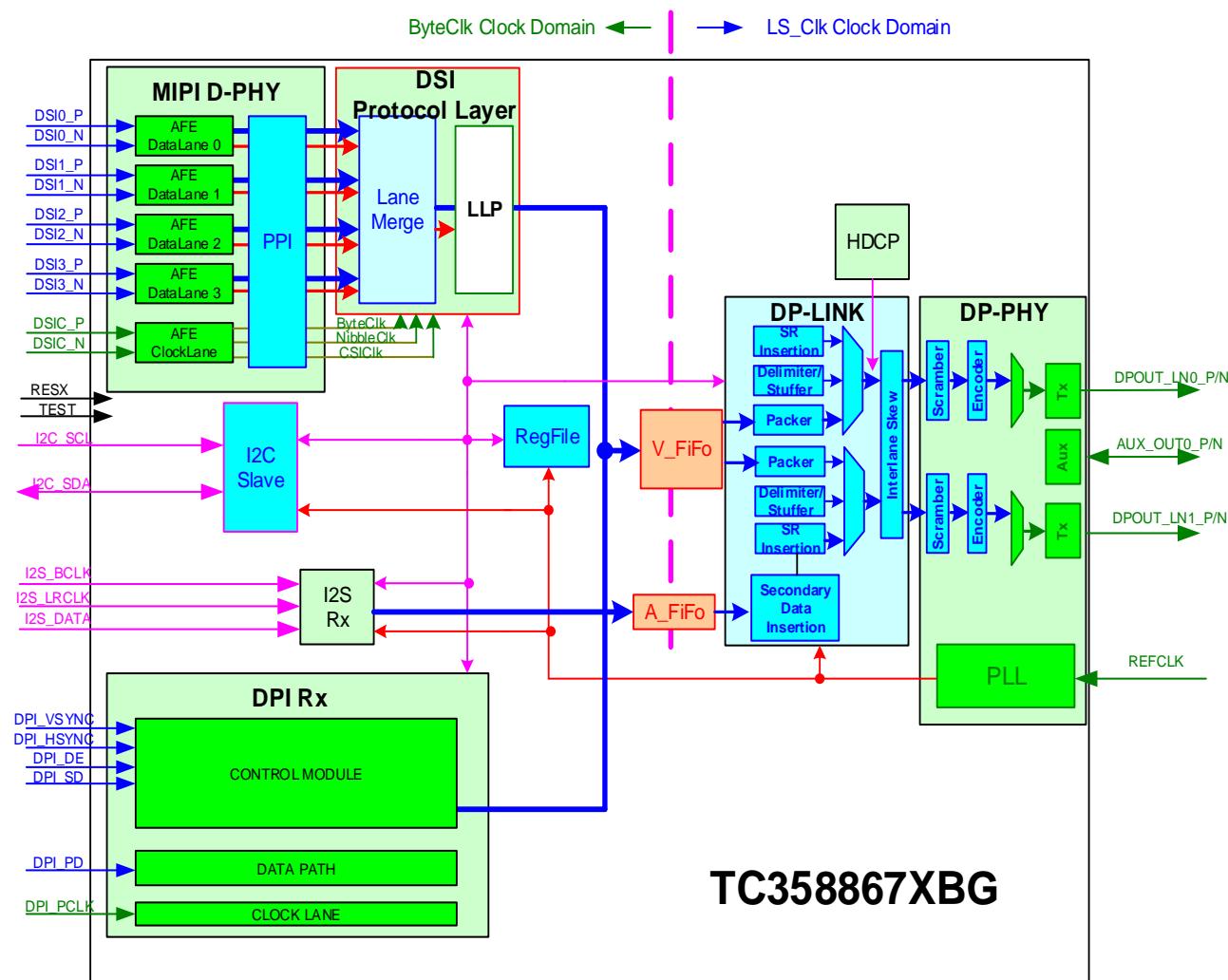


Figure 4.1 Block Diagram of TC358867XBG

4.1. MIPI DSI Rx

The MIPI DSI Rx is divided into two main portions: the analog D-PHY Rx and the digital DSI Rx consisting of PPI layer, lane merging, LLP layer, etc.

The MIPI DSI Rx supports up to four lanes in HS (High Speed) mode at data bit rate up to 1 Gbps per lane and one lane (lane 0) in LP (Low Power) mode at data bit rate up to 10 Mbps. The DSI-RX Interface can be used for:

- Streaming video to TC358867XBG FPD display panels
- Write and read access to the chip configuration and status registers.
- Enter and exit chip ultra-low power state (ULPS)

Accesses to chip configuration registers can be done either in LP mode over data lane 0 or in HS mode over one or more (up to 4) data lanes. After reset, only data lane 0 is enabled for LP mode reception until unless after DSI-Rx is configured and enabled for HS mode reception by accessing configuration registers through DSI-Rx LP mode transactions or I²C transactions.

4.1.1. Video Streaming

Video stream from Host over the DSI link will be described in the following context:

- Video transmission
- DSI packets for video transmission
- Pixel format

4.1.1.1. Video Transmission

TC358867XBG supports video transmission in DSI Video mode as described below.

Host is expected to transmit all video timing events and pixel data in proper sequence and time. Video timing events are transmitted using the DSI short packets:

- VSYNC Start
- VSYNC End
- HSYNC Start
- HSYNC End

VSYNC End and HSYNC End events can be sent by the Host in event mode, but TC358867XBG ignores them. TC358867XBG always uses the parameters programmed into the Horizontal Back Porch, Horizontal Sync width and Horizontal Front Porch (only in Frame Sync mode) to generate the output HSYNC End / VSYNC End timing.

They must be multiplexed with null (or blank) packets (or transitioned to LP idle cycle) and pixel data packets in the DSI serial link such that their reception at the chip provides VSYNC and HSYNC timing. Pixel data is expected to be transmitted using Pixel Stream packet types depending upon the video format:

- RGB565 (16bit: ID = 0x0E)
- RGB666 packed (18bit: ID = 0x1E)
- RGB666 loosely packed (18bit: ID = 0x2E)
- RGB888 (24bit: ID = 0x3E)
- YCbCr422 (16bit: ID = 0x2C)

Pixel data can be transmitted in non-burst or burst fashion. Non-burst refers to pixel data packet transmission time on DSI link being roughly the same (to account for packet overhead time) as active video line time on output display. Burst refers to pixel data packet transmission time on DSI link being less than the active video line time on output display.

Video mode transmission is further differentiated by the types of timing events being transmitted. Video pulse mode refers to the case where both sync start and sync end events (for frame and line) are transmitted. Video event mode refers to the case where only sync start events are transmitted.

The TC358867XBG chip supports both modes of video transmission, but VSYNC End and HSYNC End events are ignored in event mode. TC358867XBG always uses the parameters programmed into the Horizontal Back Porch, Horizontal Sync width and Horizontal Front Porch (only in Frame Sync mode) to generate the output HSYNC End / VSYNC End timing.

The video data extracted from the DSI Rx is written to the video buffer which provides for the synchronization between the DSI byte clock domain and the DisplayPort™ pixel clock domain.

4.1.1.2. DSI Packets for Video Transmission

DSI packets pertaining to video transmission are listed in the table below:

Table 4.1 DSI Packets pertaining to Video Transmission

Data Type	Short/Long Packet	Description	Supported	Main Use
6'h01	Short	Vsync start	Yes	Video timing events
6'h11	Short	Vsync end	Yes	
6'h21	Short	Hsync start	Yes	
6'h31	Short	Hsync end	Yes	
6'h09	Long	Null packet	Yes	Pixel data transmission
6'h19	Long	Blanking Packet	Yes	
6'h0E	Long	Pixel Stream, 16-bit RGB-565 format	Yes	
6'h1E	Long	Pixel Stream, 18-bit RGB-666 Packed format	Yes	
6'h2E	Long	Pixel Stream, 18-bit RGB-666 Loosely Packed format	Yes	
6'h3E	Long	Pixel Stream, 24-bit RGB-888 format	Yes	
6'h2C	Long	Pixel Stream, New YCbCr422 format	Yes	

4.1.1.3. Pixel Format

The chip supports RGB-565, RGB-666 packed or loose, RGB-888 pixel and the new DSI V1.02 Data Type Support format YCbCr 4:2:2 16bit in video data packets received from Host.

Pixel format is differentiated by the data type ID in the header of pixel stream packets received.

4.1.2. DSI Write/Read accesses to Chip Configuration Registers

The TC358867XBG Bridge Chip makes use of DSI Generic Long packets for Host to write and Generic short packets to read to its register set. Format of these packets is defined in the DSI specification. The payload of these packets is further defined here and is specific to the TC358867XBG Bridge Chip.

4.1.2.1. Write Access

Host sends a DSI Generic Long Write packet (Data ID = 0x29) over the DSI link for each write access transaction to the chip configuration registers. Payload of this packet is further defined as follows:

- First two bytes of the payload specifies the chip register 16-bit address, hence the address field. The first byte corresponds to address bits [7:0]. The following byte corresponds to address bits [15:8].
- Next four bytes specify the 32-bit data to be written to the address specified in the address field. The first of the four bytes corresponds to data bits [7:0]; next byte corresponds to data bits [15:8]; ...; last byte corresponds to data bits [31:24].

“Address auto-increment” capability is supported. That means Host can write to contiguous register address locations with one single packet. The address field specifies the address of the first register to be written to. Each group of following 4 bytes in the payload constitutes the 32-bit data to be written to each of the registers in the group starting with that addressed by the address field.

The word-count (WC) field in the packet header provides indication of how many registers are being written to by this packet. WC value must satisfy the following equation:

$$WC = 2 + 4*n,$$

where,

n is the number of registers being written to

n = 4 maximum

n = 0 is allowed, resulting in no action.

Other WC values result in undefined behavior.

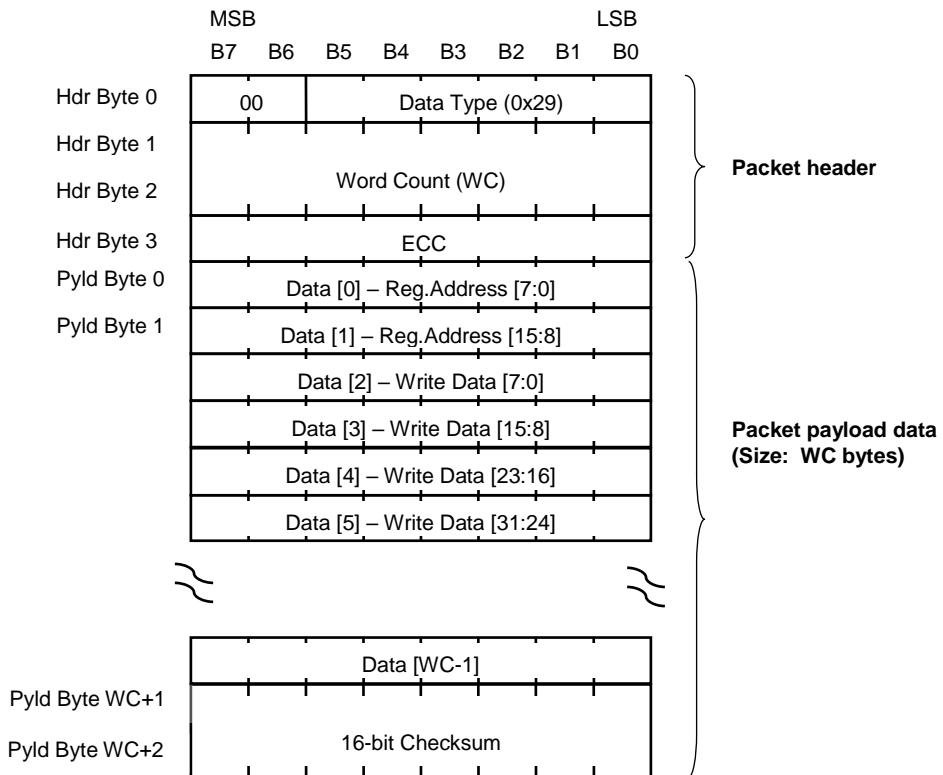


Figure 4.2 DSI Long Generic Write Packet

4.1.2.1.1. Read Access

Host sends a DSI Generic Read packet (Data ID = 0x24) over the DSI link for each read request transaction to the chip configuration registers. Payload of this packet is further defined as follows:

- The two data bytes of the packet specify the chip register 16-bit address, hence the address field. Data byte 0 corresponds to address bits [7:0]. Data byte 1 corresponds to address bits [15:8].

Immediately after sending this packet, Host performs a Bus-Turn-Around (BTA) sequence to transfer the DSI link ownership to the TC358867XBG Bridge Chip for it to send a read response packet. If a BTA does not immediately follow the read request packet, then the read transaction will be abandoned and no read response will be returned. The chip detects the BTA sequence and takes one of the following actions:

- **Case 1:** If the read request packet arrived with no errors (and there are no previously stored errors since the last reverse communication with Host), the chip forms and sends a Generic Long Read Response packet (Data ID = 0x1A) which returns the 4-byte content of the register being addressed.

- **Case 2:** If errors are detected during reception of the read request packet (or there are previously stored errors since the last reverse communication with Host), the chip sends Host an “Acknowledge and Error Report” packet (Data ID = 0x02). Please refer to MIPI DSI Specification (mentioned in references) for the details of the error packet.
- **Case 3:** If an ECC correctible error in the request was detected and corrected, the chip forms and sends the Generic Long Read Response packet (same as in case 1) followed by the “Acknowledge and Error Report” packet.

After sending the response, the chip performs its own BTA sequence to give the DSI link ownership back to the Host.

The Generic Short Read Request packet structure is shown in the following figure.

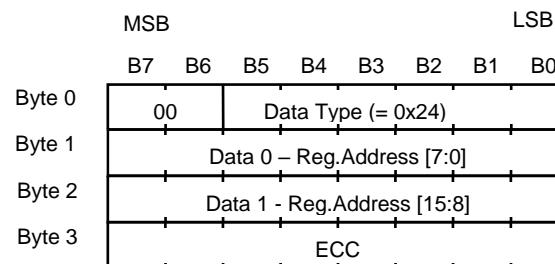


Figure 4.3 DSI Generic Short Read Request Packet

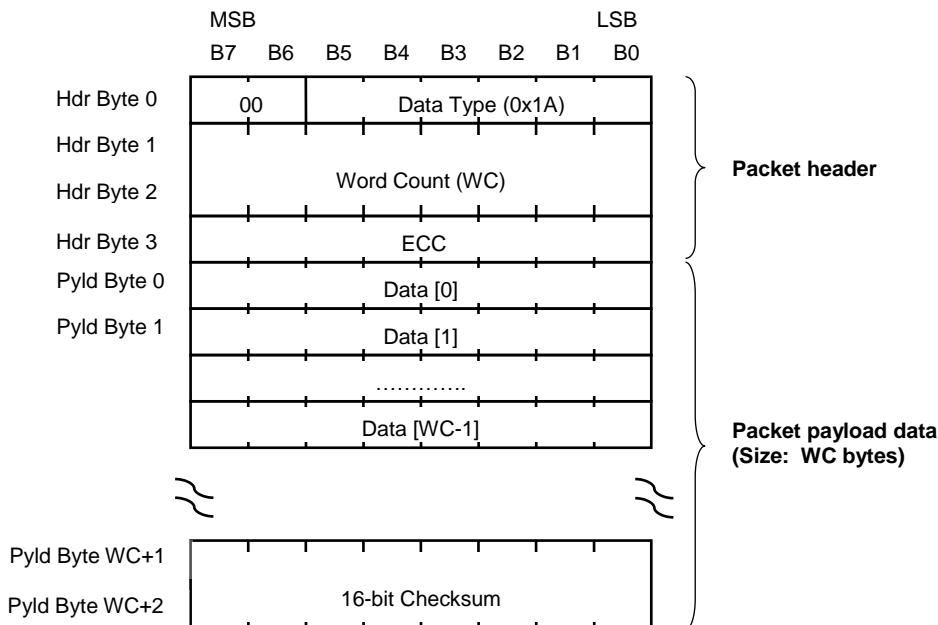


Figure 4.4 DSI Generic Long Read Response packet

4.1.3. Exit/Enter chip power-down state using DSI interface

Host sends a ULPS Entry or ULPS Exit low-power mode sequence over the DSI link to instruct the chip to enter or exit power-down state.

Following power-on reset, the chip goes in standby state, ready to receive communication packets from Host over the DSI link.

When the display is turned off and the video path from Host to the display panel through TC358867XBG Bridge Chip is not active, Host sends a ULPS Entry command to instruct the chip to transition into power-down state. Upon receiving this command, the chip powers down all of its functions except for the DSI low-power receive function (and I²C block) which is used to listen to a ULPS Exit command.

Subsequently, upon receiving the ULPS Exit command, the chip will exit the power-down state and transition to standby state.

4.1.4. Reverse Low Power Transmission

The chip supports reverse Low Power transmission as described in the MIPI DSI Specification for the following types of transactions:

Acknowledge: A Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication, has been received with no errors.

Acknowledge and Error Report: A Short packet sent if any errors were detected in preceding transmissions from the host. Once reported, accumulated errors in the error register are cleared.

Read Response: May be a Short or Long packet that returns data requested by the preceding read request command from Host.

The control flow of which packets to be returned is shown in the following figure.

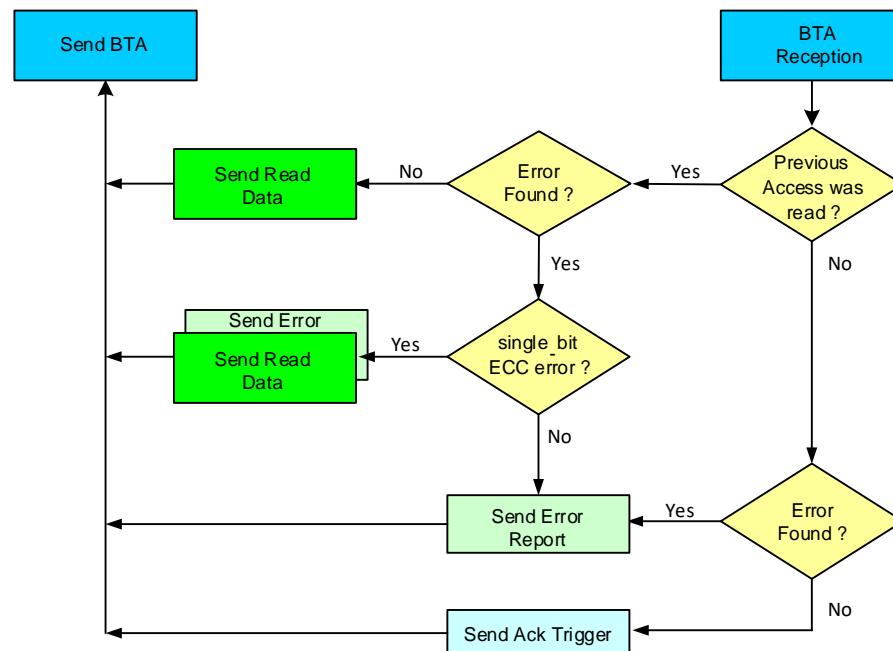


Figure 4.5 Control Flow of Reverse_link Transactions

4.1.5. DSI Packet Type Support

Following tables summarize the DSI packet types that the chip supports. Unrecognized or unsupported packet types will be treated as no-ops and error status will be saved and reported.

Table 4.2 Forward-Link DSI Packets Support

Data Type	Short/Long Packet	Description	Supported
6'h01	Short	Vsync start	Yes
6'h11	Short	Vsync end	Yes
6'h21	Short	Hsync start	Yes
6'h31	Short	Hsync end	Yes
6'h08	Short	EoT packet	Yes
6'h02	Short	Color Mode Off Command	No
6'h12	Short	Color Mode On Command	No
6'h22	Short	shut down peripheral	No
6'h32	Short	turn on peripheral	No
6'h03	Short	Generic short write, no parameters	No
6'h13	Short	Generic short write, 1 parameter	No
6'h23	Short	Generic short write, 2 parameters	No
6'h04	Short	Generic Read, no parameters	No
6'h14	Short	Generic Read, 1 parameter	No
6'h24	Short	Generic Read, 2 parameters	Yes
6'h05	Short	DCS write, no parameters	No
6'h15	Short	DCS write, 1 parameter	No
6'h06	Short	DCS read	No
6'h37	Short	Set Maximum Return Packet Size	Yes
6'h09	Long	Null packet, no data	Yes
6'h19	Long	Blanking Packet, no data	Yes
6'h29	Long	Generic Long Write	Yes
6'h39	Long	DCS Long Write/write LUT Command packet	No
6'h0E	Long	Packed Pixel Stream, 16-bit RGB, 565 format	Yes
6'h1E	Long	Packed Pixel Stream, 18-bit RGB, 666 format	Yes
6'h2E	Long	Loosely Packed Pixel Stream, 18-bit 666 RGB format	Yes
6'h3E	Long	Packed Pixel Stream, 24-bit RGB, 888 format	Yes
6'h2C	Long	Packed Pixel Stream, 16-bit YCbCr, 422 format	Yes

Table 4.3 Reverse-Link DSI Packets Support

Data Type	Short/Long Packet	Description	Supported
00h – 01 h	Short	Reserved	—
02h	Short	Acknowledge and Error Report	Yes
03h – 7h	—	Reserved	—
08h	Short	End of Transmission packet (Eotp)	No
09h – 10h	—	Reserved	—
11h	Short	Generic Short Read Response, 1 byte returned	Yes
12h	Short	Generic Short Read Response, 2 bytes returned	Yes
13 – 19h	—	Reserved	—
1Ah	Long	Generic Long Read Response	Yes
1Bh	—	Reserved	—
1Ch	Long	DCS Long Read Response	No
1Dh – 20h	—	Reserved	—
21h	Short	DCS Short Read Response, 1 byte returned	No
22h	Short	DCS Short Read Response, 2 bytes returned	No
23h – 3Fh	—	Reserved	—

4.2. MIPI DPI Rx

The MIPI DPI Rx supports up to 24 bits of parallel pixel data (24, 18 or 16-bit interface) at pixel rate of up to 154 MHz.

Accesses to chip configuration registers can be done either through I²C transactions.

4.2.1. Video Streaming

Video stream from Host over the DPI link will be described in the following context:

- Video transmission
- Pixel format

4.2.1.1. Video Transmission

TC358867XBG supports video transmission from DPI interface as described below.

TC358867XBG relies on the host to continuously provide complete frames of image data at a sufficient frame rate to avoid flicker or other visible artifacts. The displayed image, or *frame*, is comprised of a rectangular array of pixels. The frame is transmitted from the host as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

- Vsync indicates the beginning of each frame of the displayed image.
- Hsync signals the beginning of each horizontal line of pixels.
- Each pixel value (16-, 18-, or 24-bit data) is transferred from the host during one pixel period. The rising edge of PCLK is used to capture pixel data.
- Since PCLK runs continuously, control signal DE is used to indicate when valid pixel data is being transmitted on the pixel data signals.

Figure below defines timing parameters for DPI Rx operation.

The PCLK provides the pixel clock input timing. The pixel data received from the DPI Rx is written to the video buffer which provides for the synchronization between the incoming pixel clock rate and the DisplayPort™ pixel clock rate.

Unlike DSI interface, there is no embedded information regarding the pixel format in the data received from the DPI interface. Therefore, the Host needs to program the input pixel format in the TC358867XBG configuration registers using the I²C accesses prior to the start of video streaming.

In DPI Rx case (unlike DSI Rx case), the video transmission is always assumed to be in non-burst mode, meaning pixel data transmission time on DPI link being roughly the same as active video line time on output display.

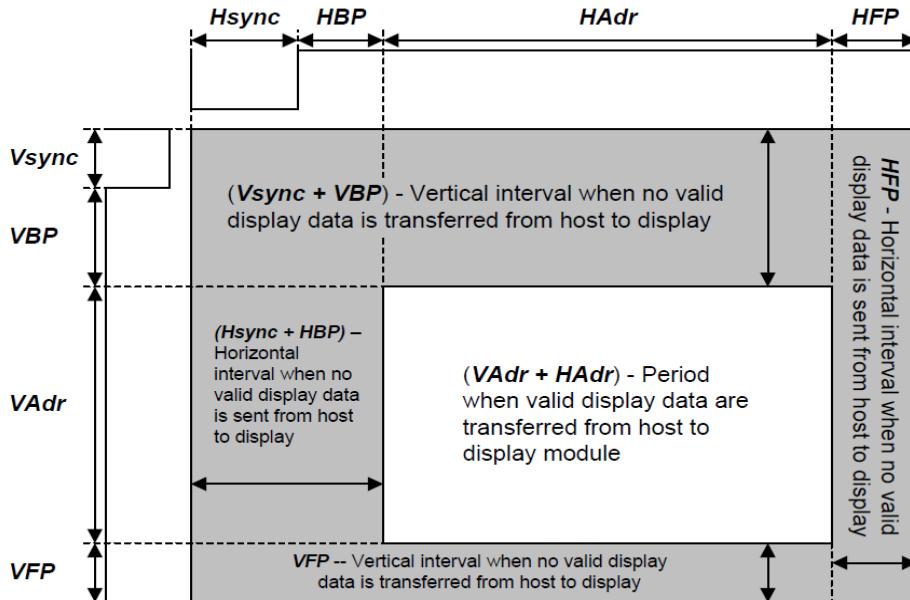


Figure 4.6 DPI Timing parameters

Each of these timing parameters (mentioned below) need to be specifically programmed into the TC358867XBG configuration registers by the DPI Host through I²C accesses prior to the start of the video streaming. This is required to help TC358867XBG accurately regenerate the required frame timing on the DisplayPortTM Tx link.

4.2.1.2. Pixel Format

Pixel format is differentiated by the data type programmed by the DPI host (prior to the start of video data transmission) in the TC358867XBG configuration registers.

The TC358867XBG chip supports the following pixel formats in video data received from DPI Host.

- RGB565 (16bit) – LSB aligned
- RGB565 (16bit) – LSB 8-bit aligned
- RGB565 loosely packed (16bit)
- RGB666 packed (18bit) – LSB aligned
- RGB666 loosely packed (18bit)
- RGB888 (24bit)

The mapping of data bits, as components of primary pixel color values R, G, and B, to signal lines at the DPI interface are shown in the figure below for all the possible formats mentioned above.

Signal Line	16-bit			18-bit		24-bit
	Configuration 1	Configuration 2	Configuration 3	Configuration 1	Configuration 2	
D23	(not used)	R7				
D22	(not used)	R6				
D21	(not used)	(not used)	R4	(not used)	R5	R5
D20	(not used)	R4	R3	(not used)	R4	R4
D19	(not used)	R3	R2	(not used)	R3	R3
D18	(not used)	R2	R1	(not used)	R2	R2
D17	(not used)	R1	R0	R5	R1	R1
D16	(not used)	R0	(not used)	R4	R0	R0
D15	R4	(not used)	(not used)	R3	(not used)	G7
D14	R3	(not used)	(not used)	R2	(not used)	G6
D13	R2	G5	G5	R1	G5	G5
D12	R1	G4	G4	R0	G4	G4
D11	R0	G3	G3	G5	G3	G3
D10	G5	G2	G2	G4	G2	G2
D9	G4	G1	G1	G3	G1	G1
D8	G3	G0	G0	G2	G0	G0
D7	G2	(not used)	(not used)	G1	(not used)	B7
D6	G1	(not used)	(not used)	G0	(not used)	B6
D5	G0	(not used)	B4	B5	B5	B5
D4	B4	B4	B3	B4	B4	B4
D3	B3	B3	B2	B3	B3	B3
D2	B2	B2	B1	B2	B2	B2
D1	B1	B1	B0	B1	B1	B1
D0	B0	B0	(not used)	B0	B0	B0

Figure 4.7 DPI Interface color coding

4.3. I2S Audio Rx

The I2S interface is used to transmit the audio data for the DisplayPort™ output. The I2S interface has the following features:

- Support for slave mode (BCLK, LRCLK and audio over-sampling clock input from Host).
- Support for sampling frequencies of 32, 44.1, 48, 88.2, 96, 176.4 & 192 kHz.
- Supports 2 channels
- Supports 16, 18, 20 or 24bits per sample.

Audio stream from Host over the I2S interface will be described in the following context:

- Audio transmission & alignment modes.
- Channel slots, sample bit-width and bit clock.
- I2S Rx to DisplayPort™ Tx interface

4.3.1. Audio Transmission & Alignment modes

TC358867XBG relies on the host to continuously provide audio streaming at proper bit rate corresponding to number of channels and sampling frequency/sample bit-width. The BCLK provides the bit clock for the incoming audio serial data while the LRCLK provides the word select (for two channels) or in other words, the sampling frequency. The audio data samples are transmitted serially over the I2S_DATA line with MSB first.

Figure below shows the basic audio transmission related waveform over I2S interface.

The I2S interface supports 3 different bit alignments of the valid data, which are:

- Standard mode - Data is sent with a leading clock cycle of invalid data within one frame. The first valid data bit is the second bit.
- Left aligned – where first valid data bit is transmitted as first bit of a frame.
- Right aligned – where the last valid data bit is transmitted as last bit of a frame.

The following diagram shows the different configurations.

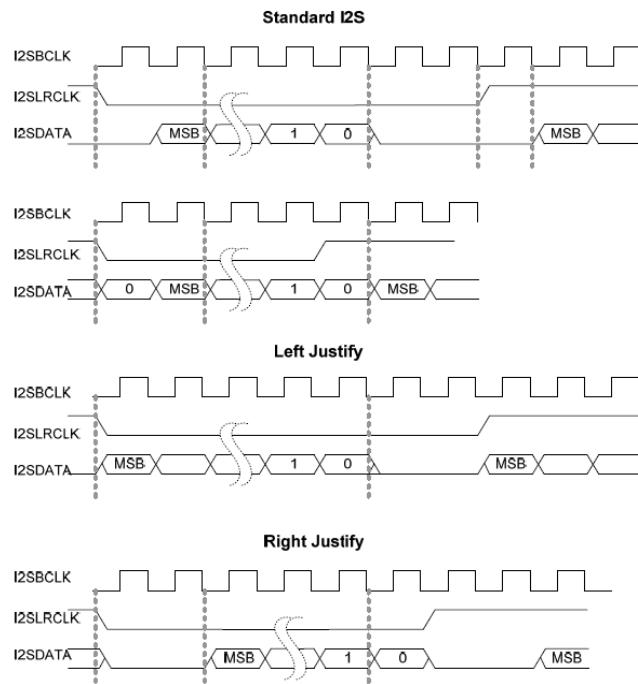


Figure 4.8 I2S Interface timing

4.3.2. Channel slots, Sample bit-width and bit clock

As shown in the diagrams above, the I2S transmission uses the LRCLK to identify the serial data bits to channel association. The LRCLK toggles at the audio sampling frequency. Each channel has its slot in the I2S serial data transmission, marked by LRCLK being high (= 1) or low (= 0). Each slot has sample bit-width number of data bits transmitted sampled at every posedge of BCLK. The BCLK relationship to the LRCLK and sample bit-width is thus:

$$\begin{aligned}
 F_{BCLK} &= F_{LRCLK} \times N_{\text{channel}} \times \text{SampleWidth} \\
 &= 192/1000 \times 2 \times 32 \text{ (for } F_{\text{sample}} = 192 \text{ kHz, dual channel)} \\
 &= 12.28 \text{ MHz}
 \end{aligned}$$

4.3.2.1. Sample Width possibilities

Different sample width options are possible for I2S input data. The host must program the sample width into the Audio control register. The default mode is where sample width of 24 bits is sent in a 32bit time slot. The remaining 8 bits in the time slot for the channel may not be used depending upon the IEC60958 status bits fill option chosen by the host. If the host chooses to send the IEC60958 status bits along with the audio bit stream, then the remaining 8 bits of data within the 32 bit sample period are used to transmit such information. If the host chooses not to send the IEC60958 information then the IEC60958 status bits are generated and inserted by the I2S receiver (explained later in detail).

4.3.3. I2S Rx to DisplayPort™ Tx Interface

TC358867XBG relies on the host to continuously provide audio streaming at proper bit rate corresponding to number of channels and sampling frequency/sample bit-width. The BCLK provides the bit clock for the incoming audio serial data while the LRCLK provides the word select (for two channels) or in other words, the sampling frequency. The audio data samples are transmitted serially over the I2S_DATA line with MSB first.

The I2S_BCLK provides the audio data input timing. The audio sample data received from the I2S Rx is written to the audio buffer which provides for the synchronization between the incoming audio clock rate and the DisplayPort™ Link Symbol clock (LSCLK) rate.

The Host needs to program the parameters of the audio transmission into the TC358867XBG configurations registers using the I²C accesses prior to the start of audio streaming for use by the DisplayPort™ transmitter module for framing the audio data packets. These parameters are:

- Sampling frequency
- Sample bit-width
- Number of channels
- IEC60958 status bits fill mode
- IEC60958 validity bit and channel status bits (for auto fill mode)

The audio data is sent over DisplayPort™ in 3 parts as follows:

- The main audio sample data is sent as secondary data packets during the H-blanking and V-blanking intervals.
- The audio Time Stamp packets are sent at least once per frame during the V-blanking period.
- The Audio InfoFrame packets are sent once per frame during the V-blanking period.

4.3.3.1. Audio Info Frame packet

The contents of Audio Info frame packet correspond to the audio sampling parameters programmed into the TC358867XBG configuration registers by the Host. The header for the audio info frame packet uses information programmed into the AudCfg0 & AudCfg1 registers, while the data bytes in the info frame packet use information programmed into the AudIFData0 to AudIFData6 registers.

4.3.3.2. Audio Time Stamp packet

The audio Time Stamp information contains the M/N values required to regenerate the audio sampling clock at the DisplayPort™ receiver. This audio M/N values are derived (through a look-up table) as follows in accordance with the DisplayPort™ specification corresponding to an audio sampling frequency programmed into the TC358867XBG configuration registers:

$$M/N = 512 \times F_{\text{sample}} / F_{\text{LSCLK}}$$

The header for the audio time stamp packet uses information programmed into the AudCfg0 register. The data bytes in the time stamp packet use the M & N values calculated as below:

For synchronous mode: M & N values calculated based on the look-up table as per DisplayPort™ specification.

For asynchronous mode, an internal M calculator is used based on the N value (usually 2^{15}) programmed into the DPx_AudMNGen1 registers. Host is assumed to provide the oversampling clock ($512 \times F_{\text{sample}}$) on the SD input pin and program the Sys_Control register accordingly.

If the audio over-sampling clock is not $512 \times F_{\text{sample}}$, then an approximated M value will be left-shifted appropriately to provide the final Maud value to DisplayPort™.

4.3.3.3. Audio Stream packet

As the audio packets might be streaming in continuously, but they cannot be transmitted unless the higher priority video pixels have been sent out on the DisplayPort™ and the H-blanking/V-blanking slot is available, so a small audio buffer (FIFO) is required to hold the audio incoming sample data.

The size of this FIFO depends upon the longest line of video data that needs to be sent out at slowest pixel clock frequency assuming audio data coming in at the highest possible bit clock. This has been calculated to be around 256 bytes (keeping some buffer).

The header for the audio stream packet uses information programmed into the AudCfg0 & AudCfg1 registers.

4.3.4. Audio Stream Start / Stop Procedure

I2S interface is an asynchronous interface.

4.3.4.1. Audio streaming Start Procedure

1. Before starting the I2S streaming, the I2S soft reset bit should be asserted and de-asserted.
2. Host should set the Audio_En bit in I2SCfg0 register to 1.

In case TC358867XBG has to generate the Preamble and other IEC60958 bits, this step marks the beginning of the 192 sample sub-block (preamble “B”).

3. Host should start toggling the BCLK and start streaming the audio data with the first BCLK.

4.3.4.2. Audio Stream Stop Procedure

1. Host mutes the audio (optional).
2. Host disables the Audio_En bit in the I2SCfg0 register.
3. Host continues to toggle the BCLK for minimum of one sub-block equivalent bits (2 channels, 1 sample per channel, 32bits per sample).

4.4. DisplayPort™ Tx

This section describes the details on DisplayPort™ transmitter (DP Tx) used to control the Display Panel(s) connected to it and to send video and audio data to the Display Panels.

4.4.1. Main Channel Overview

DisplayPort™ Main Channel Tx comprises of the digital portion and the analog portion. Detail of the analog portion is beyond the scope of this document.

4.4.1.1. Main Channel – Digital Controller

Main Channel receives the following kinds of data/information:

- Clocks (Pixel and Link Clocks).
- Timing Signals (Framing timing information)
- Video Data
- Secondary Data (including the Audio Data)
- Info Data (including information about video data, audio data, clocks, etc. to help the DP receiver properly extract the audio and video data out of the DP frames at the receiving end (Display Panel).

4.4.1.1.1. Main Channel – Clocks

The clocks used by the Main Channel are:

- Pixel Clock (PCLK) or the Stream clock (STRMCLK) used to stream in the video data into the internal FIFO for subsequent packing into the DP frames.
- Link Clock (High Speed clock = 1.62 GHz or 2.7 GHz) used to send data out serially on the DP differential pairs.
- Link Symbol Clock (LSCLK = 1/10 of high speed link clock) used to read the data from FIFO and to pack the data for presenting to the analog DP PHY layer.

4.4.1.1.2. Main Channel – Timing Signals

The main timing signals received by the Main Channel are:

- VSYNC/HSYNC: Vertical and Horizontal Framing synchronization signals.
- DE: Data Enable, marking the active pixel line period in each line.
- Additionally, lot of timing information is used from the programming registers of the TC358867XBG to properly construct the DP transmit frame based on the available bandwidth, available number of Main Channel links, required video frame size and video frame rate and audio samples to be stuffed in the frames.

4.4.2. Aux Channel Overview

The Aux channel is a slow speed channel running at 1 MHz which is used for the following purposes:

- DisplayPort™ receiver Link capability reads
- DisplayPort™ receiver Link training control
- DisplayPort™ receiver Link status reads
- DisplayPort™ receiver EDID/DPCD reads
- DisplayPort™ receiver MCCS control

The Aux channel consists of a digital & an analog portion.

4.4.2.1. Aux Channel – Digital Controller

DP TX supports two methods of initiating AUX transactions to a DP sink. One mechanism involves the host writing to DP TX registers space to initiate transactions while the other involves transactions from I²C host. Both methods are described below.

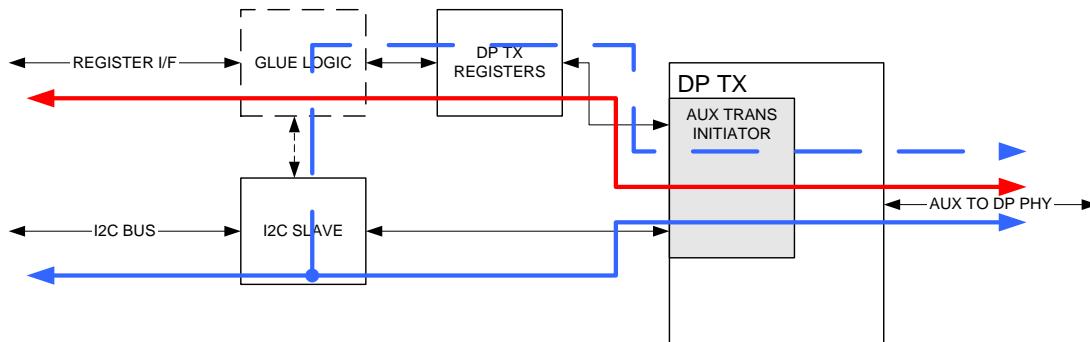


Figure 4.9 AUX transaction initiators to DP Tx

4.4.2.1.1. Register access based transactions

The Aux channel uses the TC358867XBG registers for initiating transactions to the DP receiver. Both Writes and Reads can be done using the TC358867XBG registers for Aux channel as mentioned below.

4.4.2.1.1.1. Write transactions

Host writes the target address and the write data (up to 16 bytes in case of burst write) to the TC358867XBG AUXADDR and AUXWDATA0 to AUXWDATA3 registers respectively. Following this, the Host writes the configuration register AUXCFG0 for command (write), burst size and info whether this is address only transaction (mainly for reads).

Write to the configuration register initiates the transaction on the DP Aux channel to the DP receiver.

The DP receiver can respond back with an ACK, NACK or DEFER.

Software should poll on AUXSTATUS.a_busy to see if it is de-asserted before reading the AUXSTATUS.aux_bytes and AUXSTATUS.aux_status to confirm that the transaction was successful. No new transactions can be initiated when AUXSTATUS.a_busy is set.

4.4.2.1.1.2. Read transactions

Host writes the target address to the TC358867XBG AUXADDR register. Following this, the Host writes the configuration register AUXCFG0 for command (read), burst size and info whether this is address only transaction (mainly for reads).

Write to the configuration register initiates the transaction on the DP Aux channel to the DP receiver.

The DP receiver can respond back with an ACK or DEFER.

Software should poll on AUXSTATUS.a_busy to see if it is de-asserted before reading the AUXSTATUS.aux_bytes and AUXSTATUS.aux_status to confirm that the transaction was successful. No new transactions can be initiated when AUXSTATUS.a_busy is set.

4.4.2.1.2. I²C over AUX based transactions

In this case, the transactions coming from the I²C master are directly mapped over the Aux channel as per the DisplayPortTM specification.

4.4.3. DisplayPortTM Link Establishment

Before the DP link can be used for video transmission, the TC358867XBG side DP PHY needs to be initialized following which, the TC358867XBG side DP link and DP receiver side DP link configurations need to be matched – the process of reaching a matched configuration is called link training.

A high level DisplayPortTM initialization process is shown in the flow diagram below.

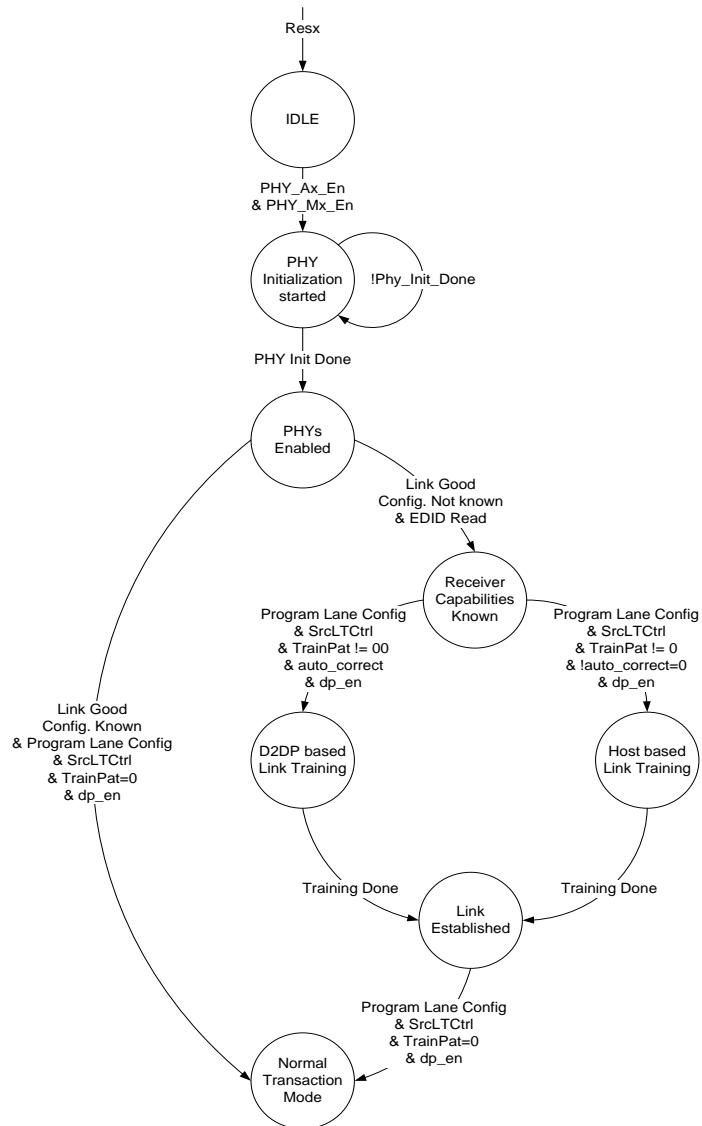


Figure 4.10 DisplayPort™ initialization – a high level overview

TC358867XBG supports two modes of link training as follows:

- Host based Link Training (default)
- Auto-correction Link Training

In either of the above modes, the following information sequence is required for successful completion of link training.

- Link capability read
- Link configuration & training
- Link status read

During the Link configuration & training step, the DP link's parameters like link frequency, number of channels, pre-emphasis levels, etc. may need to be changed based on the link training status read from the DP receiver. The two modes of link training mentioned above differ in the fact that in Host-based Link Training, these parameter adjustments are done by the Host by TC358867XBG register accesses, while in Auto-correction Link Training, some of these adjustments are automatically done by the TC358867XBG based on a preset sequence.

The link training support is divided into two parts as per DisplayPort™ specifications and handled as below:

4.4.3.1. Sink DPCD Read

Host reads the DP receiver's capabilities (DPCD registers) by accessing DP Aux control registers with appropriate DP addresses corresponding to DP Sink DPCD registers. Based on this information read, the Host needs to program the Link parameters for link training as explained in next sections.

4.4.3.2. Link Training

At the end of the previous phase (DP Sink capability read) the capabilities of the DP receiver are known to the Host and can be used for the Link Training. Three possibilities exist after this as explained below.

4.4.3.2.1. Fast Link Training

In case, the good link settings are already known for the source and sink devices, then no link training is required and the Host can simply program the known good values in the DPx_SrcCtrl register for actual transfers on the DisplayPort™ link.

4.4.3.2.2. Host Controlled Link Training

For Host controlled link training mode, the Host knows the Sink capabilities as a result of DPCD reads in previous phase. Host performs all the sequences required for each stage of link training through register read/write.

4.4.3.2.3. TC358867XBG Controlled Link Training

For TC358867XBG controlled link training mode, the Host knows the Sink capabilities as a result of DPCD reads in previous phase. In this mode, wait time required for the link training is inserted automatically referring to register value. And based on the result of link training in each phase, if increase of voltage swing/pre-emphasis is required, these values are changed automatically. Link speed and link bandwidth are not changed automatically.

4.5. Parallel Output Mode

The parallel output mode can be enabled by enabling the “S2P” bit in the POCTRL register. In this mode, TC358867XBG can output RGB888 format (24 bits of parallel pixel data) at pixel rate of up to 100 MHz. Maximum resolution supported is WXGA (1280x800).

TC358867XBG relies on the host to continuously provide complete frames of image data at a sufficient frame rate to avoid flicker or other visible artifacts. The displayed image, or *frame*, is transmitted to the display panel as sequence of pixels in a rectangular array, with each horizontal line of the image data sent as a group of consecutive pixels.

- Vsync indicates the beginning of each frame of the displayed image.
- Hsync signals the beginning of each horizontal line of pixels.
- Each 24-bit pixel is transferred during one pixel period on rising edge of PCLK [default].
- Since PCLK runs continuously, “DE” is used to indicate valid pixel data on data signals.

The pixel data transmitted over the parallel output is read from video buffer by the LCD controller. The video buffer provides for the synchronization between incoming pixel data from DSI Rx and the parallel output pixel clock rate (PCLK).

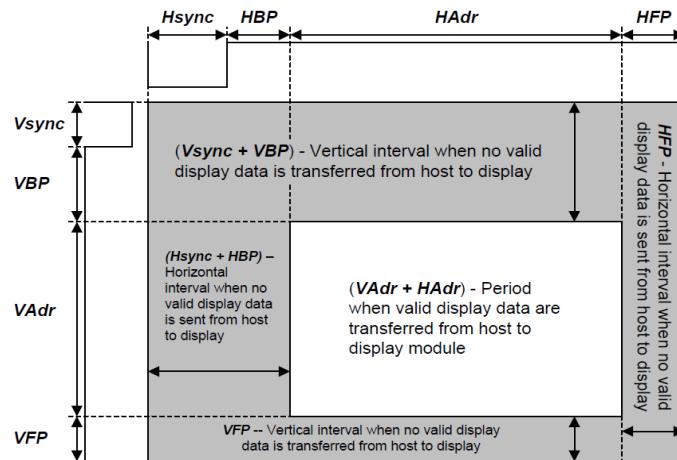


Figure 4.11 DPI Timing parameters

Each of these timing parameters need to be specifically programmed into the TC358867XBG Video Path Configuration registers by Host through DSI, I²C or SPI transactions prior to the start of video streaming to help TC358867XBG accurately regenerate required frame timing on parallel output port.

Irrespective of the format of incoming video stream on DSI Rx, the output format on parallel output port is always RGB888 with the mapping of components of primary pixel color values R, G, and B to the 24bits of parallel data as:

$$\text{DPI_D}[23:0] = \{\text{R}[7:0], \text{G}[7:0], \text{B}[7:0]\}$$

4.6. GPIO Interface

The TC358867XBG supports 2 GPIO pins that are individually configurable as either input or output.

Host configures the direction of GPIO pins by writing to register GPIO Control register. By default the GPIOs are in input mode.

As input, the logic state on the GPIO pins are reflected in the register GPI which Host can read.

When configured as output, the GPIO pins are driven by the state of register GPO which Host can write to.

Some of the GPIO pins have alternate functions as mentioned in the pin description table.

4.7. I²C Slave Interface

The TC358867XBG Bridge Chip incorporates an I²C Slave Interface port which Host can drive to configure registers in the chip.

The following features are supported:

- Fail safe I²C pad operation
- Up to 400 kHz fast mode operation
- High speed tolerant: can be plugged into a I²C high speed capable system without disturbing the high speed transmission
- No support for general call address
- Supports 16 bit index value for TC358867XBG I²C slave access
- 7-bit slave address recognition
- The I²C slave device address for TC358867XBG chip is hardcoded to be “1101 000” (0x68) or “0001 111” (0x0F) (selected using input setting – refer boot-strap section).

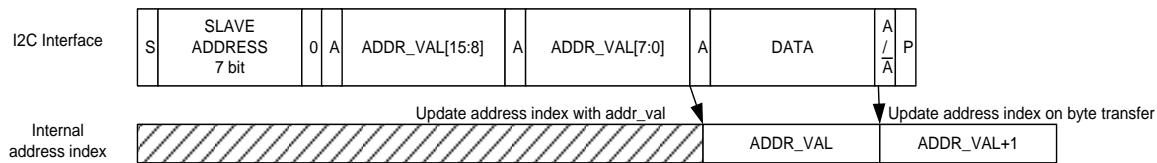
Internally to TC358867XBG chip, the I²C Slave interface port is sampled by a clock which is derived from the PLL_REF clock.

It is the responsibility of the Host to make sure an I²C slave transaction is not issued to the TC358867XBG chip while another register access from DSI link is taking place and vice versa.

The I²C slave function supports a fixed slave address only and does not support general call address. The I²C slave function does not require any programmable configuration parameters.

4.7.1. Providing Register Address over I²C Bus

The I²C slave function requires the interfacing I²C master to provide the register address of the TC358867XBG register to be accessed. The I²C slave function loads the first two bytes following a write command as the register address (address index) to be accessed (see Figure 4.12 and Figure 4.13).



S = Start condition

S_r = Repeated start condition

A = Acknowledge

Ã = Not Acknowledge

P = Stop bit

Figure 4.12 Register Write Transfer over I²C Bus

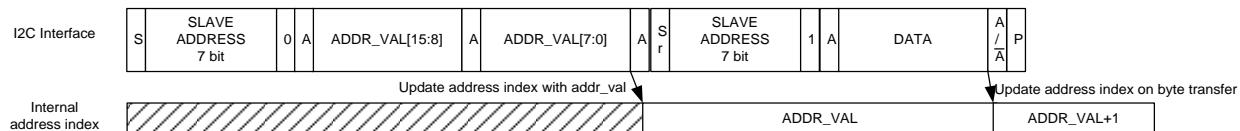


Figure 4.13 Random Register Read Transfer over I²C Bus

I²C slave function supports random write accesses and both random and continuous read accesses (see Figure 4.14).

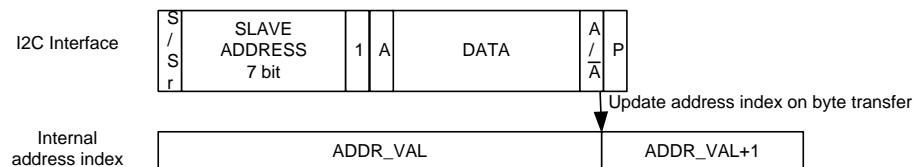


Figure 4.14 Continuous Register Read Transfer over I²C Bus

4.7.2. I²C Write Access Translation

Registers in TC358867XBG are 16 bit aligned. This implies that I²C accesses to registers should always be done on 16 bit boundaries. The I²C slave will update an internal 16-bit write data register indexed by the lsb of the internal address index. Write access to TC358867XBG registers over the register interface is performed when a byte of data has been received and the internal address index has hit a 16-bit boundary. This mechanism allows 16-bit aligned registers to be updated simultaneously based on the register address value presented on the I²C bus interface. Note that data transferred on the I²C bus is sent MSB first.

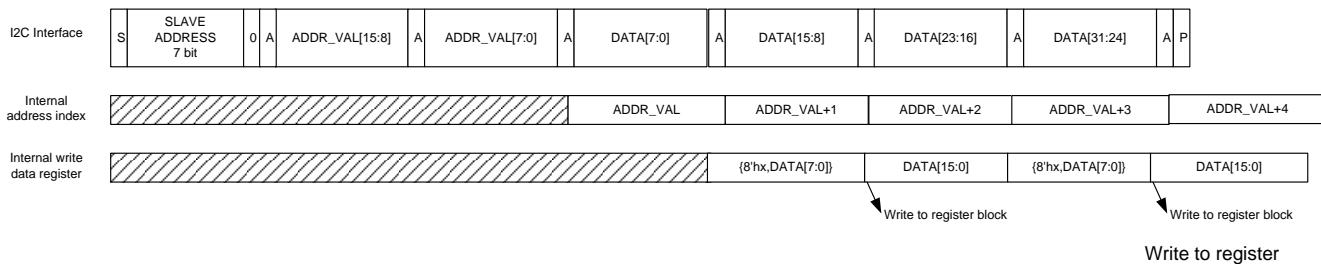


Figure 4.15 I²C Write Transfers Translated to Register Write Accesses

4.7.3. I²C Read Access Translation

Registers in TC358867XBG are 16 bit aligned. This implies that I²C accesses to registers should always be done on 16 bit boundaries. The I²C slave will update an internal 16-bit read data register when it received the I²C read command or when a byte transfer has completed and the internal address index has hit a 16-bit boundary. Data from the internal read register indexed by the lsb of the internal address index is then transferred over the I²C bus. This mechanism allows 16-bit aligned registers to be read without any side effects. Note that data transferred on the I²C bus is sent MSB first.

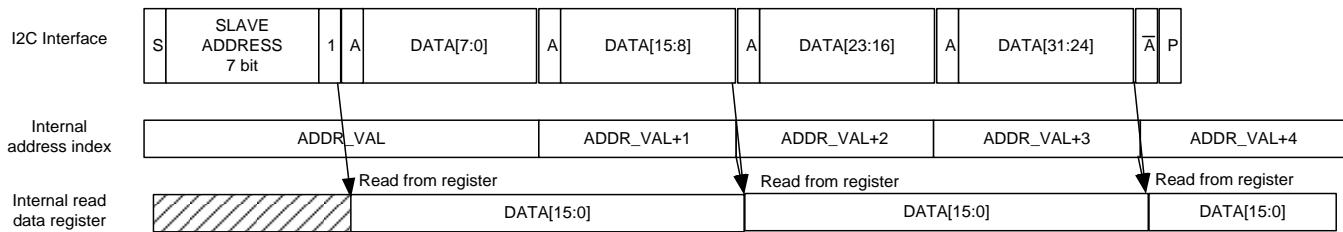


Figure 4.16 I²C Read Transfers to Register Read Accesses

4.8. Interrupt Interface

The TC358867XBG Bridge Chip uses INT to communicate internal events to the host.

The general purpose interrupt can internally be triggered independently by many different sources as explained in the Interrupt Control General Register INTCTL_G. This interrupt is asserted active high to the Host. The interrupt output stays active till the corresponding source bit is cleared in the Interrupt Status Register General INTSTS_G by writing a '1' to the bit. The status of this interrupt is provided in the Interrupt Status General Register INTSTS_G.

4.8.1. Interrupt Assertion

When the condition for one of the sources of the interrupt (enabled in the INTCTL_G register) has been met, it will cause the corresponding bit in the INTSTS_G register to be set and cause an interrupt to be generated on the interrupt line. The Host should react to each interrupt assertion as described in the next section.

4.8.1.1. GPIO0 & GPIO1 Based Interrupt Assertion

GPIO0 & GPIO1 based interrupt sources are a little different from other interrupt sources. If any of these interrupt sources is used as the source of the interrupt, any change in the value of the signal can trigger an interrupt. One interrupt is generated if the GPIO signal goes from low to high. Another interrupt is generated if the GPIO signal goes from high to low and stays low for more than a predetermined period (Interrupt GPIO Low Count register programmed by Host). Such functionality can be used to support DisplayPort™ HPD handling, etc.

4.8.2. Interrupt Handling

The host should first disable all the interrupts by writing "0" to the INTCTL_G register. The host should then read the interrupt status register general INTSTS_G to identify the cause of the interrupt. Once the cause of interrupt has been identified and handled, the host should clear the interrupt by writing to the INTSTS_G register.

The Host can enable the interrupt sources again by setting appropriate bits in the INTCTL_G register.

4.9. Internal Test Pattern (Color Bar) Generator

The TC358867XBG Bridge Chip incorporates an internal test pattern (color bar) generator in the chip that can be configured by the Host (through register accesses).

The test pattern generator does not need any input video stream from DSI or DPI host.

The following features are supported:

- Color bar or solid pattern.
- Default size of 640 x 480.
- Output configuration selectable as single or dual lane DisplayPort™.
- DSI/DPI Rx logic bypassed in this test pattern mode.

The test pattern generator's output mode is controlled by the TC358867XBG Test Control register.

For solid color mode:

- The R, G & B color component values mentioned in the test control register decide the final color value.

For vertical color bar mode, the order of color bars is (from left to right):

- Blue, Black, White, Yellow, Cyan, Green, Magenta, Red
- Width of each color bar is 1/8th of total horizontal width of frame.
- Width of last bar (red) is adjusted for any remainder from frame width division by 8.

For checker board mode, the order of color blocks is:

- From Left to Right: Blue, Black, White, Yellow, Cyan, Green, Magenta, Red and repeating in that order.
- From Top to Bottom: Blue, Black, White, Yellow, Cyan, Green, Magenta, Red and repeating in that order.
- Each color block is 64 pixels by 64 pixels size.
- Width & height of last block is adjusted for remaining frame width/height.

4.10. HDCP Support (Optional)

TC358867XBG supports HDCP version 1.3 amendment for DisplayPort™ revision 1.1 content protection. TC358867XBG supports Single Stream Transfer mode only. It does not support HDCP repeater functionality either.

1. Host enables HDCP block by enabling HDCPENB register bit in SYSRSTENB register.
2. TC358867XBG waits for the assertion of HDCPCTRL[Auth] bit by host before starting HDCP block. When HDCPCTRL[Auth] bit is set, TC358867XBG performs authentication autonomously, without host intervention.
3. HDCP Status register, HDCPSTAT, is provided for Host to monitor the status.
4. Host can issue (re)authentication command any time by setting register bit HDCPCTRL[Auth].
5. Host is responsible to check the revocation list to validate/invalidate received BKS value, once it is fetched from HDCP Rx by TC358867XBG. The availability of BKS is indicated in register bit HDCPSTAT[BKSRCV].
6. When link integrity fails, DP panel should interrupt TC358867XBG which will pass the interrupt to Host to read DP panel's interrupt status and determine what to do. Host can set TC358867XBG's HDCP block to Reset, Link Fail or Re-Authentication state by de-asserting bit ENBHDPC in SYSRSTENB register or asserting LinkFail or Auth bits in HDCPCTRL register, respectively.
7. TC358867XBG provides register ANSEED[39:0] for host to be used as the seed value to generate a random number AN[39:0].
8. For debug purpose, Rx R0, AKSV and BKS values are readable by Host.

4.10.1. HDCP encryption modules (Optional)

There are two independent HDCP modules – one for each of the DisplayPort™ ports. These are enabled/disabled by corresponding bits in the SYSRSTENB register. They share the HDCP key stored in the eFUSES.

4.11. Reset

The internal reset structure is given in Figure 4.17 below.

The external HW reset passes a reset cancellation circuit that cancels an active reset unless it is active longer than a predefined period.

The filtered HW reset and the internal SW reset are combined and distributed to the sub modules inside TC358867XBG.

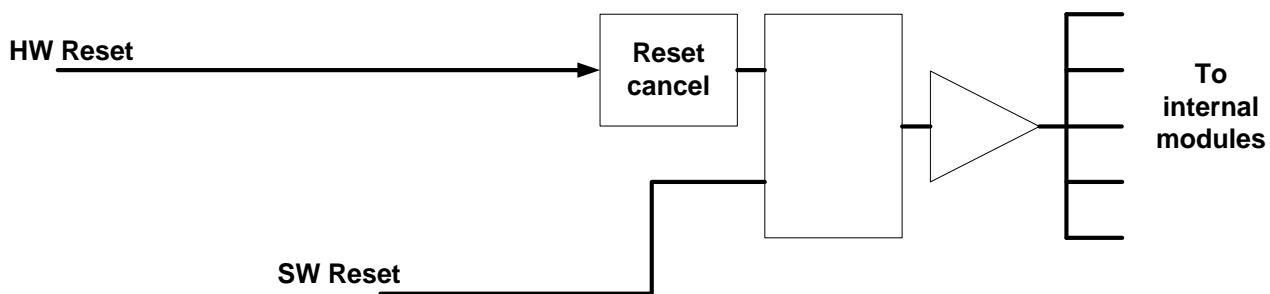


Figure 4.17 Reset System

4.12. Boot-Strap & State of TC358867XBG chip after Reset

After reset, the PLL is bypassed and the analog PHYs are in an idle state. The I²C block receives the PLL_REF clock directly (without going through the PLL) and so are active after reset. Based on the mode of the chip, the states of the different blocks are discussed below:

4.12.1. MODE[0]: Clock Source Selection

Depending upon the MODE selection, whichever clock source is used for PLL_REF clock, that clock source is required to be continuously clocking at a constant rate for guaranteed operation of the chip. MODE[0] is used to select the clock source for PLL input clock PLL_REF.

MODE[0]:

- 0: Selects external RefClk as the source of PLL input clock PLL_REF.
- 1: If REFCLK = 0, Selects clock from DSI as source of PLL input clock PLL_REF
If REFCLK = 1, Selects DPI PCLK as the source of PLL input clock PLL_REF.

4.12.2. MODE[1]: DSI Reference Clock Source Division Selection

Refer clock structure diagram in clocks chapter for further clarification of this selection. These bits are don't care if external RefClk or DPI PCLK is used as RefClk for PLLs.

MODE[1]:

- 0: HSCKBY2 divided by 7 used as DSI RefClk for PLLs (HSCK assumed = 364 MHz).
- 1: HSCKBY2 divided by 9 used as DSI RefClk for PLLs (HSCK assumed = 468 MHz).

4.12.3. I²C Slave Address Selection

I²C_ADR_SEL pin is used to select the I²C slave address:

I²C_ADR_SEL:

- 0: I²C slave device address for TC358867XBG chip is 0x68 ("1101 000").
- 1: I²C slave device address for TC358867XBG chip is 0x0F ("0001 111").

4.12.4. Miscellaneous

The DSI Rx PHY (D-PHY) is in LP mode after reset.

The DP PHY Main Channel and the AUX Channel PHYs are in powered down state unless enabled by asserting PHY_EN after reset.

All registers have their default values after reset (except the GPIO Input Status Register).

PLLs are in bypass mode.

All other digital blocks are in reset state.

4.13. Clocks

The TC358867XBG uses up to three PLLs. One PLL each (called DP_PLL) is associated with each DisplayPort™ port and is used to generate most of the clocks in the chip. If both DisplayPort™ ports use same link frequency, then one PLL is shared by both. One PLL (called Pixel_PLL) is used to generate internal pixel clock.

PLLD_REF & PLLP_REF are the input clocks for the DP_PLLs and Pixel_PLL respectively. The PLLD_REF source is selectable based on boot-strap option while the PLLP_REF source is selectable based on a register programming.

The possible sources for PLLD_REF & PLLP_REF are:

- REFCLK input from external clock source at 13, 26, 19.2 or 38.4 MHz.
- Clock extracted from DSI interface – a divided down DSICLK.

The following restrictions apply to the PLLD_REF clock source irrespective of what the source is:

- PLLD_REF should be 13, 26, 19.2 or 38.4 MHz.
- PLL_REF phase jitter peak-to-peak should be less than 50 ps.
- PLL_REF duty cycle can be up to 40 - 60%.
 - Preferred duty cycle is 50% though.
- PLL_REF has to be always clocking to provide clock sources for:
 - SYSCLK (derived from DP Tx PLL or same as PLL_REF if PLL is bypassed)
 - I²C block, Register module (& BM module) (receives SYSCLK)
 - PLLs to lock properly

The DSICLK clock source can be HSCK or HSCKBY2 or HSCKBY4 output from the DSI Clock Lane PHY. If the DSICLK is used as source for PLL_REF, then the DSICLK has to be continuously clocking in HS mode even when DisplayPort™ transmissions are not in progress. As the clock derived from the DSICLK has to be fixed at 13, 26, 19.2 or 38.4 MHz, the DSI Host may need to run DSI clock lane at higher frequency than needed by frame rate and may have to send the DSI video mode transmissions in burst mode (explained in DSI section of this specification).

The DSICLK or the REFCLK (depending on reference chosen) can be divided down to achieve required frequency of 13, 26, 19.2 or 38.4 MHz using the pre-dividers (refer clock registers). Default value of pre-divider is “divide_by_1”.

The video data is transferred to the video buffer at an average rate based on HSByteClk in DSI Rx case (= HSByteClk * 8 * Num_DSI_Lanes / BPP) or at the DPI_PCLK rate (in DPI Rx case).

The video data from the video buffer FIFO is read by the DP transmit controller using the STRMCLK, which is derived from the DPI_PCLK (in DPI Rx case) or Pixel_PLL (in DSI Rx case) and closely approximated to the input PCLK.

The video data is framed as per DP protocol and sent to the DP PHY by the DP Tx controller synchronous to LSCLK (= DP TxClk / 10) derived from DP_PLL (PLL0 or PLL1) output.

The TC358867XBG chip transmits video out to DP link at DP Tx clock rate (1.62 or 2.7 Gbps). This DP Tx clock is generated by the DP_PLL (PLL0 or PLL1).

For I2S module, the LRCLK (audio sample clock) and the BCLK (audio bit clock) are input from the Host and are used by the I2S Rx to extract audio data from input audio stream. The audio data is written to the audio buffer using BCLK and read out by the DP transmitter using LSCLK.

The SYSCLK, which is derived from the DSI HSByteClk or the DP_PLL output, is used to clock the register module, the I²C and BM modules as well as some portion of the DSI Rx module.

Clocks extracted from the DP_PLL output are summarized below:

- DisplayPortTM PHY Main link clock.
- DisplayPortTM AUX channel clock.
- LSCLK: The link symbol clock used by the digital portion of the DisplayPortTM Tx.
- SYSCLK

Clocks extracted from the Pixel_PLL output are summarized below:

- STRMCLK (or the internal Pixel clock): The approximated pixel clock used for reading DSI video data from the Video buffer FIFO before stuffing and framing for the DP PHY in DSI Rx case.

Depending on the source of video stream being used and the clock used as PLL_REF source, there can be further differences in relationship of internal clocks and are summarized below.

Table 4.4 TC358867XBG clocks relationships in different Modes

Video Source	MODE0 pin	PLL_REF	SYSCLK	Video Buffer Write Clock	Video Buffer Read Clock (STRMCLK)	LSCLK
DSI	0	RefClk	DP_PLL / x (\geq HSByteClk)	SYSCLK	Pixel_PLL / y (\approx DSI_PCLK)	PLL / 10
	1	DSICLK	HSByteClk	SYSCLK	Pixel_PLL / y (\approx DSI_PCLK)	PLL / 10
DPI	0	RefClk	DP_PLL / x (\geq 14 MHz) ^{Note1}	DPI_PCLK	DPI_PCLK	PLL / 10

Note1: SYSCLK is used for Register accesses.

Following diagram illustrates the clock source to the internal functional blocks of the chip.

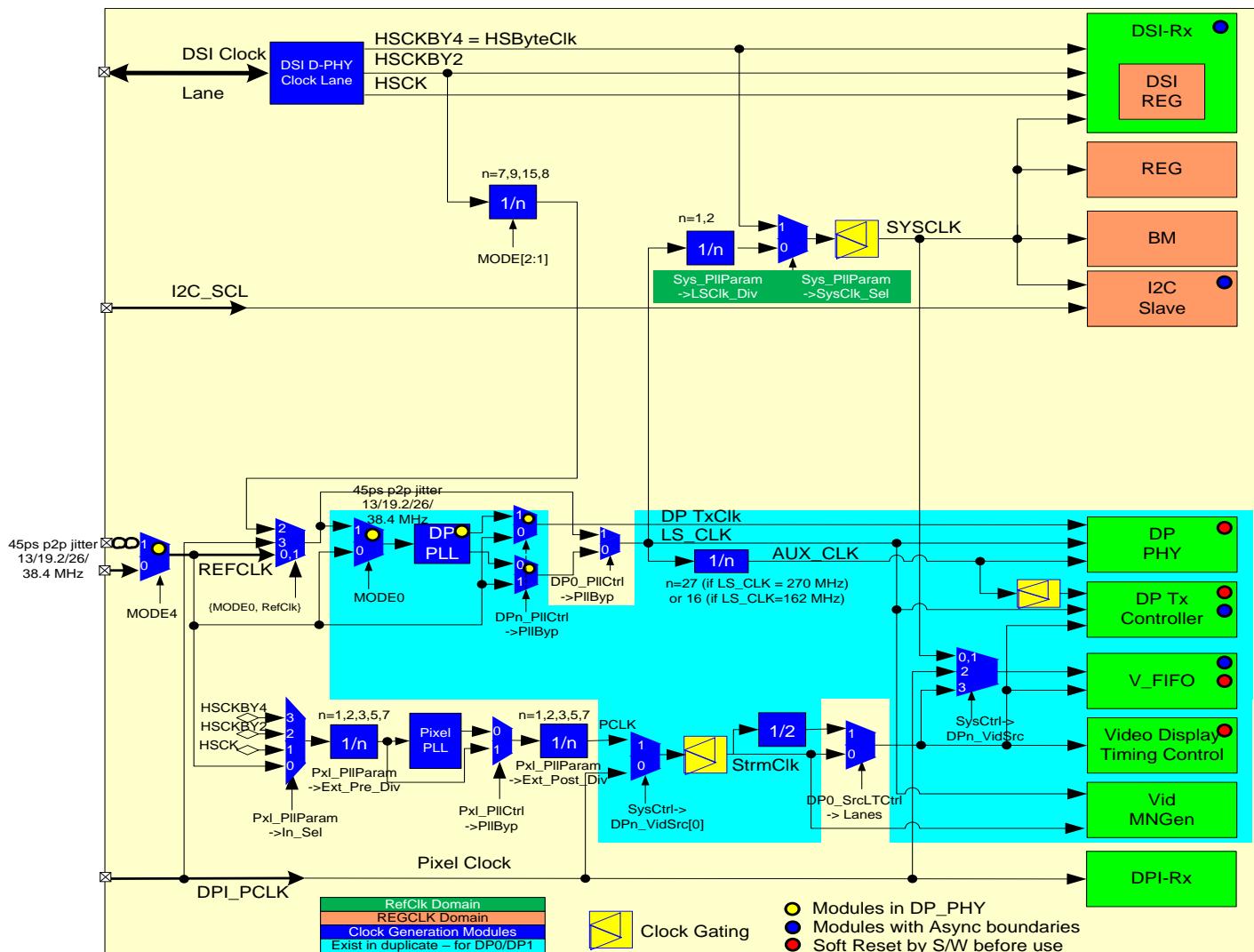


Figure 4.18 Clock Mode Selection and Clock Sources

4.13.1. Updating PLL parameters

On reset, the PLL is in bypass mode. The PLL parameter values in PLL control registers can be changed at any time, but they can be affected only when the PLL is disabled (in bypass mode) as described below.

- Make sure TC358867XBG is not transmitting any video/audio data (Required TC358867XBG modules disabled by writing to SYS Reset_Enable Register).
- Program updated PLL parameters in appropriate TC358867XBG registers.
- Disable appropriate PLL by writing '0' to the "PLLEn" bit in the appropriate PLLCtl register.
- Copy PLL parameters from PLL shadow registers in TC358867XBG register space to current PLL parameters register in PLL control block using PLL_REF by writing to the "Pllupdate" bit in the PLLCtl register.

- e) Enable appropriate PLL by writing ‘1’ to the “PLLEn” bit in the appropriate PLLCtl register.
- f) All clocks from CG are enabled after LOCKDET (frequency lock detect true signal from PLL) is asserted.
- g) Enable the appropriate modules by writing to the SYS Reset_Enable Register. In case any of the DP_PLL parameters are changed, a proper DP link initialization followed by link training sequence is required as described in the DisplayPort™ Link Establishment section.

The timing diagram of this mechanism is shown in figure below.

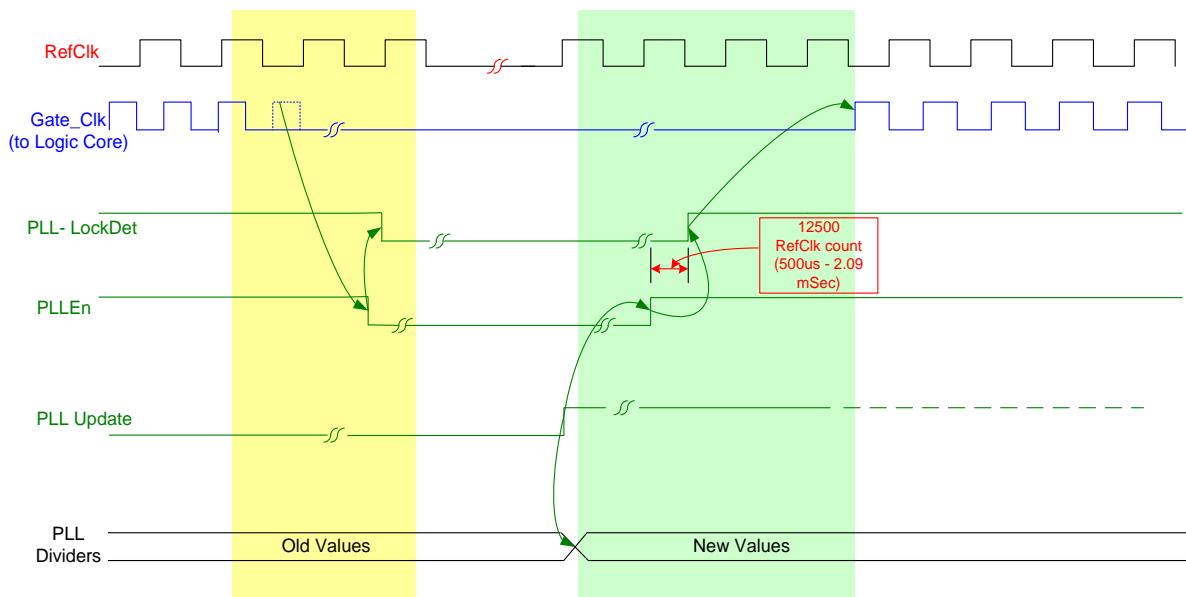


Figure 4.19 Timing diagram for updating PLL parameters

4.13.2. Down-spreading of Link Frequency (Spread Spectrum)

Down-spreading of the Link frequency (with modulation frequencies of 30 kHz to 33 kHz) is suggested by DisplayPort™ specification to reduce EMI as an optional feature for the DisplayPort™ transmitter.

TC358867XBG bridge chip provides for a programmable Spread Spectrum logic working with DisplayPort™ Tx PLL. This Spread Spectrum logic can be turned On/Off through register interface.

4.14. Power on/off Procedure

The following sequence should happen before TC358867XBG Bridge Chip is able to operate properly:

1. Provide voltage and clock sources to TC358867XBG Chip. For voltage source, it is desired to turn on core power (1.2) source first, then Analog PHY and IO (1.8V) power as shown in the figure below. The timing parameters are tabulated below.
 - o Boot-strap options shall be chosen based on the mode of operation desired.
 - o PLL_REF clock source should be turned on at least for the duration of t_{RSTW} before releasing RESX. (If Boot_Strip options are chosen such that DSI clock is to be used for PLL_REF, then the DSI Clock Lane should be turned on at this time for sufficient period as required by the interface specifications to ensure stable clock for PLL_REF).
 - o TEST signal needs to be driven low all the time.
2. Slave I²C block is ready after reset for accepting commands and for TC358867XBG register accesses.

TC358867XBG registers can be programmed at this point.

Next step is to program the TC358867XBG registers as per the mode of operation desired.

3. Host writes to the appropriate PLL control registers to enable the PLL and waits for PLL lock time before accessing the Bridge chip again (PLLs are required to ensure that internal sampling clock is stable) and DisplayPortTM PHY is getting the link clock.
4. Host reads the EDID / DPCD registers from the DisplayPortTM display device using the AUX channel to get the Display Panel capabilities.
5. Host enables the DP PHY by writing to the DP_PHY_Ctrl register and waits for the DP PHY to be enabled.
6. Host writes to DPx_SrcCtrl register (as per the information in EDID / DPCD registers) to enable link training on the DP link using the Aux channel (required by DisplayPortTM specification) and waits for the link training to be completed successfully.
7. Assuming successful link training, Host configures the TC358867XBG remaining registers based on the results of link training and according to the mode of operation desired (DSI input / DPI input mode, etc.).
 - o Based on the maximum lanes and speed supported by DisplayPortTM link and the required frame rate of video transmission, the DisplayPortTM transmit and LCD controller registers need to be programmed by the Host.
 - o If the DSI interface is used as source of video stream, then the DSI Rx control registers need to be programmed appropriately.
 - o If the DPI interface is used as source of video stream, then the DPI Rx control registers (mainly the Input Video format) need to be programmed appropriately.
 - o If Audio transmission is also required, then the Audio control registers also need to be programmed as per the available bandwidth, number of audio channels, audio sampling rate, etc.
 - o Another key programming required is the mode method of I²C commands translation onto the DisplayPortTM AUX channel.
8. Host starts transmitting video on DSI / DPI interface as per the desired mode of operation.

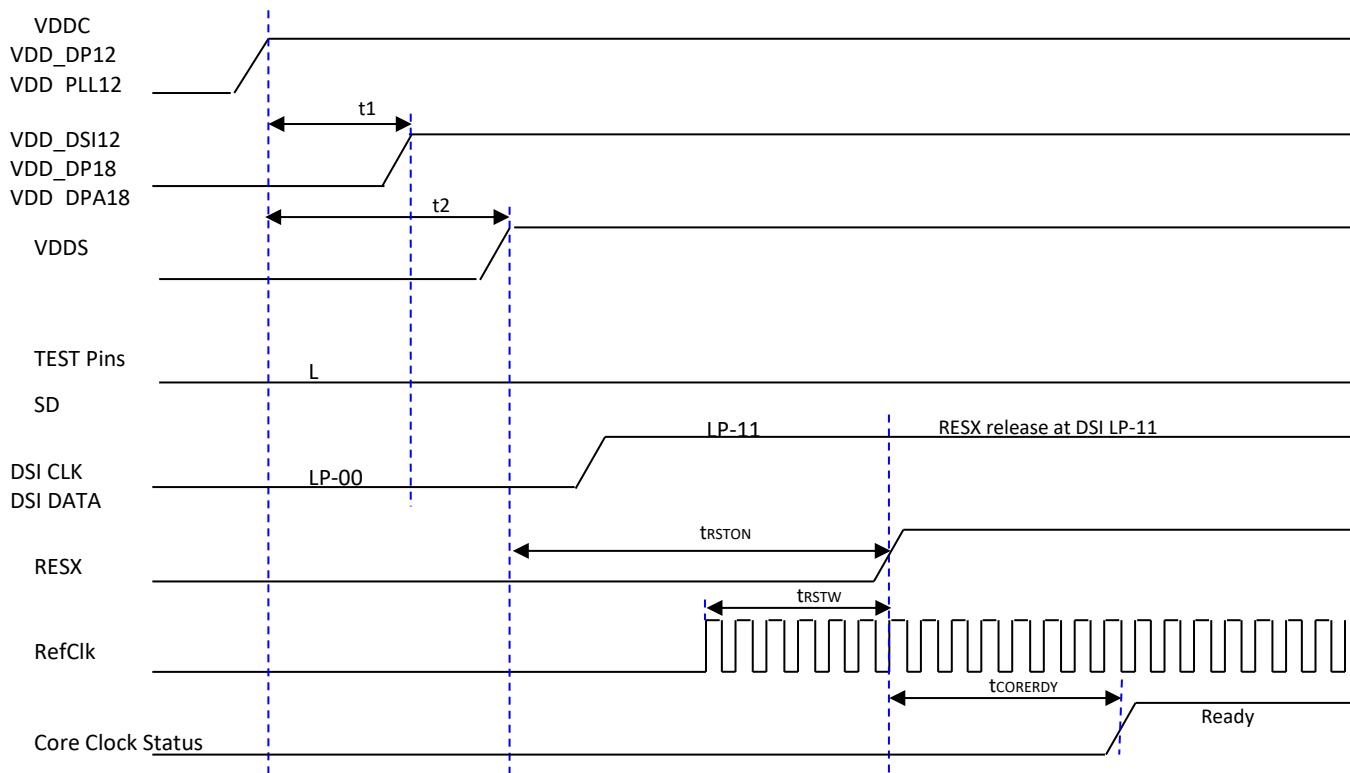


Figure 4.20 Power On Sequence

Table 4.5 Power On Sequence Timing

Parameter	Description	Min	Typ.	Max	Unit
RefClk	Reference clock frequency	13	---	38.4	MHz
t_1	VDD_DSI12 / VDD_DP18 / VDD_DPA18/VDD_PLL18 on delay from VDDC on	0	---	10	ms
t_2	VDDS on delay from VDDC on	0	---	10	ms
t_{RSTON}	RESET width period	2	---	---	μ s
t_{RSTW}	Period of Reset Signal	100	---	---	Cycle
$t_{CORERDY}$	Period after reset de-assertion when TC358867XBG clocks are stable (Dependent on RefClk frequency)	0.7	---	1	ms

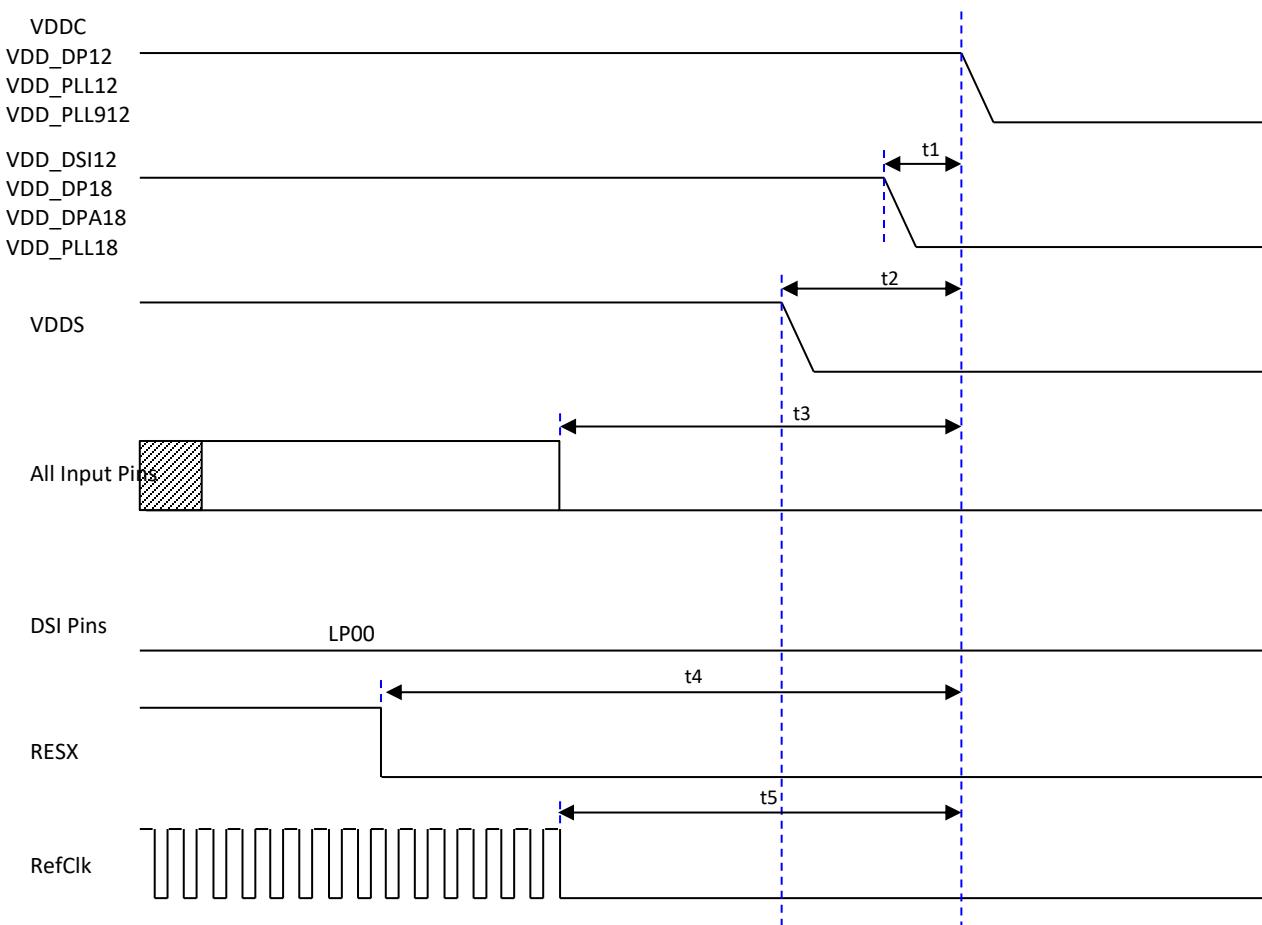


Figure 4.21 Power Off Sequence

Table 4.6 Power Off Sequence Timing

Parameter	Description	Min	Typ.	Max	Unit
t_1	VDD_DSI12 / VDD_DP18 / VDD_DPA18 / VDD_PLL18 off delay from VDDC off	0	---	10	ms
t_2	VDDS off delay from VDDC off	0	---	10	ms
t_3	All input pins turn low delay from VDDC off	t_2	---	10	ms
t_4	RESX assertion delay from VDDC off	10	---	---	ms
t_5	RefClk delay from VDDC off	t_2	---	10	ms

4.15. Register Accesses from Host

TC358867XBG provides following interfaces for register accesses from Host:

- I²C interface
- DSI Interface

The Host can use any of the two available interfaces.

Registers that can be accessed by the Host reside either in the TC358867XBG internal register space or in the DP Sink connected through DP Aux channel.

4.15.1. TC358867XBG register space accesses

Simple register accesses can be used to access the TC358867XBG internal registers. For most scenarios, all the registers in the TC358867XBG register space can be treated in a similar way, but for certain scenarios, some register accesses require special handling from certain register access interfaces as explained below.

4.15.1.1. TC358867XBG register accesses from DSI

For Host to access TC358867XBG registers through DSI interface, the DSI access clock should be slower than TC358867XBG SYSCLK by at least a factor of ½. During PLL On mode, this condition is met implicitly. During the initialization phase, (PLL Off mode), the SYSCLK is based on the RefClk (13, 19.2, 26 or 38.4 MHz). So, during PLL Off mode, the DSI access clock should be slowed down accordingly.

4.15.1.1.1. Sys_PliParam register update access from DSI

Writes to the Sys_PliParam register result in the SYSCLK / ClkGen parameters updates and this causes the SYSCLK to be stopped for few clocks. For this reason, writes to the Sys_PliParam register should be last packet in a sequence of DSI packets. Any packets followed immediately after the write to Sys_PliParam register might result in CRC errors, in which case, these errors should be ignored by the host.

4.15.1.2. DP PHY internal register space accesses

Accesses to the DP PHY internal register address space are done using the DP_PHY_CFG_WR and DP_PHY_CFG_RD registers.

Writes are accomplished by writing the register address and data to the appropriate bits of the DP_PHY_CFG_WR register.

Reads are accomplished by writing the register address to the appropriate bits of the DP_PHY_CFG_RD register followed by a read to the DP_PHY_CFG_RD register to read the data from the appropriate bits in the register.

These registers can be accessed from any host register interface.

4.15.2. DP Sink register space accesses

Accesses from TC358867XBG Host can be at a high frequency clock (DSI clock) or at a low frequency clock (I²C clock). The accesses to the DP Sink registers through the TC358867XBG registers will always be at the DP Aux channel data rate of 1 Mbps.

For writes to DP Sink, this is not an issue as the writes are posted (in the TC358867XBG Aux control registers).

For reads to the DP Sink, this means the Host might have to wait for many cycles before getting the read data back from the DP Sink. To allow for this data rate difference, the Host must always monitor the “Busy” bit in the AUXSTATUS register before reading the read data back from the DP_x_AuxRData0 – DP_x_AuxRData3 registers.

Either “native Aux” accesses or “I²C over Aux – Indirect” or “I²C over Aux – Direct” accesses can be used to access registers in the DP sink as explained below.

4.15.2.1. Native Aux access

“Native Aux” accesses can be initiated by any of the three TC358867XBG host register interfaces by accessing the DP_AuxAddr, DP_x_AuxWData0-3 and DP_x_AuxRData0-3 registers as explained below.

4.15.2.1.1. Register Write

“Native Aux” write accesses can be generated by setting the register address in the DP_AuxAddr register and the write data in the DP_AuxWData0 to DP_AuxWData3 registers. After this, a write to the DP_AuxCfg0 register to set the “native write” command and burst size, shall start a native aux write transaction on the DP Aux channel.

4.15.2.1.2. Register Read

“Native Aux” read accesses can be generated by setting the register address in the DP_AuxAddr register and setting the “native read” command and burst size in the DP_AuxCfg0 register. After this, once the “busy” bit is de-asserted in the DP_AuxStatus register, the read data is accessible in the DP_x_AuxRData0 to DP_x_AuxRData3 registers and can be read out.

4.15.2.2. I²C Aux access

“I²C Aux accesses – indirect” can be initiated by any of the three TC358867XBG host register interfaces by accessing the DP_x_AuxAddr, DP_x_AuxWData0-3 and DP_x_AuxRData0-3 registers as explained below.

4.15.2.2.1. Register Write through TC358867XBG register access

“I²C over Aux” write accesses can be generated by setting the register address in the DPx_AuxAddr register and the write data in the DPx_AuxWData0 to DPx_AuxWData3 registers. After this, a write to the DPx_AuxCfg0 register to set the “I²C write” command and burst size, shall start a “I²C over aux” write transaction on the DP Aux channel. In case a longer write burst needs to be done, then the “I²C write (middle of transaction)” command should be used instead.

4.15.2.2.2. Register Read through TC358867XBG register access

“I²C over Aux” read accesses can be generated by setting the register address in the DPx_AuxAddr register. After this, a write to the DPx_AuxCfg0 register to set the “I²C write (middle of transaction)” command, burst size and “address only”, shall start a “I²C over aux” write transaction on the DP Aux channel. This should be followed by a write to the DPx_AuxCfg0 register to set the “I²C read” command and burst size which shall start a “I²C over aux” read transaction on the DP Aux channel. The Host should monitor the Busy bit in the AUXSTATUS register before reading the read data back from the DPx_AuxRData0 – DPx_AuxRData3 registers. In case a longer read burst needs to be done, then the “I²C read (middle of transaction)” command should be used instead of “I²C read” command.

4.16. Video Transmission over DP link

This section briefly describes how the video data received from the DSI or DPI receiver is transmitted to display panels using the DP Tx (DisplayPort™ transmitter). The audio data received over the I2S interface is also multiplexed into the DP frame during the horizontal and vertical blanking periods.

The possible scenarios are discussed below.

4.16.1. DSI to DisplayPort™ Tx

In case of DSI interface used as the source of video stream, the programming/selections that need to be done are:

- DP output port(s) used as single lane or dual lane port.
- Audio input enabled or not
- Register access mechanism from DSI or I²C.
- PLL_REF clock source from external RefClk or clock extracted from DSI interface.

The data path for DSI to DP video transfer is:

DSI Host -> D-PHY -> DSI Rx -> Video buffer -> DP Digital Controller -> DP PHY -> DP Display Panel

The control path for DSI to DP video transfer is:

DSI Host -> D-PHY -> DSI Rx -> TimingGen (LCDC) -> DP Digital Controller -> DP PHY -> DP Display Panel

4.16.2. DPI to DisplayPort™ Tx

In case of DPI interface as source of video stream, programming that needs to be done are:

- DP output port(s) used as single lane or dual lane port.
- Audio input enabled or not
- Register access mechanism I²C.
- PLL_REF clock source from external RefClk or pixel clock from DPI interface.

The data path for DPI to DP video transfer is:

DPI Host -> DPI Rx -> Video buffer -> DP Digital Controller -> DP PHY -> DP Display Panel

The control path for DPI to DP video transfer is:

DPI Host -> DPI Rx -> TimingGen (LCDC) -> DP Digital Controller -> DP PHY -> DP Display Panel

4.16.3. Pixel Format Translation

As discussed earlier, the TC358867XBG chip can receive video data from Host in one of the following formats:

- 16-bit RGB565
- 18-bit RGB666 (Packed)
- 24-bit RGB666 (Loosely Packed)
- 24-bit RGB888
- 16-bit YCbCr422

Pixel data are always stored in the video line buffer as 24-bit. When lower BPP formats are received, each color component will be padded with 0 in its LSB bit position.

The following pixel translation paths are supported between the received and transmitted video formats:

Table 4.7 Pixel Translation Paths

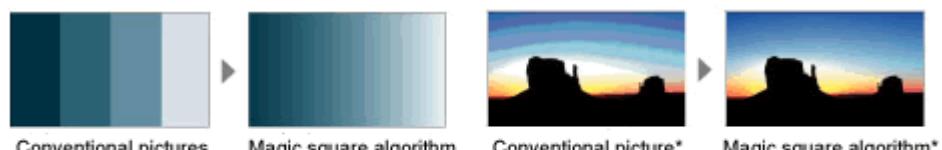
Received Pixel Format	Re-transmitted Pixel Format
16-bit RGB565	24-bit RGB888
	18-bit RGB666
18-bit RGB666 (Packed)	18-bit RGB666
24-bit RGB666 (Loosely Packed)	18-bit RGB666
24-bit RGB888	24-bit RGB888
	18-bit RGB666
16-bit YCbCr	16-bit YCbCr

4.16.4. Magic Square Algorithm

When the display panel's color depth capability is less than that of the input data, say sending RGB888 data to 18-bit display panel, the number of bits of display need to be reduced. With the Toshiba Magic Square algorithm, an RGB666 18-bit LCD panel can produce a display quality equivalent to that of an RGB888 24-bit LCD panel.

For example, when Magic Square algorithm is enabled the red component of the RGB666 output becomes either "R [7:2]" or "R [7:2] + 1". The ratio of these two values depends on the horizontal and vertical position and the display timing. With this changing pixel value, human eye senses the red color component as "R [7:2]", "R [7:2] + 0.25", "R [7:2] + 0.5" and "R [7:2] + 0.75". Therefore, the color depth for the human eye becomes almost those of RGB888 data.

By employing Toshiba's Magic Square algorithm the color graduation is increased significantly compared to 18-bit RGB666 data. The following figure shows 2 conceptual examples of the effect from the Magic Square algorithm.



Compared with our own models.

Photos marked with a mark "*" show conceptual images that illustrate the effect.

Figure 4.22 Magic Square Algorithm Effect

4.16.5. TC358867XBG transfer paths

Following table summarizes the different video data/control paths allowed from possible video inputs to the DisplayPort™ output and the use of key internal components in each possible path.

Table 4.8 TC358867XBG Video Transfer Paths

Case	Mode	I/P	DP_IP	DP_PHY	Monitor (# of DP lanes)	PLL	SYSCLK Source	VB Write Clock	Stream Clock
1	S21	DSI	IP0	PHY0	M0 (1L)	PLL0	PLL0/ HSByteClk	SYSCLK	Pixel PLL
2	S21	DSI	IP0	PHY0 + PHY1	M0 (2L)	PLL0	PLL0/ HSByteClk	SYSCLK	Pixel PLL
3	P21	DPI	IP0	PHY0	M0 (1L)	PLL0	PLL0	DPI_PCLK	DPI_PCLK
4	P21	DPI	IP0	PHY0 + PHY1	M0 (2L)	PLL0	PLL0	DPI_PCLK	DPI_PCLK

4.17. Power Management

The TC358867XBG chip operates under three general power states: Reset, ULPS, and Normal state. Transition between the three states, as illustrated in diagram below, is controlled by three mechanisms:

- Hardware reset (power-on reset and input pin RESX reset).
- ULPS trigger messages over the DSI link.

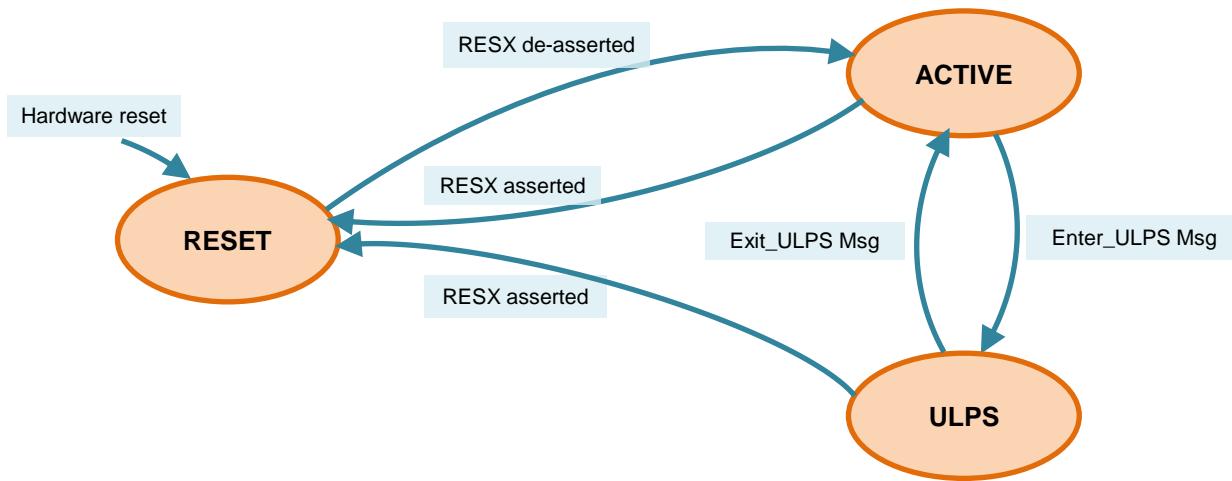


Figure 4.23 Power State Transition Diagram

4.17.1. Power State transitions

As can be seen from the diagram above, there are 6 possible power state transitions.

RESX assertion in any power state transitions the TC358867XBG into the “RESET” state.

The ULPS message transmission over the DSI link for forcing the TC358867XBG into the “ULPS” state should happen only in the DSI input mode. It is the responsibility of the Host to make sure of the state of the system before sending the ULPS message to TC358867XBG. If the ULPS message is used to enter the “ULPS” state, then a “ULPS-Exit” message should be used to exit the “ULPS” state.

The state of TC358867XBG registers does not change during the “ULPS” state and their values are maintained from the state before entering the “ULPS” state.

After transitioning from the “ULPS” to the “ACTIVE” state, the Host should wait for the PLLs to get locked before starting any video streaming.

Table below summarizes active state of major TC358867XBG components during three power states.

Table 4.9 Component Power State summary

State	I ² C	Reg & BM	DSI-PHY	DSI Rx Logic	DPI Rx	DP-PHY	PLL	Reg Values	FSM State
Off	X	X	X	X	X	X	X	X	X
RESET	Reset	Reset	LP mode	Reset	Reset	Idle	Disabled	Reset	Reset
ULPS	Use PII_Ref (& I2C_SCL)	Use PII_Ref	LP mode	Used for DSI-specific register accesses	Idle	Idle	Disabled	Maintain value; inaccessible	Reset
ACTIVE	* Use SYSCLK	Use PII_Ref	* Active (LP/HS)	* Active	* Active	* Active	Active	Host accessible	Active state

* Depends on mode of operation – I²C based register access; DSI or DPI input mode.

5. RegFile Block (Reg)

The Host accesses TC358867XBG RegFile block to read status and/or write control registers through the DSI or I²C slave function. I²C slave functions interface to RegFile block through a simple register interface that is documented in the sections below. The DSI Rx interface also interfaces to the registers in response to certain DSI commands as described in the DSI Rx portion of this specification.

5.1. Register Map

The control and status registers in TC358867XBG are provided in table below.

5.1.1. Address Map Summary

Following table gives a summary of the address map in terms of main modules.

Table 5.1 Register Map

Address Offset	Pnemonic	Register Description
0x0000	DSI	DSI D-PHY
0x0100		DSI PPI
0x0200		DSI Protocol
0x0300		DSI General
0x0400		DSI Application
0x0440	DPI Rx	MIPI Display Parallel Interface
0x0448	Parallel Out	Parallel Output Interface
0x0450	Video Path	Path to DP Tx0
0x0480		Path to DP Tx1
0x0500	System	System Control & Status
0x0520	I ² C	I ² C Control & Status
0x0540	GPIO	GPIO Control & Status
0x0560	Interrupt	Interrupt Control & Status
0x0600	DisplayPort™	Control
0x0610		Clock
0x0640		DP0 - Main Channel
0x0660		DP0 – Aux Channel
0x06A0		DP0 – Link Training
0x0700		Audio
0x0800		DP PHY
0x0880	I2S	Audio I2S Receiver
0x0900	PLL	—
0x0980	HDCP	—
0x0A00	Test & Debug	—

5.1.2. Register Map

The control and status registers in TC358867XBG are provided in table below.

Table 5.2 Register Map

Address Offset	Pnemonic	R/W	Default	Register Description
DSI D-PHY Layer Registers				
0x0004	D0W_DPHYCONTX	R/W	0x0000_0002	Data Lane 0 D-PHY Tx Control register
0x0020	CLW_DPHYCONTRX	R/W	0x0000_A002	Clock Lane D-PHY Rx Control register
0x0024	D0W_DPHYCONTRX	R/W	0x0000_A002	Data Lane 0 D-PHY Rx Control register
0x0028	D1W_DPHYCONTRX	R/W	0x0000_A002	Data Lane 1 D-PHY Rx Control register
0x002C	D2W_DPHYCONTRX	R/W	0x0000_A002	Data Lane 2 D-PHY Rx Control register
0x0030	D3W_DPHYCONTRX	R/W	0x0000_A002	Data Lane 3 D-PHY Rx Control register
0x0038	COM_DPHYCONTRX	R/W	0x0000_0000	D-PHY Rx Common Control register
0x0040	CLW_CNTRL	R/W	0x0000_0000	Clock Lane Control register
0x0044	D0W_CNTRL	R/W	0x0000_0000	Data Lane 0 Control register
0x0048	D1W_CNTRL	R/W	0x0000_0000	Data Lane 1 Control register
0x004C	D2W_CNTRL	R/W	0x0000_0000	Data Lane 2 Control register
0x0050	D3W_CNTRL	R/W	0x0000_0000	Data Lane 3 Control register
0x0054	TESTMODE_CNTRL	R/W	0x0000_0000	Test Mode Control register
DSI PPI Layer Registers				
0x0104	PPI_STARTPPI	R/W	0x0000_0000	START control of PPI-RX function.
0x0108	PPI_BUSYPPI	RO	0x0000_0000	PPI busy status
0x0110	PPI_LINEINITCNT	R/W	0x0000_208E	Line Initialization Wait Counter
0x0114	PPI_LPTXTIMECNT	R/W	0x0000_0001	T _{LPX} period setting.
0x0134	PPI_LANEENABLE	R/W	0x0000_0003	PPI lane enable.
0x013C	PPI_TX_RX_TA	R/W	0x0008_0008	DSI Bus Turn Around timing parameters
0x0140	PPI_CLS_ATMR	R/W	0x0000_0000	LPRX analog timer test register for clock lane
0x0144	PPI_D0S_ATMR	R/W	0x0000_0000	LPRX analog timer test register for data lane 0
0x0148	PPI_D1S_ATMR	R/W	0x0000_0000	LPRX analog timer test register for data lane 1
0x014C	PPI_D2S_ATMR	R/W	0x0000_0000	LPRX analog timer test register for data lane 2
0x0150	PPI_D3S_ATMR	R/W	0x0000_0000	LPRX analog timer test register for data lane 3
0x0164	PPI_D0S_CLRSIPOCOUNT	R/W	0x0000_0019	PPI input mask period for data lane 0
0x0168	PPI_D1S_CLRSIPOCOUNT	R/W	0x0000_0019	PPI input mask period for data lane 1
0x016C	PPI_D2S_CLRSIPOCOUNT	R/W	0x0000_0019	PPI input mask period for data lane 2
0x0170	PPI_D3S_CLRSIPOCOUNT	R/W	0x0000_0019	DSI input mask period for data lane 3
0x0180	CLS_PRE	R/W	0x0000_X000	PPI PRE test register for clock lane
0x0184	D0S_PRE	R/W	0x0000_X000	PPI PRE test register for clock data lane 0
0x0188	D1S_PRE	R/W	0x0000_X000	PPI PRE test register for clock data lane 1
0x018C	D2S_PRE	R/W	0x0000_X000	PPI PRE test register for clock data lane 2
0x0190	D3S_PRE	R/W	0x0000_X000	PPI PRE test register for clock data lane 3
0x01A0	CLS_PREP	R/W	0x0000_X000	PPI PREP test register for clock lane
0x01A4	D0S_PREP	R/W	0x0000_X000	PPI PREP test register for data lane 0

Address Offset	Pnemonic	R/W	Default	Register Description
0x01A8	D1S_PREP	R/W	0x0000_X000	PPI PREP test register for data lane 1
0x01AC	D2S_PREP	R/W	0x0000_X000	PPI PREP test register for data lane 2
0x01B0	D3S_PREP	R/W	0x0000_X000	PPI PREP test register for data lane 3
0x01C0	CLS_ZERO	R/W	0x0000_X000	PPI ZERO test register for clock lane
0x01C4	D0S_ZERO	R/W	0x0000_X000	PPI ZERO test register for data lane 0
0x01C8	D1S_ZERO	R/W	0x0000_X000	PPI ZERO test register for data lane 1
0x01CC	D2S_ZERO	R/W	0x0000_X000	PPI ZERO test register for data lane 2
0x01D0	D3S_ZERO	R/W	0x0000_X000	PPI ZERO test register for data lane 3
0x01E0	PPI_CLRFLG	R/W	0x0000_0000	PPI CLRFLG test control
0x01E4	PPI_CLRSIPO	R/W	0x0000_0155	PPI CLRSIPO test control.
0x01F0	HSTIMEOUT	R/W	0x0000_0000	HS Rx Time Out Counter test register
0x01F4	HSTIMEOUTENABLE	R/W	0x0000_0000	Enable HS Rx Time Out Counter test register
DSI Protocol Layer Registers				
0x0204	DSI_STARTDSI	WO	--	START control bit of DSI-RX function
0x0208	DSI_BUSYDSI	RO	0x0000_0001	DSI busy status
0x0210	DSI_LANEENABLE	R/W	0x0000_0002	DSI lane enable
0x0214	DSI_LANESTATUS0	RO	0x0000_0000	DSI lane status 0
0x0218	DSI_LANESTATUS1	RO	--	DSI lane status 1
0x0220	DSI_INTSTATUS	RO	0x0000_0000	Interrupt Status
0x0224	DSI_INTMASK	R/W	0xF07F_AFFF	Interrupt Mask
0x0228	DSI_INTCLR	WO	0x0000_0000	Interrupt Clear
0x0230	DSI_LPTXTO	R/W	0xFFFF_FFFF	LPTX Time Out Counter
DSI General Registers				
0x0300	DSIERRCNT	R/W	0xC080_0000	DSI Error Count Register
DSI Application Layer Registers				
0x0400	APLCTRL	R/W	0x0000_0002	Application Layer Control Register
0x0404	RDPKTLN	R/W	0x0000_0003	DSI Read Packet Length Register
DPI Display Parallel Registers				
0x0440	DPIPIXLFMT	R/W	0x0000_0600	DPI Input Pixel Format Register
Parallel Output Registers				
0x0448	POCTRL	R/W	0x0000_0000	Parallel Output Control Register
Video Path0 Registers				
0x0450	VPCTRL0	R/W	0x0050_0000	Video Path Control Register
0x0454	HTIM01	R/W	0x0004_0008	Horizontal Timing Control Register 1
0x0458	HTIM02	R/W	0x0004_00A0	Horizontal Timing Control Register 2
0x045C	VTIM01	R/W	0x0008_0010	Vertical Timing Control Register 1
0x0460	VTIM02	R/W	0x0008_00F0	Vertical Timing Control Register 2
0x0464	VFUENO	R/W	0x0000_0000	Video Frame Timing Update Enable Register
System Registers				
0x0500	IDREG	RO	0x0000_660X	Chip ID and Revision ID
0x0504	SYSBOOT	RO	0x0000_00XX	System BootStrap Status Register
0x0508	SYSSTAT	RO	0x0000_0000	System Status Register

Address Offset	Pnemonic	R/W	Default	Register Description
0x050C	SYSRSTENB	R/W	0x0000_00FF	System Reset/Enable Register
0x0510	SYSCTRL	R/W	0x0000_0000	System Control Register
I²C Registers				
0x0520	I2CTIMCTRL	R/W	0x0000_0080	I ² C Timing Control Register
GPIO Registers				
0x0540	GPIOM	R/W	0x0000_0000	GPIO Mode Control Register
0x0544	GPIOC	R/W	0x0000_0000	GPIO Direction Control Register
0x0548	GPIOO	R/W	0x0000_0000	GPIO Output Register
0x054C	GPIOI	RO	0x0000_00XX	GPIO Input Register
Interrupt Registers				
0x0560	INTCTL_G	R/W	0x0000_0000	General Interrupts Control Register
0x0564	INTSTS_G	R/W	0x0000_0000	General Interrupts Status Register
0x0570	TEST_INT_C	R/W	0x0000_0000	Test Interrupts Control Register
0x0574	TEST_INT_S	R/W	0x0000_0000	Test Interrupts Status Register
0x0584	INT_GP0_LCNT	R/W	0x0001_3C68	Interrupt GPIO0 Low Count Value Register
0x0588	INT_GP1_LCNT	R/W	0x0001_3C68	Interrupt GPIO1 Low Count Value Register
DisplayPortTM Control Registers				
0x0600	DP0Ctl	R/W	0x0000_0040	DP0 Control Register
DisplayPortTM Clock Registers				
0x0610	DP0_VidMNGen0	R/W	0x000F_423F	DP0 Video Force M Value Register
0x0614	DP0_VidMNGen1	R/W	0x0062_1795	DP0 Video Force N Value Register
0x0618	DP0_VMNGenStatus	R/W	0xFFFF_FFFF	DP0 Video Current M Value Register
0x0628	DP0_AudMNGen0	R/W	0x0000_0000	DP0 Audio Force M Value Register
0x062C	DP0_AudMNGen1	R/W	0x0000_0000	DP0 Audio Force N Value Register
0x0630	DP0_AMNGenStatus	R/W	0x0000_0000	DP0 Audio Current M Value Register
DisplayPort0 Main Channel Registers				
0x0640	DP0_SecSample	R/W	0x000F_000F	DP0 Audio Sample Count Register
0x0644	DP0_VidSyncDelay	R/W	0x000F_000F	DP0 Video Sync Delay Register
0x0648	DP0_TotalVal Register	R/W	0x020D_0320	DP0 Total Frame Size Register
0x064C	DP0_StartVal	R/W	0x0023_0090	DP0 Active Line/Pixel Start Register
0x0650	DP0_ActiveVal	R/W	0x01E0_0280	DP0 Active Line/Pixel Count Register
0x0654	DP0_SyncVal	R/W	0x8002_8060	DP0 Sync Width Register
0x0658	DP0_Misc	R/W	0x0B3F_0000	DP0 Miscellaneous MSA Register
DisplayPort0 AUX Channel Registers				
0x0660	DP0_AuxCfg0	R/W	0x0000_0000	DP0 Aux Channel Config0 Register
0x0664	DP0_AuxCfg1	R/W	0x0001_0732	DP0 Aux Channel Config1 Register
0x0668	DP0_AuxAddr	R/W	0x0000_0000	DP0 Aux Access Address Register
0x066C	DP0_AuxWData0	R/W	0x0000_0000	DP0 Aux Write Data bytes 0 to 3
0x0670	DP0_AuxWData1	R/W	0x0000_0000	DP0 Aux Write Data bytes 4 to 7
0x0674	DP0_AuxWData2	R/W	0x0000_0000	DP0 Aux Write Data bytes 8 to 11
0x0678	DP0_AuxWData3	R/W	0x0000_0000	DP0 Aux Write Data bytes 12 to 15
0x067C	DP0_AuxRData0	R/W	0x0000_0000	DP0 Aux Read Data bytes 0 to 3

Address Offset	Pnemonic	R/W	Default	Register Description
0x0680	DP0_AuxRData1	R/W	0x0000_0000	DP0 Aux Read Data bytes 4 to 7
0x0684	DP0_AuxRData2	R/W	0x0000_0000	DP0 Aux Read Data bytes 8 to 11
0x0688	DP0_AuxRData3	R/W	0x0000_0000	DP0 Aux Read Data bytes 12 to 15
0x068C	DP0_AuxStatus	R/W	0x0000_0000	DP0 Aux Channel Access Status
0x0698	DP0_AuxI2CAdr	R/W	0x0000_0000	DP0 Aux Channel I ² C Address Register
DP0 Link Training Control & Status Registers				
0x06A0	DP0_SrcCtrl	R/W	0x0000_3080	DP0 Control Register
0x06D0	DP0_LTStat	RO	0x0000_2000	DP0 Link Training Status Register
0x06D4	DP0_SnkLTChgReq	RO	0x0000_0000	DP0 Sink Link Training Update Request
0x06D8	DP0_LTLoopCtrl	R/W	0x7500_0000	DP0 Link Training Loop Control Register
0x06E4	DP0_SnkLTCtrl	R/W	0x0000_0000	DP0 Link Training Config. for Sink address 0x00102
0x06E8	DP0_TPatDat0	R/W	0x0000_0000	DP0 Test Pattern bits 29 to 0
0x06EC	DP0_TPatDat1	R/W	0x0000_0000	DP0 Test Pattern bits 59 to 30
0x06F0	DP0_TPatDat2	R/W	0x0000_0000	DP0 Test Pattern bits 89 to 60
0x06F4	DP0_TPatDat3	R/W	0x0000_0000	DP0 Test Pattern bits 119 to 90
DisplayPort™ Audio Registers				
0x0700	AudCfg0	R/W	0x0000_0000	DP0 Audio Config0 Register
0x0704	AudCfg1	R/W	0x0000_0000	DP0 Audio Config1 Register
0x0708	AudIFData0	R/W	0x0000_0000	DP0 Audio Info Frame Bytes 3 to 0
0x070C	AudIFData1	R/W	0x0000_0000	DP0 Audio Info Frame Bytes 7 to 4
0x0710	AudIFData2	R/W	0x0000_0000	DP0 Audio Info Frame Bytes 11 to 8
0x0714	AudIFData3	R/W	0x0000_0000	DP0 Audio Info Frame Bytes 15 to 12
0x0718	AudIFData4	R/W	0x0000_0000	DP0 Audio Info Frame Bytes 19 to 16
0x071C	AudIFData5	R/W	0x0000_0000	DP0 Audio Info Frame Bytes 23 to 20
0x0720	AudIFData6	R/W	0x0000_0000	DP0 Audio Info Frame Bytes 27 to 24
DP1 Source Control Register				
0x07A0	DP1_SrcCtrl	R/W	0x0000_3000	DP1 Control Register
DisplayPort™ PHY Registers				
0x0800	DP_PHY_CTRL	R/W	0x030X_0000	DP PHY Control Register
0x0810	DP_PHY_CFG_WR	R/W	0x0000_0000	DP PHY Configuration Test Write Register
0x0814	DP_PHY_CFG_RD	R/W	0x0000_0000	DP PHY Configuration Test Read Register
0x0820	DP0_AUX_PHY_CTRL	R/W	0x0000_0001	DP0 AUX PHY Control Register
0x0840	DP0_MAIN_PHY_DBG	R/W	0x0000_0000	DP0 Main PHY Test Debug Register
I2S Registers				
0x0880	I2SCfg	R/W	0x0000_0000	I2S Audio Config0 Register
0x0888	I2SCH0Stat0	R/W	0x0000_0000	I2S Audio Channel0 Status Bytes 3 to 0
0x088C	I2SCH0Stat1	R/W	0x0000_0000	I2S Audio Channel0 Status Bytes 7 to 4
0x0890	I2SCH0Stat2	R/W	0x0000_0000	I2S Audio Channel0 Status Bytes 11 to 8
0x0894	I2SCH0Stat3	R/W	0x0000_0000	I2S Audio Channel0 Status Bytes 15 to 12
0x0898	I2SCH0Stat4	R/W	0x0000_0000	I2S Audio Channel0 Status Bytes 19 to 16
0x089C	I2SCH0Stat5	R/W	0x0000_0000	I2S Audio Channel0 Status Bytes 23 to 20

Address Offset	Pnemonic	R/W	Default	Register Description
0x08A0	I2SCH1Stat0	R/W	0x0000_0000	I2S Audio Channel1 Status Bytes 3 to 0
0x08A4	I2SCH1Stat1	R/W	0x0000_0000	I2S Audio Channel1 Status Bytes 7 to 4
0x08A8	I2SCH1Stat2	R/W	0x0000_0000	I2S Audio Channel1 Status Bytes 11 to 8
0x08AC	I2SCH1Stat3	R/W	0x0000_0000	I2S Audio Channel1 Status Bytes 15 to 12
0x08B0	I2SCH1Stat4	R/W	0x0000_0000	I2S Audio Channel1 Status Bytes 19 to 16
0x08B4	I2SCH1Stat5	R/W	0x0000_0000	I2S Audio Channel1 Status Bytes 23 to 20
PLL Control Registers				
0x0900	DP0_PLLCTRL	R/W	0x0000_0002	DP0 PLL Control register
0x0908	PXL_PLLCTRL	R/W	0x0000_0002	Pixel PLL Control register
0x0914	PXL_PLLPARAM	R/W	0x0033_041A	Pixel PLL Parameters register
0x0918	SYS_PLLPARAM	R/W	0x0000_0000	PLLs & SYSCLK input selection parameters register
HDCP Control Registers (Optional)				
0x0980	HDCP related register	R/W	0x0000_0002	-
0x0984	HDCP related register	R/W	0x0001_819D	-
0x0988	HDCP related register	R/W	0x0000_0000	-
0x098C	HDCP related register	R/W	0xA5A5_A5A5	-
0x0990	HDCP related register	R/W	0x0000_00A5	-
0x0994	HDCP related register	R/W	0x0000_0000	-
0x0998	HDCP related register	R/W	0x0000_0000	-
0x099C	HDCP related register	R/W	0x0000_0000	-
0x09A0	HDCP related register	R/W	0x0000_0000	-
0x09A4	HDCP related register	R/W	0x0000_0000	-
0x09A8	HDCP related register	R/W	0x0000_0000	-
0x09AC	HDCP related register	R/W	0x0000_0000	-
Test & Debug Registers				
0x0A00	TSTCTL	R/W	0xFFFF_FF10	TC358867XBG Test Control register
0x0A04	PLL_DBG	R/W	0x0000_0000	DP PLL Test Debug register

5.2. Register access protocol

I²C slave function follows a generic register access protocol when interfacing with regFile block. The following sections describe the protocol using I²C slave function accesses as an example.

5.2.1. Register Write

The I²C slave asserts the register address to be accessed on i2c_reg_addr and register write data on i2c_reg_wdata at the same cycle that i2c_reg_wr is asserted. Note that i2c_reg_wr is generated for 1 cg_reg_clk cycle. i2c_reg_addr and i2c_reg_wdata is driven 0 when i2c_reg_wr is de-asserted.

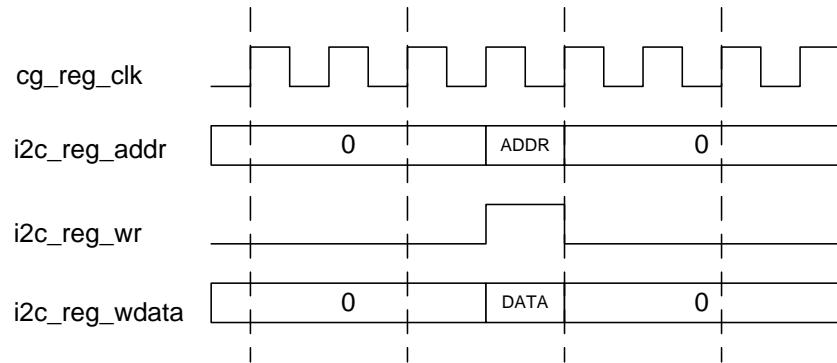


Figure 5.1 Register Write Access from I²C Slave

5.2.2. Register Read

The I²C slave asserts the register address to be accessed on i2c_reg_addr at the same cycle that i2c_reg_rd is asserted. Valid data is driven on i2c_reg_rdata one cg_reg_clk cycle after i2c_reg_rd is sampled asserted. Note that i2c_reg_rd is generated for 1 cg_reg_clk cycle. i2c_reg_addr is driven 0 when i2c_reg_rd and i2c_reg_wr are de-asserted.

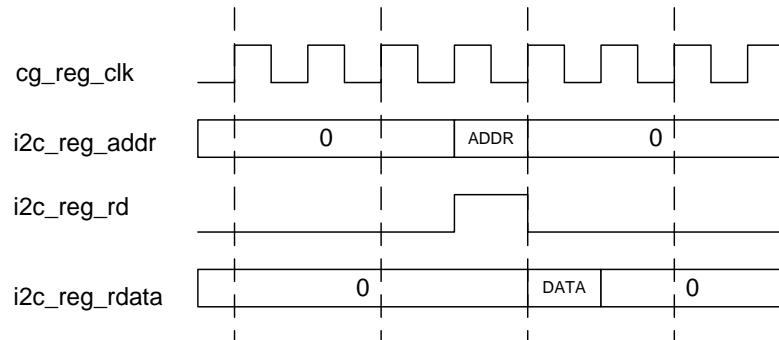


Figure 5.2 Register Read Access from I²C Slave

5.3. DSI Registers

5.3.1. DSI PHY Layer Registers

5.3.1.1. D0W_DPHYCONTX Register

Mnemonic	D0W_DPHYCONTX (Address = 0x0004)								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	---								
Default	0x00								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved						LPTXCURR1EN	LPTXCURR0EN	
Type	---						R/W	R/W	
Default	0x00						1	0	

Table 5.3 D0W_DPHYCONTX Register

Field Name	Bit	Description
Reserved	[31:2]	Reserved
D0W_LPTXCURR1EN	[1]	D0W_LPTXCURR1EN: Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 0.
D0W_LPTXCURR0EN	[0]	D0W_LPTXCURR0EN: Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 0.
00:	no additional output current	
01:	25% additional output current	
10:	25% additional output current	
11:	50% additional output current	
The Default value is “00”. Setting it to “00” makes rise/fall time longer, and setting to “11” makes it shorter.		

5.3.1.2. CLW_DPHYCONTRX Register

Mnemonic	CLW_DPHYCONTRX (Address = 0x0020)								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved	Reserved	HSRXTUNE1	HSRXTUNE0	Reserved	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	
Type	--	--	R/W	R/W	--	R/W	R/W	R/W	
Default	1	0	1	0	0	0	0	0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved	Reserved	Reserved	LPRXVTHLOW	Reserved	ATMREN	ATMR1	ATMR0	
Type	--	--	--	R/W	--	R/W	R/W	R/W	
Default	0	0	0	0	0	0	1	0	

Table 5.4 CLW_DPHYCONTRX Register

Field Name	Bit	Description
Reserved	[31:14]	Reserved
CLW_HSRXTUNE	[13:12]	CLW_HSRXTUNE [1:0]: Selection of HSRX bias resistance for Clock Lane. (TUNE1,TUNE0): = (00): 1.50k [Ohm] (TUNE1,TUNE0): = (01): 1.75k [Ohm] (TUNE1,TUNE0): = (10): 2.00k [Ohm] (Default) (TUNE1,TUNE0): = (11): 2.25k [Ohm]
Reserved	[11]	Reserved
CLW_DLYCNTRL	[10:8]	CLW_DLYCNTRL [2:0]: Skew control bits. Input/Output skew delayed by ~ 2^(DLYCNTRL-1) x 20ps for Clock Lane in HSRX. 3'b000: (Temporary Default)
Reserved	[7:5]	Reserved
CLW_LPRXVTHLOW	[4]	CLW_LPRXVTHLOW: LPRX input threshold select for Clock Lane. 1: LPRX input threshold is low 0: LPRX input threshold is high (Temporary Default)
Reserved	[3]	Reserved
CLW_ATMREN	[2]	CLW_ATMREN: Analog timer function enable for Clock Lane in HSRX. 0: analog timer function off (Default) 1: analog timer function on This bit is valid only in TESTMODE = 1. When TESTMODE = 0, this bit can be written or read but it does not affect any function.
CLW_ATMR	[1:0]	CLW_ATMR [1:0]: Selection of different delay times for tuning of Analog Timer for Clock Lane in HSRX. (ATMR1, ATMR0) = (0,0): Bypass mode (ATMR1, ATMR0) = (0,1): delay = D1 (ATMR1, ATMR0) = (1,0): delay = D2 (Default) (ATMR1, ATMR0) = (1,1): delay = D3

Note: In the description for DSI-RX related registers, TESTMODE and TESTMODEREGEN refers to the chip internal test mode signals, and should be treated as for internal test purpose only.

5.3.1.3. D0W_DPHYCONTRX Register

Mnemonic	D0W_DPHYCONTRX (Address = 0x0024)								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved	Reserved	HSRXTUNE1	HSRXTUNE0	Reserved	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	
Type	--	--	R/W	R/W	--	R/W	R/W	R/W	
Default	1	0	1	0	0	0	0	0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved	Reserved	Reserved	LPRXVTHLOW	Reserved	ATMREN	ATMR1	ATMR0	
Type	--	--	--	R/W	--	R/W	R/W	R/W	
Default	0	0	0	0	0	0	1	0	

Table 5.5 D0W_DPHYCONTRX Register

Field Name	Bit	Description
Reserved	[31:14]	Reserved
D0W_HSRXTUNE	[13:12]	D0W_HSRXTUNE [1:0]: Selection of HSRX bias resistance for Data Lane 0. (TUNE1,TUNE0): = (00): 1.50k [Ohm] (TUNE1,TUNE0): = (01): 1.75k [Ohm] (TUNE1,TUNE0): = (10): 2.00k [Ohm] (Default) (TUNE1,TUNE0): = (11): 2.25k [Ohm]
Reserved	[11]	Reserved
D0W_DLYCNTRL	[10:8]	D0W_DLYCNTRL [2:0]: Skew control bits. Input/Output skew delayed by ~2^(DLYCNTRL-1) x 20ps for Data Lane 0 in HSRX. 3'b000: (Temporary Default)
Reserved	[7:5]	Reserved
D0W_LPRXVTHLOW	[4]	D0W_LPRXVTHLOW: LPRX input threshold select for Data Lane 0. 1: LPRX input threshold is low 0: LPRX input threshold is high (Temporary Default)
Reserved	[3]	Reserved
D0W_ATMREN	[2]	D0W_ATMREN: Analog timer function enable for Data Lane 0 in HSRX. 0: analog timer function off (Default) 1: analog timer function on This bit is valid only in TESTMODE=1. When TESTMODE = 0, this bit can be written or read but it does not affect any function.
D0W_ATMR	[1:0]	D0W_ATMR [1:0]: Selection of different delay times for tuning of Analog Timer for Clock Lane 0 in HSRX. (ATMR1, ATMR0) = (0,0): Bypass mode (ATMR1, ATMR0) = (0,1): delay = D1 (ATMR1, ATMR0) = (1,0): delay = D2 (Default) (ATMR1, ATMR0) = (1,1): delay = D3

5.3.1.4. D1W_DPHYCONTRX Register

Mnemonic	D1W_DPHYCONTRX (Address = 0x0028)								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved	Reserved	HSRXTUNE1	HSRXTUNE0	Reserved	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	
Type	--	--	R/W	R/W	--	R/W	R/W	R/W	
Default	1	0	1	0	0	0	0	0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved	Reserved	Reserved	LPRXVTHLOW	Reserved	ATMREN	ATMR1	ATMR0	
Type	--	--	--	R/W	--	R/W	R/W	R/W	
Default	0	0	0	0	0	0	1	0	

Table 5.6 D1W_DPHYCONTRX Register

Field Name	Bit	Description
Reserved	[31:14]	Reserved
D1W_HSRXTUNE	[13:12]	D1W_HSRXTUNE [1:0]: Selection of HSRX bias resistance for Data Lane 1. (TUNE1,TUNE0): = (00): 1.50k [Ohm] (TUNE1,TUNE0): = (01): 1.75k [Ohm] (TUNE1,TUNE0): = (10): 2.00k [Ohm] (Default) (TUNE1,TUNE0): = (11): 2.25k [Ohm]
Reserved	[11]	Reserved
D1W_DLYCNTRL	[10:8]	D1W_DLYCNTRL [2:0]: Skew control bits. Input/Output skew delayed by ~ $2^{(DLYCNTRL-1)} \times 20\text{ps}$ for Data Lane 1 in HSRX. 3'b000: (Temporary Default)
Reserved	[7:5]	Reserved
D1W_LPRXVTHLOW	[4]	D1W_LPRXVTHLOW: LPRX input threshold select for Data Lane 1. 1: LPRX input threshold is low 0: LPRX input threshold is high (Temporary Default)
Reserved	[3]	Reserved
D1W_ATMREN	[2]	D1W_ATMREN: Analog timer function enable for Data Lane 1 in HSRX. 0: analog timer function off (Default) 1: analog timer function on This bit is valid only in TESTMODE = 1. When TESTMODE = 0, this bit can be written or read but it does not affect any function.
D1W_ATMR	[1:0]	D1W_ATMR [1:0]: Selection of different delay times for tuning of Analog Timer for Data Lane 1 in HSRX. (ATMR1, ATMR0) = (0,0): Bypass mode (ATMR1, ATMR0) = (0,1): delay = D1 (ATMR1, ATMR0) = (1,0): delay = D2 (Default) (ATMR1, ATMR0) = (1,1): delay = D3

5.3.1.5. D2W_DPHYCONTRX Register

Mnemonic	D2W_DPHYCONTRX (Address = 0x002C)								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved	Reserved	HSRXTUNE1	HSRXTUNE0	Reserved	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	
Type	--	--	R/W	R/W	--	R/W	R/W	R/W	
Default	1	0	1	0	0	0	0	0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved	Reserved	Reserved	LPRXVTHLOW	Reserved	ATMREN	ATMR1	ATMR0	
Type	--	--	--	R/W	--	R/W	R/W	R/W	
Default	0	0	0	0	0	0	1	0	

Table 5.7 D2W_DPHYCONTRX Register

Field Name	Bit	Description
Reserved	[31:14]	Reserved
D2W_HSRXTUNE	[13:12]	D2W_HSRXTUNE [1:0]: Selection of HSRX bias resistance for Data Lane 2. (TUNE1,TUNE0): = (00): 1.50k [Ohm] (TUNE1,TUNE0): = (01): 1.75k [Ohm] (TUNE1,TUNE0): = (10): 2.00k [Ohm] (Default) (TUNE1,TUNE0): = (11): 2.25k [Ohm]
Reserved	[11]	Reserved
D2W_DLYCNTRL	[10:8]	D2W_DLYCNTRL [2:0]: Skew control bits. Input/Output skew delayed by ~ $2^{(DLYCNTRL-1)} \times 20\text{ps}$ for Data Lane 2 in HSRX. 3'b000: (Temporary Default)
Reserved	[7:5]	Reserved
D2W_LPRXVTHLOW	[4]	D2W_LPRXVTHLOW: LPRX input threshold select for Data Lane 2. 1: LPRX input threshold is low 0: LPRX input threshold is high (Temporary Default)
Reserved	[3]	Reserved
D2W_ATMREN	[2]	D2W_ATMREN: Analog timer function enable for Data Lane 2 in HSRX. 0: analog timer function off (Default) 1: analog timer function on This bit is valid only in TESTMODE = 1. When TESTMODE = 0, this bit can be written or read but it does not affect any function.
D2W_ATMR	[1:0]	D2W_ATMR [1:0]: Selection of different delay times for tuning of Analog Timer for Data Lane 2 in HSRX. (ATMR1, ATMR0) = (0,0): Bypass mode (ATMR1, ATMR0) = (0,1): delay = D1 (ATMR1, ATMR0) = (1,0): delay = D2 (Default) (ATMR1, ATMR0) = (1,1): delay = D3

5.3.1.6. D3W_DPHYCONTRX Register

Mnemonic	D3W_DPHYCONTRX (Address = 0x0030)								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved	Reserved	HSRXTUNE1	HSRXTUNE0	Reserved	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	
Type	--	--	R/W	R/W	--	R/W	R/W	R/W	
Default	1	0	1	0	0	0	0	0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved	Reserved	Reserved	LPRXVTHLOW	Reserved	ATMREN	ATMR1	ATMR0	
Type	--	--	--	R/W	--	R/W	R/W	R/W	
Default	0	0	0	0	0	0	1	0	

Table 5.8 D3W_DPHYCONTRX Register

Field Name	Bit	Description
Reserved	[31:14]	Reserved
D3W_HSRXTUNE	[13:12]	D3W_HSRXTUNE [1:0]: Selection of HSRX bias resistance for Data Lane 3. (TUNE1,TUNE0): = (00): 1.50k [Ohm] (TUNE1,TUNE0): = (01): 1.75k [Ohm] (TUNE1,TUNE0): = (10): 2.00k [Ohm] (Default) (TUNE1,TUNE0): = (11): 2.25k [Ohm]
Reserved	[11]	Reserved
D3W_DLYCNTRL	[10:8]	D3W_DLYCNTRL [2:0]: Skew control bits. Input/Output skew delayed by ~ $2^{(DLYCNTRL-1)} \times 20ps$ for Data Lane 3 in HSRX. 3'b000: (Temporary Default)
Reserved	[7:5]	Reserved
D3W_LPRXVTHLOW	[4]	D3W_LPRXVTHLOW: LPRX input threshold select for Data Lane 3. 1: LPRX input threshold is low 0: LPRX input threshold is high (Temporary Default)
Reserved	[3]	Reserved
D3W_ATMREN	[2]	D3W_ATMREN: Analog timer function enable for Data Lane 3 in HSRX. 0: analog timer function off (Default) 1: analog timer function on This bit is valid only in TESTMODE = 1. When TESTMODE = 0, this bit can be written or read but it does not affect any function.
D3W_ATMR	[1:0]	D3W_ATMR [1:0]: Selection of different delay times for tuning of Analog Timer for Data Lane 3 in HSRX. (ATMR1, ATMR0) = (0,0): Bypass mode (ATMR1, ATMR0) = (0,1): delay = D1 (ATMR1, ATMR0) = (1,0): delay = D2 (Default) (ATMR1, ATMR0) = (1,1): delay = D3

5.3.1.7. COM_DPHYCONTRX Register

Mnemonic	COM_DPHYCONTRX (Address = 0x0038)								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	---								
Default	0x00								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved					LPRXCALRES		LPRXCALEN	
Type	---					R/W		R/W	
Default	0x00					0		0	

Table 5.9 COM_DPHYCONTRX Register

Field Name	Bit	Description
Reserved	[31:2]	Reserved
LPRXCALRES	[1]	<p>LPRXCALRES: LPRX Calibration Reset. 0: Not Reset 1: Resets high LPRXCTHLOW Reset with this bit set to 1 requires the bit remains set to 1 for 500 μs or more.</p>
LPRXCALEN	[0]	<p>LPRXCALEN: LPRX Calibration Enable 0: Calibration Switch OFF 1: Calibration Switch ON Calibration with this bit set to 1 requires the bit remains set to 1 for 500 μs or more</p>

5.3.1.8. CLW_CNTRL Register

Mnemonic	CLW_CNTRL (Address = 0x0040)									
Bit	B15	B14	B13	B12	B11	B10	B9	B8		
Name	LaneEnDFT	Reserved								
Type	R/W	---								
Default	0	0x00								
Bit	B7	B6	B5	B4	B3	B2	B1	B0		
Name	Reserved							LaneDisable		
Type	---							R/W		
Default	0x00							0		

Table 5.10 CLW_CNTRL Register

Field Name	Bit	Description
Reserved	[31:16]	Reserved
LaneEnDFT	[15]	<p>LaneEnDFT: Force Lane Enable for DFT The lane is forced to be enabled when TESTMODE = 1 irrespective of status of D0W_LaneDisable and Lane Enable control from PPI layer.</p> <p>1'b1: Force Lane Enable 1'b0: Bypass Lane Enable from PPI Layer enable and LaneDisable (Default)</p>
Reserved	[14:1]	Reserved
LaneDisable	[0]	<p>LaneDisable: Force Lane Disable for Clock Lane. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable (Default)</p> <p>When this bit is set to 1, the Lane is set to Disable by EN port. When this bit is set to 0, the Lane Enable is controlled by EN port from upper layer.</p>

5.3.1.9. D0W_CNTRL Register

Mnemonic	D0W_CNTRL (Address = 0x0044)									
Bit	B15	B14	B13	B12	B11	B10	B9	B8		
Name	LaneEnDFT	Reserved								
Type	R/W	---								
Default	0	0x00								
Bit	B7	B6	B5	B4	B3	B2	B1	B0		
Name	Reserved							LaneDisable		
Type	---							R/W		
Default	0x00							0		

Table 5.11 D0W_CNTRL Register

Field Name	Bit	Description
Reserved	[31:16]	Reserved
LaneEnDFT	[15]	<p>LaneEnDFT: Force Lane Enable for DFT The lane is forced to be enabled when TESTMODE = 1 irrespective of status of D0W_LaneDisable and Lane Enable control from PPI layer.</p> <p>1'b1: Force Lane Enable 1'b0: Bypass Lane Enable from PPI Layer enable and LaneDisable (Default)</p>
Reserved	[14:1]	Reserved
LaneDisable	[0]	<p>LaneDisable: Force Lane Disable for Data Lane 0. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable (Default)</p> <p>When this bit is set to 1, the Lane is set to Disable by EN port. When this bit is set to 0, the Lane Enable is controlled by EN port from upper layer.</p>

5.3.1.10. D1W_CNTRL Register

Mnemonic	D1W_CNTRL (Address = 0x0048)								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	LaneEnDFT	Reserved							
Type	R/W	---							
Default	0	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved							LaneDisable	
Type	---							R/W	
Default	0x00							0	

Table 5.12 D1W_CNTRL Register

Field Name	Bit	Description
Reserved	[31:16]	Reserved
LaneEnDFT	[15]	<p>LaneEnDFT: Force Lane Enable for DFT The lane is forced to be enabled when TESTMODE = 1 irrespective of status of D1W_LaneDisable and Lane Enable control from PPI layer. 1'b1: Force Lane Enable 1'b0: Bypass Lane Enable from PPI Layer enable and LaneDisable (Default)</p>
Reserved	[14:1]	Reserved
LaneDisable	[0]	<p>LaneDisable: Force Lane Disable for Data Lane 1. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable (Default) When this bit is set to 1, the Lane is set to Disable by EN port. When this bit is set to 0, the Lane Enable is controlled by EN port from upper layer.</p>

5.3.1.11. D2W_CNTRL Register

Mnemonic	D2W_CNTRL (Address = 0x004C)									
Bit	B15	B14	B13	B12	B11	B10	B9	B8		
Name	LaneEnDFT	Reserved								
Type	R/W	---								
Default	0	0x00								
Bit	B7	B6	B5	B4	B3	B2	B1	B0		
Name	Reserved							LaneDisable		
Type	---							R/W		
Default	0x00							0		

Table 5.13 D2W_CNTRL Register

Field Name	Bit	Description
Reserved	[31:16]	Reserved
LaneEnDFT	[15]	LaneEnDFT: Force Lane Enable for DFT The lane is forced to be enabled when TESTMODE = 1 irrespective of status of D2W_LaneDisable and Lane Enable control from PPI layer. 1'b1: Force Lane Enable 1'b0: Bypass Lane Enable from PPI Layer enable and LaneDisable (Default)
Reserved	[14:1]	Reserved
LaneDisable	[0]	LaneDisable: Force Lane Disable for Data Lane 2. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable (Default) When this bit is set to 1, the Lane is set to Disable by EN port. When this bit is set to 0, the Lane Enable is controlled by EN port from upper layer.

5.3.1.12. D3W_CNTRL Register

Mnemonic	D3W_CNTRL (Address = 0x0050)								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	LaneEnDFT	Reserved							
Type	R/W	---							
Default	0	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved							LaneDisable	
Type	---							R/W	
Default	0x00							0	

Table 5.14 D3W_CNTRL Register

Field Name	Bit	Description
Reserved	[31:16]	Reserved
LaneEnDFT	[15]	LaneEnDFT: Force Lane Enable for DFT The lane is forced to be enabled when TESTMODE = 1 irrespective of status of D3W_LaneDisable and Lane Enable control from PPI layer. 1'b1: Force Lane Enable 1'b0: Bypass Lane Enable from PPI Layer enable and LaneDisable (Default)
Reserved	[14:1]	Reserved
LaneDisable	[0]	LaneDisable: Force Lane Disable for Data Lane 3. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable (Default) When this bit is set to 1, the Lane is set to Disable by EN port. When this bit is set to 0, the Lane Enable is controlled by EN port from upper layer.

5.3.1.13. Test Mode Control Register

0x0054 is Test Mode Control Register. Don't access this register.

5.3.2. DSI PPI Layer Registers

5.3.2.1. PPI_STARTPPI Register

Mnemonic	PPI_STARTPPI (Address = 0x0104)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	---							
Default	---							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							
Type	---							
Default	---							

Table 5.15 PPI_STARTPPI Register

Field Name	Bit	Description
Reserved	[31:1]	Reserved
startPPI	[0]	startPPI START control bit of PPI-TX function. By writing 1 to this bit, the values of initial registers are latched inside of PPI, and PPI starts function. Once START bit is set to high, the change of the register bits does not affect to function. 0: (Default) Stop function. Writing 0 is invalid and the bit can be set to zero by system reset only. 1: Start function.

5.3.2.2. PPI_BUSYPPI Register

Mnemonic	PPI_BUSYPPI (Address = 0x0108)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	---							
Default	---							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							
Type	---							
Default	---							

Table 5.16 PPI_BUSYPPI Register

Field Name	Bit	Description
Reserved	[31:1]	Reserved
BusyPPI	[0]	BUSY After writing 1 to START bit in STARTPPI register, this bit is set until RESET_N is asserted. 0: Not Busy. (Default) 1: Busy.

5.3.2.3. PPI_LINEINITCNT Register

Mnemonic	PPI_LINEINITCNT (Address = 0x0110)								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	LINEINITCNT[15:8]								
Type	R/W								
Default	0x20								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	LINEINITCNT[7:0]								
Type	R/W								
Default	0x8E								

Table 5.17 PPI_LINEINITCNT Register

Field Name	Bit	Description
Reserved	[31:16]	Reserved
LINEINITCNT	[15:0]	<p>LINEINITCNT Line Initialization Wait Counter This counter is used for line initialization. The count value depends on HFCLK and the value needs to be set to achieve more than 100 μs. The counter starts after STARTPPI bit of STARTPPI register is set. Master device needs to output LP-11 for 100 μs in order for slave device to observe LP-11 for the period. For example, in order to set 100 μs when the period of HFCLK is 12 ns, the counter value should be more than $8333.3 = 0x208D$ (100 μs / 12 ns). Default is 0x208E.</p>

5.3.2.4. PPI_LPTXTIMECNT Register

Mnemonic	PPI_LPTXCNT (Address = 0x0114)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						LPTXCNT[10:8]	
Type	---						R/W	
Default	---						0x00	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LPTXCNT[7:0]							
Type	R/W							
Default	0x01							

Table 5.18 PPI_LPTXTIMECNT Register

Field Name	Bit	Description
Reserved	[31:11]	Reserved
LPTXCNT	[10:0]	LPTXTIMECNT SYSLPTX Timing Generation Counter The counter generates a timing signal for the period of T_{LPX} . The counter is counted by HFCLK. Default value is one. Setting zero is prohibited and the working when set to zero is not guaranteed.

Overwrite prohibited while [BUSYPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)

5.3.2.5. PPI_LANEENABLE Register

Mnemonic	PPI_LANEENABLE (Address = 0x0134)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	---							
Default	---							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			L3EN	L2EN	L1EN	L0EN	CLEN
Type	---			R/W	R/W	R/W	R/W	R/W
Default	---			0	0	0	1	1

Table 5.19 PPI_LANEENABLE Register

Field Name	Bit	Description
Reserved	[15:5]	Reserved
L3EN	[4]	L3 Lane Enable Data Lane 3 Enable 0: Lane operation disabled (Default) 1: Lane operation enabled
L2EN	[3]	L2 Lane Enable Data Lane 2 Enable 0: Lane operation disabled (Default) 1: Lane operation enabled
L1EN	[2]	L1 Lane Enable Data Lane 1 Enable 0: Lane operation disabled 1: Lane operation enabled (Default)
L0EN	[1]	L0 Lane Enable Data Lane 0 Enable 0: Lane operation disabled (Default) 1: Lane operation enabled
CLEN	[0]	Clock Lane Enable Clock Lane 0 Enable 0: Lane operation disabled 1: Lane operation enabled (Default)

This register controls the lane operation at the PPI layer within the DSI-RX module.

In a typical configuration sequence, this register is programmed before StartPPI register. Once StartPPI register is enabled and BusyPPI status indicates busy, user should only reprogram the setting of this register with great care. The following constraints are advised:

Modification to allow the change during busy is considered acceptable with following limitations.

- 1) There must be sufficient length (minimum 100 μ s) of LP11 period before and after the register change such that internal data transfer within the DSI-RX pipeline has been flushed out.
- 2) Switching lane 0 during BTA (when the lane is TX) is not allowed.

5.3.2.6. PPI_TX_RX_TA Register

Mnemonic	PPI_TX_RX_TA (Address = 0x013C)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved					TXTAGOCNT[10:8]		
Type	RO					RW		
Default	0x00					0x0		
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	TXTAGOCNT[7:0]							
Type	RW							
Default	0x08							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					TXTASURECNT[10:8]		
Type	RO					RW		
Default	0x00					0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TXTASURECNT[7:0]					R/W		
Type						0x8		

Table 5.20 PPI_TX_RX_TA Register

Field Name	Bit	Description
Reserved	[31:27]	Reserved
TXTAGOCNT[10:0]	[26:16]	TXTAGOCNT is used to configure the TTA-GET timing as specified by the MIPI D-PHY specification on Global Operation Timing Parameters. This register field should be set to be = $(5 * \text{PPI_LPTXTIMECNT} - 3) / 4$.
Reserved	[15:11]	Reserved
TXTAGOCNT[10:0]	[10:0]	TXTASURECNT is used to configure the TTA-SURE timing as specified by the MIPI D-PHY specification on Global Operation Timing Parameters. This register field should be set to be = $1.5 * \text{PPI_LPTXTIMECNT}$

5.3.2.7. PPI_ATMR Register

0x0140 to 0x0150 are LPRX analog timer test registers. Don't access these registers.

Keep default value.

5.3.2.8. PPI_D0S_CLRSIPOCOUNT Register

Mnemonic	PPI_D0S_CLRSIPOCOUNT (Address = 0x0164)								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	---								
Default	---								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved		D0S_CLRSIPOCOUNT						
Type	--		R/W	R/W	R/W	R/W	R/W	R/W	
Default	--		0	1	1	0	0	1	

Table 5.21 PPI_D0S_CLRSIPOCOUNT Register

Field Name	Bit	Description
Reserved	[31:6]	Reserved
D0S_CLRSIPOCOUNT	[5:0]	D0S_CLRSIPOCOUNT CLRSIPO counter for data lane 0. This counter is used to set asserting period from the time when LP-00 is detected for HS data reception. Counter value is counted by DSI HS Byte clock, which is DSI bit clock / 4. Counted cycle is the sum of four or five and the registered value.

Overwrite prohibited while [BUSYPPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)

5.3.2.9. PPI_D1S_CLRSIPOCOUNT Register

Mnemonic	PPI_D1S_CLRSIPOCOUNT (Address = 0x0168)								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	---								
Default	---								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved		D1S_CLRSIPOCOUNT						
Type	--		R/W	R/W	R/W	R/W	R/W	R/W	
Default	--		0	1	1	0	0	1	

Table 5.22 PPI_D1S_CLRSIPOCOUNT Register

Field Name	Bit	Description
Reserved	[31:6]	Reserved
D1S_CLRSIPOCOUNT	[5:0]	<p>D1S_CLRSIPOCOUNT CLRSIPO counter for data lane 1. This counter is used to set asserting period from the time when LP-00 is detected for HS data reception. Counter value is counted by DSI HS Byte clock, which is DSI bit clock / 4. Counted cycle is the sum of four or five and the registered value.</p>

Overwrite prohibited while [BUSYPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)

5.3.2.10. PPI_D2S_CLRSIPOCOUNT Register

Mnemonic	PPI_D2S_CLRSIPOCOUNT (Address = 0x016C)								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	---								
Default	---								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved	D2S_CLRSIPOCOUNT							
Type	--	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Default	---	0	1	1	0	0	0	1	

Table 5.23 PPI_D2S_CLRSIPOCOUNT Register

Field Name	Bit	Description
Reserved	[31:6]	Reserved
D2S_CLRSIPOCOUNT	[5:0]	<p>D2S_CLRSIPOCOUNT CLRSIPO counter for data lane 2. This counter is used to set asserting period from the time when LP-00 is detected for HS data reception. Counter value is counted by DSI HS Byte clock, which is DSI bit clock / 4. Counted cycle is the sum of four or five and the registered value.</p>

Overwrite prohibited while [BUSYPPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)

5.3.2.11. PPI_D3S_CLRSIPOCOUNT Register

Mnemonic	PPI_D3S_CLRSIPOCOUNT (Address = 0x0170)								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	---								
Default	---								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved		D3S_CLRSIPOCOUNT						
Type	--		R/W	R/W	R/W	R/W	R/W	R/W	
Default	--		0	1	1	0	0	1	

Table 5.24 PPI_D3S_CLRSIPOCOUNT Register

Field Name	Bit	Description
Reserved	[31:6]	Reserved
D3S_CLRSIPOCOUNT	[5:0]	<p>D3S_CLRSIPOCOUNT CLRSIPO counter for data lane 3. This counter is used to set asserting period from the time when LP-00 is detected for HS data reception. Counter value is counted by DSI HS Byte clock, which is DSI bit clock / 4. Counted cycle is the sum of four or five and the registered value.</p>

Overwrite prohibited while [BUSYPPPI].BusyPpi is 1. (HW implementation blocks an overwrite.)

5.3.2.12. PPI_PRE Register

0x0180 to 0x0190 are PPI PRE parameter test registers. Don't access these registers.
Keep default value.

5.3.2.13. PPI_PREP Register

0x01A0 to 0x01B0 are PPI PREP parameter test registers. Don't access these registers.
Keep default value.

5.3.2.14. PPI_ZERO Register

0x01C0 to 0x01D0 are PPI ZERO parameter test registers. Don't access these registers.
Keep default value.

5.3.2.15. PPI_CLRFLG Register

0x01E0 is PPI CLRFLG test control register. Don't access this register.
Keep default value.

5.3.2.16. PPI_CLRSIPO Register

0x01E4 is PPI CLRSIPO test control register. Don't access this register.
Keep default value.

5.3.2.17. HSTIMEOUT Register

0x01F0 is HSTIMEOUT test register. Don't access this register.
Keep default value.

5.3.2.18. HSTIMEOUTENABLE Register

0x01F4 is HSTIMEOUTENABLE test register. Don't access this register.
Keep default value.

5.3.3. DSI Protocol Layer Registers

5.3.3.1. DSI_STARTDSI Register

Mnemonic	DSI_STARTDSI (Address = 0x0204)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	---							
Default	---							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							
Type	---							
Default	---							

Table 5.25 DSI_STARTDSI Register

Field Name	Bit	Description
Reserved	[31:1]	Reserved
startDSI	[0]	<p>STARTDSI START control bit of DSI-TX function. When 1 is set to this bit, the value is preserved in the DSI-RX internal register and DSI-RX starts up. Once this bit is set, modification to the bit does not affect the DSI-RX operation.</p> <p>0: DSI-RX is stopped (Default). Writing 0 to this bit is invalid. Only system reset can set it to 0.</p> <p>1: DSI-RX starts up.</p>

5.3.3.2. DSI_BUSYDSI Register

Mnemonic	DSI_BUSYDSI (Address = 0x0208)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	---							
Default	---							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							busyDSI
Type	---							RO
Default	---							1

Table 5.26 DSI_BUSYDSI Register

Field Name	Bit	Description
Reserved	[31:1]	Reserved
BusyDSI	[0]	Busy state Writing 1 to STARTDsi bit of STARTDSI sets this bit to 1 until the reset signal RESET_N is asserted. 0: Not used (Not Busy) 1: Used (Busy) (Default)

5.3.3.3. DSI_LANEENABLE Register

Mnemonic	DSI_LANEENABLE (Address = 0x0210)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	---							
Default	---							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			L3EN	L2EN	L1EN	L0EN	CLEN
Type	---			R/W	R/W	R/W	R/W	R/W
Default	---			0	0	0	1	0

Table 5.27 DSI_LANEENABLE Register

Field Name	Bit	Description
Reserved	[15:5]	Reserved
L3EN	[4]	L3 Lane Enable Data Lane 3 Enable 0: Lane operation disabled (Default) 1: Lane operation enabled
L2EN	[3]	L2 Lane Enable Data Lane 2 Enable 0: Lane operation disabled (Default) 1: Lane operation enabled
L1EN	[2]	L1 Lane Enable Data Lane 1 Enable 0: Lane operation disabled 1: Lane operation enabled (Default)
L0EN	[1]	L0 Lane Enable Data Lane 0 Enable 0: Lane operation disabled (Default) 1: Lane operation enabled
CLEN	[0]	Clock Lane Enable Clock Lane 0 Enable 0: Lane operation disabled (Default) 1: Lane operation enabled

This register controls the lane operation at the PPI layer within the DSI-RX module.

In a typical configuration sequence, this register is programmed before StartDSI register. Once StartDSI register is enabled and BusyDSI status indicates busy, user should only reprogram the setting of this register with great care. The following constraints are advised:

Modification to allow the change during busy is considered acceptable with following limitations.

- 1) There must be sufficient length (minimum 100 μ s) of LP11 period before and after the register change such that internal data transfer within the DSI-RX pipeline has been flushed out.
- 2) Switching lane 0 during BTA (when the lane is TX) is not allowed.

5.3.3.4. DSI_LANESTATUS0 Register

Mnemonic	DSI_LANESTATUS0 (Address = 0x0214)								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	---								
Default	---								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved		L1RxActiveHs	L0RxActiveHs	L1RxActiveHs	L0RxActiveHs	CIRxActiveHs		
Type	---		RO	RO	RO	RO	RO		
Default	---		0	0	0	0	0		

Table 5.28 DSI_LANESTATUS0 Register

Field Name	Bit	Description
Reserved	[31:5]	Reserved
L3RxActiveHS	[4]	Data Lane 3 Rx Active HS mode status 0: Lane 3 not in HS Mode 1: Lane 3 in HS Mode
L2RxActiveHS	[3]	Data Lane 2 Rx Active HS mode status 0: Lane 2 not in HS Mode 1: Lane 2 in HS Mode
L1RxActiveHS	[2]	Data Lane 1 Rx Active HS mode status 0: Lane 1 not in HS Mode 1: Lane 1 in HS Mode
L0RxActiveHS	[1]	Data Lane 0 Rx Active HS mode status 0: Lane 0 not in HS Mode 1: Lane 0 in HS Mode
CIRxActiveHS	[0]	Clock Lane Rx Active HS mode status 0: Clock Lane not in HS Mode 1: Clock Lane in HS Mode

Displays dynamically when a lane is in HS RX mode.

5.3.3.5. DSI_LANESTATUS1 Register

Mnemonic	DSI_LANESTATUS1 (Address = 0x0218)							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved			L3 UlpsEsc	L2 UlpsEsc	L1 UlpsEsc	L0 UlpsEsc	Cl UlpsEsc
Type	---			RO	RO	RO	RO	RO
Default	---			0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			L3Stop State	L2Stop State	L1Stop State	L0Stop State	ClStop State
Type	---			RO	RO	RO	RO	RO
Default	---			-	-	-	-	-

Table 5.29 DSI_LANESTATUS1 Register

Field Name	Bit	Description
Reserved	[31:13]	Reserved
L3 UlpsEsc	[12]	L3UlpsEsc—Data Lane 3 Rx Ulps Esc
L2 UlpsEsc	[11]	L2UlpsEsc—Data Lane 2 Rx Ulps Esc
L1 UlpsEsc	[10]	L1UlpsEsc—Data Lane 1 Rx Ulps Esc
L0 UlpsEsc	[9]	L0UlpsEsc—Data Lane 0 Rx Ulps Esc
Cl UlpsEsc	[8]	ClUlpsEsc—Clock Lane Rx Ulps Esc
Reserved	[7:5]	Reserved
L3Stop State	[4]	Data Lane 3 in Stop State, initial value depends on the lane status
L2Stop State	[3]	Data Lane 2 in Stop State, initial value depends on the lane status
L1Stop State	[2]	Data Lane 1 in Stop State, initial value depends on the lane status
L0Stop State	[1]	Data Lane 0 in Stop State, initial value depends on the lane status
ClStop State	[0]	Clock Lane in Stop State, initial value depends on the lane status

5.3.3.6. DSI_INTSTATUS Register

Mnemonic	DSI_INTSTATUS (Address = 0x0220)											
Bit	B31	B30	B29	B28	B27	B26	B25	B24				
Name	ErrRxFifoOvf	ErrLpTxTo	ErrCntLP1	ErrCntLP0	Reserved							
Type	RO											
Default	0x00											
Bit	B23	B22	B21	B20	B19	B18	B17	B16				
Name	Reserved	L0BTAResquest	L0UlpsEscOFF	L0UlpsEscON	L0Trigger[3:0]							
Type	RO											
Default	0x00											
Bit	B15	B14	B13	B12	B11	B10	B9	B8				
Name	ErrDsiProtocol	Reserved	ErrInvalid	Reserved	ErrDataType	Reserved	ErrEccDbl	ErrEccCrctd				
Type	RO											
Default	0x00											
Bit	B7	B6	B5	B4	B3	B2	B1	B0				
Name	Reserved	ErrCntr	ErrHsRxTo	ErrSyncEsc	ErrEsc	ErrEotSyncHs	ErrSotSyncHs	ErrSotHs				
Type	RO											
Default	0x00											

Table 5.30 DSI_INTSTATUS Register

Field Name	Bit	Description
ErrRxFifoOvf	[31]	ErrRxFifoOvf—Fifo Overflow This bit is set if the synchronization FIFO in PPI from HS data RX clock to system clock is full when an additional HS data is written. Assertion of this bit means there was an omission in RX data. An overflow may happen for example when the system clock is slower than the line rate byte clock
ErrLpTxTo	[30]	ErrLpTxTo — LP Transmission Timeout Error This bit indicates that an error has been detected at the point of LP TX timeout period ([LPTXTO].LpTxTo) during an LP transfer. The application layer must issue a BTA and return the bus to DSI-TX when it receives this error.
ErrCntLP1	[29]	ErrCntLP1 — Contention Detection LP1 Error This bit is set to 1 when a contention is detected during LP1 transfer.
ErrCntLP0	[28]	ErrCntLP0 — Contention Detection LP0 Error This bit is set to 1 when a contention is detected during LP1 transfer.
Reserved	[27:23]	Reserved
L0BTAResquest	[22]	L0BTAResquest—Lane 0 BTA Request This bit is set to 1 when Direction signal from PPI is changed from 1 (input) to 0 (output).
L0UlpsEscOFF	[21]	L0UlpsEscOFF—Lane 0 ULPS OFF This bit is set to 1 when UlpsActiveNot of lane 0 is deasserted from 0 to 1.
L0UlpsEscON	[20]	L0UlpsEscON—Lane 0 ULPS ON This bit is set to 1 when UlpsActiveNot of lane 0 is asserted from 1 to 0.
L0Trigger	[19:16]	L0Trigger—Lane 0 Trigger These bits are set to 1 when corresponding trigger is received. According to MIPI DSI specification [2], DSI-RX may only receive remote application reset

		trigger. [3] = Unknown-5 “10100000” [2] = Unknown-4 “00100001” [1] = Unknown-3 “01011101” [0] = Reset-Trigger [Remote Application] “01100010”
ErrDsiProtocol	[15]	ErrDsiProtocol—DSI Protocol Violation Flags an error when a MIPI specification violation of following two types is detected. EoT packet is not received before EoT sequence in HS transfer. (It is because EoT packet transfer in LP transfer is not recommended. This error is not detected in LP transfer mode.) BTA is not received though a read request command is received (this condition is not implemented in TC358867XBG.)
Reserved	[14]	Reserved
ErrInvalid	[13]	ErrInvalid—Invalid transmission length Indicates an error is detected that LP-11 is observed before the payload of bytes described in head WC has been received, after a correct packet header is received. The received data before this error is detected is sent to upper layer.
Reserved	[12]	Reserved
ErrDataType	[11]	ErrDataType—DSI Data Type Not Recognized Indicates an error is detected that a packet of undefined Data Type in DSI-RX is received.
Reserved	[10]	Reserved
ErrEccDbl	[9]	ErrEccDbl—Ecc Error cannot be corrected Indicates an uncorrectable error is detected in ECC
ErrEccCrctd	[8]	ErrEccCrctd—Ecc Error corrected Indicates a corrected error is detected in ECC.
Reserved	[7]	Reserved
ErrCntrl	[6]	ErrCntrl—False Control Error Indicates an error is detected that LP-10 is not detected after a valid escape sequence or a BTA sequence. Bit[5] : ErrHsRxTo—Hs Rx Time out Error
ErrHsRxTo	[5]	ErrHsRxTo—Hs Rx Time out Error Indicates an error is detected that HS RX timeout period is reached during HS transfer.
ErrSyncEsc	[4]	ErrSyncEsc—LP Transmission Sync Error Indicates an error is detected that the received data is not aligned to byte at the end of LP transfer.
ErrEsc	[3]	ErrEsc—Escape Mode Entry Command Error Indicates an error is detected that an entry command to unknown escape mode is received
ErrEotSyncHs	[2]	ErrEotSyncHs—EoT Sync Error Indicates an error is detected that the last bit of transferred data is not aligned to byte in EoT sequence of HS transfer.
ErrSotSyncHs	[1]	ErrSotSyncHs—SoT Sync Error Indicates an uncorrectable error is detected in SoT sequence of HS transfer.
ErrSotHs	[0]	ErrSotHs—SoT Error Indicates a corrected error is detected in SoT sequence of HS transfer.

5.3.3.7. DSI_INTMASK Register

Mnemonic		DSI_INTMASK (Address = 0x0224)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24		
Name	MaskRxFifoOvf	MaskLpTxTo	Reserved							
Type	R/W	R/W	---							
Default	1	1	0x30							
Bit	B23	B22	B21	B20	B19	B18	B17	B16		
Name	Reserved	MaskL0BTAResquest	MaskL0UlpsEscOFF	MaskL0UlpsEscON	MaskL0Trigger[3:0]					
Type	-	R/W								
Default	0	1	1	1	0xF					
Bit	B15	B14	B13	B12	B11	B10	B9	B8		
Name	MaskDsiProtocol	Reserved	MaskInvalid	Reserved	MaskDataType	Reserved	MaskEccDbl	MaskEccCrctd		
Type	R/W	-	R/W	-	R/W	-	R/W	R/W		
Default	1	0	1	0	1	1	1	1		
Bit	B7	B6	B5	B4	B3	B2	B1	B0		
Name	Reserved	MaskCntr	MaskHsRxTo	MaskSyncEsc	MaskEsc	MaskEotSyncHs	MaskSotSyncHs	MaskSotHs		
Type	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Default	1	1	1	1	1	1	1	1		

Table 5.31 DSI_INTMASK Register

Field Name	Bit	Description
MaskRxFifoOvf	31	MaskRxFifoOvf—Fifo Overflow Mask Masks FIFO overflow notification.
MaskLpTxTo	30	MaskLpTxTo — LP Transmission Timeout Mask Masks LP TX Timeout error notification.
Reserved	[29:23]	Reserved
MaskL0BTAResquest	22	MaskL0BTAResquest—Lane 0 BTA Request Mask Masks BTA request of lane 0.
MaskL0UlpsEscOFF	21	MaskL0UlpsEscOFF—Lane 0 ULPS OFF Mask Masks ULPS OFF notification of lane 0.
MaskL0UlpsEscON	20	MaskL0UlpsEscON—Lane 0 ULPS ON Mask Masks ULPS ON notification of lane 0.
MaskL0Trigger	[19:16]	MaskL0Trigger—Lane 0 Trigger Mask Masks trigger notification of lane 0
MaskDsiProtocol	15	MaskDsiProtocol—DSI Protocol Violation Mask This bit needs to be set to mask “EoT packet not received” error if the host device does not support EoT packet
Reserved	14	Reserved

MaskInvalid	13	MaskInvalid—Invalid transmission length Mask Masks invalid transmission length error notification.
Reserved	12	Reserved
MaskDataType	11	MaskDataType—DSI Data Type Not Recognized Mask Masks DSI Data Type error notification.
Reserved	10	Reserved
MaskEccDbl	9	MaskEccDbl—Ecc Error cannot be corrected Mask Masks ECC uncorrectable error notification
MaskEccCrctd	8	MaskEccCrctd—Ecc Error corrected Mask Masks ECC correctable error notification.
Reserved	7	Reserved
MaskCntrl	6	MaskCntrl—False Control Error Mask Masks False Control error notification
MaskHsRxTo	5	MaskHsRxTo—Hs Rx Time out Error Mask Masks HS RX timeout notification.
MaskSyncEsc	4	MaskSyncEsc—LP Transmission Sync Error Mask Masks LP Transmission Sync Error notification.
MaskEsc	3	MaskEsc—Escape Mode Entry Command Error Mask Masks EoT Sync error notification.
MaskEotSyncHs	2	MaskEotSyncHs—EoT Sync Error Mask Masks EoT Sync error notification.
MaskSotSyncHs	1	MaskSotSyncHs—SoT Sync Error Mask Masks SoT Sync error notification.
MaskSotHs	0	MaskSotHs—SoT Error Mask Masks SoT error notification.

5.3.3.8. DSI_INTCLR Register

DSI_INTCLR (Address = 0x0228)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	ClrRxFifoOvf	ClrLpTxTo	Reserved					
Type	W	W	---					
Default	0	0	0x00					
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved	ClrL0BTAResquest	ClrL0UlpsEscOFF	ClrL0UlpsEscON	ClrL0Trigger[3:0]			
Type	-	W						
Default	0	0	0	0	0x0			
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	ClrDsiProtocol	Reserved	ClrInvalid	Reserved	ClrDataType	Reserved	ClrEccDbl	ClrEccCrctd
Type	R/W	-	R/W	-	W	-	W	W
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	ClrCntr	ClrHsRxTo	ClrSyncEsc	ClrEsc	ClrEotSyncHs	ClrSotSyncHs	ClrSotHs
Type	-	W	W	W	W	W	W	W
Default	0	0	0	0	0	0	0	0

Table 5.32 DSI_INTCLR Register

Field Name	Bit	Description
ClrRxFifoOvf	31	ClrRxFifoOvf—Clear Fifo Overflow Clears FIFO overflow notification.
ClrLpTxTo	30	ClrLpTxTo — Clear LP Transmission Timeout Clears LP TX Timeout error notification.
Reserved	[29:23]	Reserved
ClrL0BTAResquest	22	ClrL0BTAResquest—Clear Lane 0 BTA Request Clears BTA request of lane 0.
ClrL0UlpsEscOFF	21	ClrL0UlpsEscOFF—Clear Lane 0 ULPS OFF Clears ULPS OFF notification of lane 0.
ClrL0UlpsEscON	20	ClrL0UlpsEscON—Clear Lane 0 ULPS ON Clears ULPS ON notification of lane 0.
ClrL0Trigger	[19:16]	ClrL0Trigger—Clear Lane 0 Trigger Clears trigger notification of lane 0
ClrDsiProtocol	15	ClrDsiProtocol—Clear DSI Protocol Violation Clears DSI protocol violation interrupt.
Reserved	14	Reserved
ClrInvalid	13	ClrInvalid—Clear Invalid transmission length Clears invalid transmission length error notification.

Reserved	12	Reserved
ClrDataType	11	ClrDataType—Clear DSI Data Type Not Recognized Clears DSI Data Type error notification.
Reserved	10	Reserved
ClrEccDbl	9	CLREccDbl—Clear Ecc Error cannot be corrected Clears ECC uncorrectable error notification
ClrEccCrctd	8	ClrEccCrctd—Clear Ecc Error corrected Clears ECC correctable error notification.
Reserved	7	Reserved
ClrCntrl	6	ClrCntrl—Clear False Control Error Clears False Control error notification
ClrHsRxTo	5	ClrHsRxTo—Clear Hs Rx Time out Error Clears HS RX timeout notification.
ClrSyncEsc	4	ClrSyncEsc—Clear LP Transmission Sync Error Clears LP Transmission Sync Error notification.
ClrEsc	3	ClrEsc—Clear Escape Mode Entry Command Error Clears EoT Sync error notification.
CLREotSyncHs	2	ClrEotSyncHs—Clear EoT Sync Error Clears EoT Sync error notification.
ClrSotSyncHs	1	ClrSotSyncHs—Clear SoT Sync Error Clears SoT Sync error notification.
ClrSotHs	0	ClrSotHs—Clear SoT Error Clears SoT error notification.

5.3.3.9. DSI_LPTXTO Register

Mnemonic	DSI_LPTXO (Address = 0x0230)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	LPTXTO[31:24]							
Type	R/W							
Default	0xFF							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	LPTXTO[23:16]							
Type	R/W							
Default	0xFF							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	LPTXTO[15:8]							
Type	R/W							
Default	0xFF							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LPTXTO[7:0]							
Type	R/W							
Default	0xFF							

Table 5.33 DSI_LPTXTO Register

Field Name	Bit	Description
LPTXTO[31:0]	[31:0]	<p>LpTxTO — LP Transmission Timeout Value</p> <p>Specify the LP TX timeout period in SYSCLK cycle. LP TX timeout counter counts by SYSCLK. DSI-RX counts the period in which Direction from PPI is 0 (output) and issues an interrupt ([INTSTATUS].ErrLpTxTo) to the application layer when the counter value reaches LpTxTo.</p>

5.3.4. DSI General Registers

5.3.4.1. DSIERRCNT Register

Mnemonic	DSIERRCNT (Address = 0x0300)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Err_Mask							
Type	R/W							
Default	0xC0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Err_Mask							
Type	R/W							
Default	0x80							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Overflow	ErrCnt						
Type	RO	RO						
Default	1'b0	0x00						

Table 5.34 DSIERRCNT Register

Field Name	Bit	Description
ERR_MASK	[31:16]	DSI Error mask 0: enable 1: mask
Reserved	[15:8]	Reserved
Overflow	[7]	Overflow This bit is set if ErrCnt is overflowed. Similar to ErrCnt, it is cleared when it is read
ErrCnt	[6:0]	DSI Error Count Error count increment whenever the DSI Rx receives an error as defined in DSI standard. It is cleared after reading by the DSI host or I ² C master.

5.3.5. DSI Application Layer Registers

5.3.5.1. Application Layer Control Register

Mnemonic	APLCTRL (Address = 0x0400)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					NOPKTENDMSK	CHKSUMMSK	ECCDBLMSK
Type	RO					R/W	R/W	R/W
Default	0x0					1'b0	1'b1	1'b0

Table 5.35 Application Layer Control Register

Field Name	Bit	Description
Reserved	[31:3]	Reserved
NOPKTENDMSK	[2]	No dsapPktEnd error mask 1'b0: mask 1'b1: not mask
CHKSUMMSK	[1]	Checksum error mask 1'b0: mask 1'b1: not mask
ECCDBLMSK	[0]	Multi-bit ECC error mask 1'b0: mask 1'b1: not mask

This register is reserved for internal use only.

5.3.5.2. DSI Read Packet Length Register

Mnemonic	RDPKTLN (Address = 0x0404)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					RDPKTLN		
Type	RO					R/W		
Default	0x00					0x3		

Table 5.36 DSI Read Packet Length Register

Field Name	Bit	Description
Reserved	[31:3]	Reserved
RDPKTLN	[2:0]	<p>DSI Read Packet Size. Configures the number of bytes that TC358867XBG chip is to return in the DSI read response packet.</p> <p>3'b000: 1 byte 3'b001: 2 byte 3'b010: 3 byte :: 3'b111: 8 bytes</p> <p>Default is set to 3 (4 bytes).</p>

5.4. DPI Registers

5.4.1. DPIPXLFMT

Mnemonic	DPIPXLFMT (Address = 0x0440)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved					VS_Pol	HS_Pol	DE_Pol	
Type	RO					RW	RW	RW	
Default	0x0					0x1	0x1	0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved				sub_cfg_type		dpi_bpp		
Type	RO				RW		RW		
Default	0x0				0x0		0x0		

Table 5.37 DPIPXLFMT Register

Register Field	Bit	Default	Description
Reserved	[31:11]	0x0	Reserved
VS_Pol	[10]	0x1	VSYNC Polarity Control 0: Active High 1: Active Low
HS_Pol	[9]	0x1	HSYNC Polarity Control 0: Active High 1: Active Low
DE_Pol	[8]	0x0	DE Polarity Control 0: Active High 1: Active Low
Reserved	[7:4]	0x0	Reserved
sub_cfg_type	[3:2]	0x0	Alignment of pixels 0: Config1 (LSB aligned) 1: Config2 (Loosely Packed) 2: Config3 (LSB aligned 8-bit)
dpi_bpp	[1:0]	0x0	0: RGB888 1: RGB666 2: RGB565

5.5. Parallel Output Registers

5.5.1. POCTRL

Mnemonic	POCTRL (Address = 0x0448)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	S2P	Reserved			PCLK_Pol	VS_Pol	HS_Pol	DE_Pol	
Type	RW	RO			RW	RW	RW	RW	
Default	0x0	0x0			0x0	0x0	0x0	0x0	

Table 5.38 POCTRL Register

Register Field	Bit	Default	Description
Reserved	[31:8]	0x0	Reserved
S2P	[7]	0x0	DSI to Parallel Out mode This bit will set the iomux to output parallel data. 0: Parallel data not output 1: Parallel data output
Reserved	[6:4]	0x0	Reserved
PCLK_Pol	[3]	0x0	PCLK Polarity Control Decides which edge of PCLK will be aligned with output data 0: Rising edge of PCLK aligned with output data 1: Falling edge of PCLK aligned with output data
VS_Pol	[2]	0x0	VSYNC Polarity Control 0: Active High 1: Active Low
HS_Pol	[1]	0x0	HSYNC Polarity Control 0: Active High 1: Active Low
DE_Pol	[0]	0x0	DE Polarity Control 0: Active High 1: Active Low

5.6. Video Path0 Configuration Registers

5.6.1. Video Path0 Control (VPCTRL0)

Mnemonic	VPCTRL (Address = 0x0450)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	VSDELAY[11:4]							
Type	RW							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	VSDELAY [3:0]				Reserved			
Type	RW				RO			
Default	0x5				0x0			
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						OPXLFMT	
Type	RO						RW	
Default	0x0						0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			FRMSYNC	Reserved			MSF
Type	RO			RW	RO			RW
Default	0x0			0x0	0x0			0x0

Table 5.39 Video Path0 Control (VPCTRL0) Register

Field Name	Bit	Description
VSDELAY[11:0]	[31:20]	<p>VSYNC Delay</p> <p>- if FRMSYNC is enabled:</p> <p>The start of VSYNC is delayed from the time that a VSYNC Start DSI packet is received on DSI link by the number of pixel clocks as configured in this register.</p> <p>- if FRMSYNC is disabled:</p> <p>The start of VSYNC/HSYNC is delayed from the time that a VSYNC/HSYNC Start DSI packet is received on the DSI link by the number of pixel clocks as configured in this register.</p>
reserved	[19:9]	Reserved
OPXLFMT	[8]	<p>Output Pixel Format</p> <p>1'b0: Selects RGB666 format for output on TC358867XBG link. (Default)</p> <p>1'b1: Selects RGB888 format for output on TC358867XBG link.</p>
Reserved	[7:5]	Reserved

FRMSYNC	[4]	<p>Video Timing Gen Enable 1'b0: Disabled(Default) 1'b1: Enabled.</p> <p>When enabled, video timing signals that drive TC358867XBG Transmitter (VSYNC, HSYNC and DE) are driven by the on-chip Video Timing Gen module according to programmed parameters in VTIM1, VTIM2, HTIM1, HTIM2 and VPCTRL registers.</p> <p>This bit should be disabled only in video mode transmission where Host transmits video timing together with video data and where pixel clock source is from DSI clock.</p>
Reserved	[3:1]	Reserved
MSF	[0]	<p>MSF: Magic Square FRC 1'b0: Magic Square is disabled. (Default) 1'b1: magic Square is enabled</p>

5.6.2. Horizontal Timing Control0 Register 1 (HTIM01)

Mnemonic	HTIM1 (Address = 0x0454)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	HBPR[7:0]							
Type	R/W							
Default	0x4							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	HPW[7:0]							
Type	R/W							
Default	0x8							

Table 5.40 Horizontal Timing Control0 Register 1 (HTIM01) Register

Field Name	Bit	Description
Reserved	[31:25]	Reserved
HBPR	[24:16]	<p>Horizontal Back Porch</p> <p>8'h0: : 8'h4: Default : 8'hff: HBPR</p> <p>Max HBPR = 510 pixel</p> <p>Note: These bits must be multiple of even pixel</p> <p>This bit field is used only when:</p> <ul style="list-style-type: none"> - VPCTRL.FRMSYNC bit is enabled
Reserved	[15:9]	Reserved
HPW	[8:0]	<p>Horizontal Pulse Width</p> <p>8'h0: : 8'h8: Default : 8'hff: HPW</p> <p>Max HPW = 510 pixel</p> <p>Note: These bits must be multiple of even pixel</p> <p>This bit field is used only when:</p> <ul style="list-style-type: none"> - VPCTRL.FRMSYNC bit is enabled

5.6.3. Horizontal Timing Control0 Register 2 (HTIM02)

Mnemonic	HTIM2 (Address = 0x0458)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	HFPR[7:0]							
Type	R/W							
Default	0x4							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	HDISPR[7:0]							
Type	R/W							
Default	0xa0							

Table 5.41 Horizontal Timing Control0 Register 2 (HTIM02) Register

Field Name	Bit	Description
Reserved	[31:25]	Reserved
HFPR	[24:16]	<p>Horizontal Front Porch</p> <p>8'h0: : 8'h4: Default : 8'hff: HFPR</p> <p>Max HFPR = 510 pixel</p> <p>Note: These bits must be multiple of even pixel</p> <p>This bit field is used only when:</p> <ul style="list-style-type: none"> - VPCTRL.FRMSYNC bit is enabled.
Reserved	[15:11]	Reserved
HDISPR	[10:0]	<p>Horizontal Active video size</p> <p>8'h0: : 8'ha0: Default : 8'h3ff: HDISPR</p> <p>Max HDISPR = 2046 pixel</p> <p>Note: These bits must be multiple of even pixel</p> <p>This bit field is used only when:</p> <ul style="list-style-type: none"> - VPCTRL.FRMSYNC bit is enabled.

5.6.4. Vertical Timing Control0 Register 1 (VTIM01)

Mnemonic	VTIM1 (Address = 0x045C)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	VBPR[7:0]							
Type	R/W							
Default	0x8							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VSPR[7:0]							
Type	R/W							
Default	0x10							

Table 5.42 Vertical Timing Control0 Register 1 (VTIM01) Register

Field Name	Bit	Description
Reserved	[31:24]	Reserved
VBPR[7:0]	[23:16]	<p>Vertical Back Porch 8'h0: : 8'h08: Default : 8'hff: VBPR Max VBPR = 256 line This bit field is used only when:</p> <ul style="list-style-type: none"> - VPCTRL.FRMSYNC bit is enabled. - This field is not used in pulse mode.
Reserved	[15:8]	Reserved
VSPR[7:0]	[7:0]	<p>Vertical Sync Pulse Width 8'h0: : 8'h10: Default : 8'hff: VSPR Max VSPR = 255 line This bit field is used only when:</p> <ul style="list-style-type: none"> - VPCTRL.FRMSYNC bit is enabled. - This field is not used in pulse mode.

5.6.5. Vertical Timing Control0 Register 2 (VTIM02)

Mnemonic	VTIM2 (Address = 0x0460)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	VFPR[7:0]							
Type	R/W							
Default	0x8							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					VDISPR[10:8]		
Type	RO					R/W		
Default	0x0					0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VDISPR[7:0]							
Type	R/W							
Default	0xf0							

Table 5.43 Vertical Timing Control0 Register 2 (VTIM02) Register

Field Name	Bit	Description
Reserved	[31:24]	Reserved
VFPR[7:0]	[23:16]	<p>Vertical Front Porch 8'h0: : 8'h08: Default : 8'hff: VFP Max VFP = 255 line This bit field is used only when: - VPCTRL.FRMSYNC bit is enabled.</p>
Reserved	[15:11]	Reserved
VDISPR[10:0]	[10:0]	<p>Vertical Display Size 11'h0: : 11'hf0: Default : 11'h7ff: VDISPR Max VDISPR = 2047 line This bit field is used only when: - VPCTRL.FRMSYNC bit is enabled.</p>

5.6.6. Video Frame Timing Upload Enable0 (VFUEN0)

Mnemonic	VFUEN (Address = 0x0464)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							
Type	RO							
Default	0x0							

Table 5.44 Video Frame Timing Upload Enable0 (VFUEN0) Register

Field Name	Bit	Description
Reserved	[31:1]	Reserved
VFUEN	[0]	<p>Video Frame Timing Upload Enable 0: No action 1: Upload enable</p> <p>After this bit has been written to 1, the chip will upload (copy) the newly programmed video timing parameters (HTIM1, HTIM2, VTIM1, and VTIM2) to the active set of video timing registers at the next VSYNC event. At that point, this bit will also be automatically cleared by hardware.</p> <p>This register must be programmed after the above video timing parameters have been programmed.</p> <p>Following a hardware reset, this bit is Default to “1” so that when VSYNC is active, Default values in the video timing parameter registers will be uploaded to the shadow registers.</p> <p>This bit field is used only when:</p> <ul style="list-style-type: none"> - VPCTRL.FRMSYNC bit is enabled.

5.7. System register description

The following sections provide a detailed description of the registers that are responsible for TC358867XBG chip's overall control & Status.

5.7.1. Chip ID and Revision Register

Mnemonic	IDREG (Address = 0x0500)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	CHIPID[7:0]								
Type	RO								
Default	0x66								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	REVID								
Type	RO								
Default	0x0X								

Table 5.45 Chip ID and Revision ID Register

Field Name	Bit	Description
Reserved	[31:16]	Reserved
ChipID[7:0]	[15:8]	Chip ID 8'h66
REVID[7:0]	[7:0]	Revision ID 8'h01: DIS_ASSR pin is "L". ASSR is enabled on DP main link. 8'h03: DIS_ASSR pin is "H". ASSR is disabled on DP main link.

5.7.2. SYS BOOT Register

Mnemonic	SYSBOOT (Address = 0x0504)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		I2CAdr	Reserved		DSIRef	ClkSrc	
Type	RO		RO	RO		RO	RO	
Default	0x0		0xX	0xX		0xX	0xX	

Table 5.46 SYS Boot Register

Field Name	Bit	Description
Reserved	[31:6]	Reserved
I2CAdr	[5]	I ² C Slave Address Selection: 0: I ² C Slave Address = "110 1000" 1: I ² C Slave Address = "000 1111"
Reserved	[4:3]	Reserved
DSIRef	[2]	DSI RefClk Source Division Selection (MODE[1] pins status) 0: HSCKBY2 divided by 7 used as RefClk (HSCK assumed = 364 MHz). 1: HSCKBY2 divided by 9 used as RefClk (HSCK assumed = 468 MHz).
ClkSrc[1:0]	[1:0]	PLL_Ref Source Selection (MODE[0] & RefClk pins status) {Mode[0], RefClk} = 2'b0x: Ext REFCLK as clock input for DP PHY PLLs 2'b10: DSI Clock as clock input for DP PHY PLLs 2'b11: DPI Clock as clock input for DP PHY PLLs

5.7.3. SYS Status Register

Mnemonic	SYSSTAT (Address = 0x0508)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved	ERRID						
Type	RO	RO						
Default	0x0	0x00						
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					VCERR	PKTERR	
Type	RO					RO	RO	
Default	0x0					0x0	0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	DP0BUNF	ABOVF	ABUNF	Reserved		VB0OVF	VB0UNF
Type	RO	RO	RO	RO	RO		RO	RO
Default	0x0	0x0	0x0	0x0	0x0		0x0	0x0

Table 5.47 SYS Status Register

Field Name	Bit	Description
Reserved	[31:22]	Reserved
ERRID	[21:16]	Un-Supported Packet ID This field is valid only when PKTERR is asserted
Reserved	[15:10]	Reserved
VCERR	[9]	Un-supported VC number This bit is asserted when receiving DSI Packets with VC field other than 0
PKTERR	[8]	Un-supported DSI Packets This bit is asserted when receiving Un-supported DSI Packets after application layer decodes Packet ID. The unsupported packet ID is reported in the ERRID field in this register.
Reserved	[7]	Reserved
DP0BUNF	[6]	DisplayPort1 Buffer Underflow flag Note: Reading this register will clear this flag
ABOVF	[5]	Audio Buffer Overflow flag Note: Reading this register will clear this flag
ABUNF	[4]	Audio Buffer Underflow flag Note: Reading this register will clear this flag
Reserved	[3:2]	Reserved
VB0OVF	[1]	Video Buffer0 Overflow flag Note: Reading this register will clear this flag
VB0UNF	[0]	Video Buffer0 Underflow flag Note: Reading this register will clear this flag

Note: Read to this register clears all the bits.

5.7.4. SYS_Reset_Enable Register

Mnemonic	SYSRSTENB (Address = 0x050C)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved	Reserved	ENBREG	ENBDSIRX	ENBBM	ENBLCD0	Reserved	ENBI2C	
Type	RW	RO	RW	RW	RW	RW	RW	RW	
Default	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	

Table 5.48 SYS Reset Register

Field Name	Bit	Description
Reserved	[31:9]	Reserved
ENBHDPC	[8]	Enable/Disable for HDCP controller 0: Reset / Disable module (default) 1: Enable module
Reserved	[7]	Reserved
Reserved	[6]	Reserved
ENBREG	[5]	Software reset for Register (REG) module which includes all registers excluding DSI D-PHY, DSI PPI Layer, and DSI Protocol Layer registers 0: Reset / Disable module 1: Enable module (default)
ENBDSIRX	[4]	Software reset for DSI-RX and Application controller 0: Reset / Disable module 1: Enable module (default)
ENBBM	[3]	Software reset for Bus Management (BM) controller 0: Reset / Disable module 1: Enable module (default)
ENBLCD0	[2]	Software reset for LCD controller0 0: Reset / Disable module 1: Enable module (default) Notes: This will also reset Video Line Buffer (VB) for DP0
Reserved	[1]	Reserved

ENBI2C	[0]	Software reset I ² C-Slave controller 0: Reset / Disable module 1: Enable module (default) This bit is meaningful only when written to from DSI link, and is useful only as a chip debugging aide.
--------	-----	--

Note: Enable/Disable controls for PLLs, PHYs and DP modules are in their respective control registers.

5.7.5. SYS Control Register

Mnemonic	SYSCTRL (Address = 0x0510)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved				ExtClkEn	AudOS_Val			
Type	RO				R/W	R/W			
Default	0x0				0x0	0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved				DP0_AudSrc	DP0_VidSrc			
Type	RO				R/W	R/W			
Default	0x0				0x0	0x0			

Table 5.49 SYS Control Register

Register Field	Bit	Default	Description
Reserved	[31:12]	0x0	Reserved
ExtClkEn	[11]	0x0	Selects SD pin to be used as Over-sampling clock input 0: OSCLK not available 1: OSCLK available on SD pin
AudOS_Val	[10:8]	0x0	Relative frequency of audio over-sampling clock 0: 512 x F _{sample} 1: 256 x F _{sample} 2: 128 x F _{sample} 3: 64 x F _{sample} Other: Reserved
Reserved	[7:4]	0x0	Reserved
DP0_AudSrc	[3]	0x0	Source of Audio Stream for DP0 port 0: No Input 1: I2S Rx
DP0_VidSrc	[2:0]	0x0	Source of Video Stream for DP0 port 0: No input 1: DSI Rx 2: DPI Rx 3: Color Bar Other: Reserved

5.7.6. DisplayPort™ Clock Registers

5.7.6.1. DP0_VidMNGen0

Mnemonic	DP0_VIDMNGEN0 (Address = 0x0610)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	force_vid_m								
type	RW								
Default	0x0F								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	force_vid_m								
Type	RW								
Default	0x42								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	force_vid_m								
type	RW								
Default	0x3F								

Table 5.50 DP0_VidMNGen0 Register

Register Field	Bit	Default	Description
Reserved	[31:24]	0x0	Reserved
force_vid_m	[23:0]	0x0	—

5.7.6.2. DP0_VidMNGen1

Mnemonic	DP0_VIDMNGEN1 (Address = 0x0614)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	force_vid_n								
type	RW								
Default	0x62								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	force_vid_n								
Type	RW								
Default	0x17								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	force_vid_n								
type	RW								
Default	0x95								

Table 5.51 DP0_VidMNGen1 Register

Register Field	Bit	Default	Description
Reserved	[31:24]	0x0	Reserved
force_vid_n	[23:0]	0x0	—

5.7.6.3. DP0_VMNGenStatus

Mnemonic	DP0_VMNGENSTATUS (Address = 0x0618)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0xX								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	vid_m								
type	RO_S								
Default	0xX								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	vid_m								
Type	RO_S								
Default	0xX								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	vid_m								
type	RO_S								
Default	0xX								

Table 5.52 DP0_VMNGenStatus Register

Register Field	Bit	Default	Description
Reserved	[31:24]	0x0	Reserved
vid_m	[23:0]	0x0	Current value of Mvid

5.7.6.4. DP0_AudMNGen0

Mnemonic	DP0_AUDMNGEN0 (Address = 0x0628)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	force_aud_m								
Type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	force_aud_m								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	force_aud_m								
Type	RW								
Default	0x0								

Table 5.53 DP0_AudMNGen0 Register

Register Field	Bit	Default	Description
Reserved	[31:24]	0x0	Reserved
force_aud_m	[23:0]	0x0	—

5.7.6.5. DP0_AudMNGen1

Mnemonic	DP0_AUDMNGEN1 (Address = 0x062C)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	force_aud_n								
Type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	force_aud_n								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	force_aud_n								
Type	RW								
Default	0x0								

Table 5.54 DP0_AudMNGen1 Register

Register Field	Bit	Default	Description
Reserved	[31:24]	0x0	Reserved
force_aud_n	[23:0]	0x0	—

5.7.6.6. DP0_AMNGenStatus

Mnemonic	DP0_AMNGENSTATUS (Address = 0x0630)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	aud_m								
type	RO_S								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	aud_m								
Type	RO_S								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	aud_m								
type	RO_S								
Default	0x0								

Table 5.55 DP0_AMNGenStatus Register

Register Field	Bit	Default	Description
Reserved	[31:24]	0x0	Reserved
aud_m	[23:0]	0x0	Current value output of Maud

5.8. I²C Registers

5.8.1. I²C Timing Control and Enable Register

Mnemonic	I2CTIMCTRL (Address = 0x0520)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I2CSCCTL[7:0]							
Type	R/W							
Default	0x80							

Table 5.56 I²C Timing Control and Enable Register

Field Name	Bit	Description
Reserved	[31:8]	Reserved
I2CSCCTL[7:0]	[7:0]	<p>I²C Slave interface SCL clock low control This field is used to define the period between the first valid read data bit on SDA and SCL low to high transition. SCL low period = I2CCLKCTL * I2CCLK. Value 0 is invalid and will result in undefined behaviour.</p>

5.9. GPIO Registers

5.9.1. GPIO Mode Register

Mnemonic	GPIO M (Address = 0x0540)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						GPM[1:0]	
Type	RO						R/W	
Default	0x00						0x0	

Table 5.57 GPIO Control Register

Field Name	Bit	Description
Reserved	[31:2]	Reserved
GPM[1:0]	[1:0]	GPIO function mode control 0: GPIO mode (direction controlled by GPIO Control register) 1: Alternate Function mode (refer pin list for details)

5.9.2. GPIO Control Register

Mnemonic	GPIOC (Address = 0x0544)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved							GPC[1:0]	
Type	RO							R/W	
Default	0x00							0x0	

Table 5.58 GPIO Control Register

Field Name	Bit	Description
Reserved	[31:2]	Reserved
GPC[1:0]	[1:0]	GPIO direction mode control 0: Input mode 1: Output mode

5.9.3. GPIO Output Register

Mnemonic	GPIOO (Address = 0x0548)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						GPO[1:0]	
Type	RO						R/W	
Default	0x00						0x0	

Table 5.59 GPIO Output Register

Field Name	Bit	Description
Reserved	[31:2]	Reserved
GPO[1:0]	[1:0]	GPIO Output data Value of this register will output to the GPIOx pins if the GPIOx select to be in OUTPUT mode

5.9.4. GPIO Input Register

Mnemonic	GPIOI (Address = 0x054C)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							
Type	RO							
Default	0x00							

Table 5.60 GPIO Input Register

Field Name	Bit	Description
Reserved	[31:2]	Reserved
GPI[1:0]	[1:0]	GPIO Input data Value of this register reflects the state of GPIOx pins (after a couple of synchronization clock delays.)

5.10. Interrupt Registers

5.10.1. INTCTL_G Register

Mnemonic	INTCTL_G (Address = 0x0560)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved						SysErr	
Type	RO						R/W	
Default	0x00						0x0	
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				GPIO1_LC	GPIO1_H	Reserved	
Type	RO				R/W	R/W	RO	
Default	0x0				0x0	0x0	0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			HDCP	GPIO0_LC	GPIO0_H	LT0	Aux0
Type	RO			R/W	R/W	R/W	R/W	R/W
Default	0x0			0x0	0x0	0x0	0x0	0x0

Table 5.61 INTCTL_G Control Register

Field Name	Bit	Description
Reserved	[31:17]	Reserved
SysErr	[16]	SYS Status register bits 15 to 0 non zero combined Interrupt Source Enable
Reserved	[15:12]	Reserved
GPIO1_LC	[11]	GPIO1 input toggle H -> L and stay low for low counter time Interrupt Source Enable
GPIO1_H	[10]	GPIO1 input toggle L -> H Interrupt Source Enable
Reserved	[9:5]	Reserved
HDCP_Err	[4]	HDCP Status register bits RxR0NG, BKSVErr, AKSVErr or AUXErr non zero combined Interrupt Source Enable.
GPIO0_LC	[3]	GPIO0 input toggle H -> L and stay low for low counter time Interrupt Source Enable
GPIO0_H	[2]	GPIO0 input toggle L -> H Interrupt Source Enable
LT0	[1]	DP0 Link Training Loop Done (valid only for auto_correct = 1 mode) Interrupt Source Enable
Aux0	[0]	DP0 Aux Channel Access Done Interrupt Source Enable Note: Even timer time out (timer in DP0_AuxCfg1 register) will result in this bit getting set.

5.10.2. INTSTS_G Register

Mnemonic	INTSTS_G (Address = 0x0564)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved						SysErr	
Type	RO						RO	
Default	0x00						0x0	
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				GPIO1_LC	GPIO1_H	Reserved	
Type	RO				R/W1C	R/W1C	RO	
Default	0x0				0x0	0x0	0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			HDCP_Err	GPIO0_LC	GPIO0_H	LT0	Aux0
Type	RO			R/W1C	R/W1C	R/W1C	R/W1C	R/W1C
Default	0x0			0x0	0x0	0x0	0x0	0x0

Table 5.62 INTSTS_G Control Register

Field Name	Bit	Description
Reserved	[31:17]	Reserved
SysErr	[16]	SYS Status register bits 15 to 0 non zero combined Interrupt Source Status
Reserved	[15:12]	Reserved
GPIO1_LC	[11]	GPIO1 input toggle H -> L and stay low for low counter time Interrupt Source Status
GPIO1_H	[10]	GPIO1 input toggle L -> H Interrupt Source Status
Reserved	[9:5]	Reserved
HDCP_Err	[4]	HDCP Status register bits RxR0NG, BKSVErr, AKSVErr or AUXErr non zero combined Interrupt Source Status. Writing 1 to this bit clears only AUXErr bit in HDCPSTAT register
GPIO0_LC	[3]	GPIO0 input toggle H -> L and stay low for low counter time Interrupt Source Status
GPIO0_H	[2]	GPIO0 input toggle Interrupt Source Status
LT0	[1]	DP0 Link Training Loop Done Interrupt Source Status
Aux0	[0]	DP0 Aux Channel Access Done Interrupt Source Status

5.10.3. INT_GPO_LCNT Register

Mnemonic	INTGP0LCNT (Address = 0x0584)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Count[23:16]							
Type	R/W							
Default	0x01							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Count[15:8]							
Type	R/W							
Default	0x3C							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Count[7:0]							
Type	R/W							
Default	0x68							

Table 5.63 INT GPIO0 Low Count Register

Field Name	Bit	Description
Reserved	[31:24]	Reserved
Count	[23:0]	Counter value to be used for GPIO0_LC interrupt source Uses REFCLK for counting. *Setting 0, 1 are prohibited.

5.10.4. INT_GP1_LCNT Register

Mnemonic	INTGP1LCNT (Address = 0x0588)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Count[23:16]							
Type	R/W							
Default	0x01							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Count[15:8]							
Type	R/W							
Default	0x3C							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Count[7:0]							
Type	R/W							
Default	0x68							

Table 5.64 INT GPIO1 Low Count Register

Field Name	Bit	Description
Reserved	[31:24]	Reserved
Count	[23:0]	Counter value to be used for GPIO1_LC interrupt source Uses REFCLK for counting *Setting 0, 1 are prohibited.

5.11. DP – DisplayPort™ Registers

5.11.1. DisplayPort0 Control Registers

5.11.1.1. DP0Ctl

Mnemonic	DP0Ctl (Address = 0x0600)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	aud_mn_gen	vid_mn_gen	ef_en	cp_en	Reserved	aud_en	vid_en	dp_en	
Type	R/W	R/W	R/W	R/W	RO	R/W	R/W	R/W	
Default	0x0	0x1	0x0	0x0	0x0	0x0	0x0	0x0	

Table 5.65 DP0Ctl Register

Register Field	Bit	Default	Description
Reserved	[31:8]	0x0	Reserved
aud_mn_gen	[7]	0x0	<p>This signal enables the generation of M/N values for audio. 0: Internal generation of M/N is disabled. DP0_AudMNGen0 & DP0_AudMNGen1 values are assigned to Maud/Naud respectively. 1: Internal generation of M/N is enabled. DP0_AudMNGen1 gives the reference period in LSCLK cycles over which Maud is to be calculated</p>
vid_mn_gen	[6]	0x1	<p>This signal enables the auto-generation of M/N values for video. 0: Internal generation of M/N is disabled. DP0_VidMNGen0 & DP0_VidMNGen1 values are assigned to Mvid/Nvid respectively. 1: Internal generation of M/N is enabled. DP0_VidMNGen1 gives the reference period in LSCLK cycles over which Mvid is to be calculated</p>
ef_en	[5]	0x0	<p>Enhanced Framing Enable 0: Disable enhanced framing 1: Enable enhanced framing See DisplayPort™ Specification for more description on enhanced framing.</p>
cp_en	[4]	0x0	<p>Content Protection Enable 0: Disable Content Protection 1: Enable Content Protection</p>
Reserved	[3]	0x0	Reserved
aud_en	[2]	0x0	<p>Audio transmission enable Used to enable audio transmission on DP link</p>
vid_en	[1]	0x0	<p>Video transmission enable Used to enable video transmission on DP link</p>
dp_en	[0]	0x0	DPTX function enable as well as Link Training Start

Table 5.66 Effect of dp_en and vid_en controls on DP0 link Register

dp_en	aud_en	vid_en	Description
0	X	X	DPTX will terminate all main link PHY interface transmissions. No new transmissions are initiated on the main link PHY interface.
1	0	0	Main Stream Attribute, InfoFrame, Audio TimeStamp, Video Data and Audio Data packets will not be transmitted.
1	0	1	Main Stream Attribute and Video Data packets will be transmitted. InfoFrame, Audio TimeStamp and Audio Data packets will not be transmitted.
1	1	0	InfoFrame, Audio TimeStamp will be transmitted. Audio Data packets will be transmitted only when Audio data is present on the audio port interface.
1	1	1	Main Stream Attribute, InfoFrame, Audio TimeStamp and Video Data packets will be transmitted. Audio Data packets will be transmitted only when Audio data is present on the audio port interface.

5.11.2. DisplayPort0 Main Channel Registers

5.11.2.1. DP0_SecSample

DPO_SECSAMPLE (Address = 0x0640)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved			v_sec_sample				
type	RO			RW				
Default	0x0			0xF				
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			h_sec_sample				
type	RO			RW				
Default	0x0			0xF				

Table 5.67 DP0_SecSample Register

Register Field	Bit	Default	Description
Reserved	[31:21]	0x0	Reserved
v_sec_sample	[20:16]	0xF	<p>When DPTX is in video enabled mode, this signal defines the maximum number of audio samples that may be sent in one line during vertical blanking time.</p> <p>0-15: Valid values</p> <p>This field is ignored when DisplayPort™ is in video disabled mode.</p>
Reserved	[15:5]	0x0	Reserved
h_sec_sample	[4:0]	0xF	<p>When DPTX is in video enabled mode, this signal defines the maximum number of audio samples that may be sent during horizontal blanking time in the active video region.</p> <p>0-15: Valid values</p> <p>This field is ignored when DisplayPort™ is in video disabled mode.</p>

5.11.2.2. DP0_VidSyncDelay

Mnemonic	DP0_VIDSYNCDELAY (Address = 0x0644)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	thresh_dly								
type	RW								
Default	0xf								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	vid_sync_dly								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	vid_sync_dly								
type	RW								
Default	0xf								

Table 5.68 DP0_VidSyncDelay Register

Register Field	Bit	Default	Description
Reserved	[31:24]	0x0	Reserved
thresh_dly	[23:16]	0xf	<p>This value gives the delay in LSCLK cycles from hync and de to internal hsync and de signals. See vid_sync_dly for more information. The recommended value for thresh_dly is max_tu_symbol as defined in register bits 0x0658[28:23]</p> <p>Note: The maximum valid value is limited to 64</p>
vid_sync_dly	[15:0]	0xf	<p>This value gives the number of STRMCLK cycles from hsync assertion after which a Blanking Start symbol is to send over DP PHY interface during the video blanking region. The recommended value for vid_sync_dly is Hsync width + Horizontal Back Porch + Active line period. Note that the effect delay from hsync assertion to BS symbol on DP PHY is vid_sync_dly x STRMCLK + thresh_dly x LSCLK +/- 2 LSCLK.</p> <p>Note that due to synchronization from STRMCLK and LSCLK domain, Blanking Start symbols may not be sent at the same time and the line period may vary by up to 2 LSCLK.</p>

5.11.2.3. DP0_TotalVal

Mnemonic	DP0_TOTALVAL (Address = 0x0648)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	v_total								
Type	RW								
Default	0x02								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	v_total								
Type	RW								
Default	0x0D								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	h_total								
Type	RW								
Default	0x03								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	h_total								
Type	RW								
Default	0x20								

Table 5.69 DP0_TotalVal Register

Register Field	Bit	Default	Description
v_total	[31:16]	0x020D	Transmitted frame vertical total in number of lines
h_total	[15:0]	0x0320	Transmitted frame horizontal total in number of pixels

5.11.2.4. DP0_StartVal

Mnemonic	DP0_STARTVAL (Address = 0x064C)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	v_start								
Type	RW								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	v_start								
Type	RW								
Default	0x23								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	h_start								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	h_start								
Type	RW								
Default	0x90								

Table 5.70 DP0_StartVal Register

Register Field	Bit	Default	Description
v_start	[31:16]	0x0023	This input provides the start of active video in Frame based on the video timing input to DPTX. This input serves only as valid data to be sent during Main Stream Attribute packet transmission. See DisplayPort™ Specification for more information.
h_start	[15:0]	0x0090	This input provides start of active video in line based on the video timing input to DPTX. This input serves only as valid data to be sent during Main Stream Attribute packet transmission. See DisplayPort™ Specification for more information.

5.11.2.5. DP0_ActiveVal

Mnemonic	DP0_ACTIVEVAL (Address = 0x0650)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	v_act								
Type	RW								
Default	0x01								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	v_act								
Type	RW								
Default	0xE0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	h_act								
Type	RW								
Default	0x02								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	h_act								
Type	RW								
Default	0x80								

Table 5.71 DP0_ActiveVal Register

Register Field	Bit	Default	Description
v_act	[31:16]	0x01E0	This input specifies the number of line in active video for a frame based on the video timing input to DPTX. This input serves only as data to be sent during Main Stream Attribute packet transmission. See DisplayPort™ Specification for more information.
h_act	[15:0]	0x0280	This input specifies the number of pixel in active video for a line based on the video timing input to DPTX. This input serves only as data to be sent during Main Stream Attribute packet transmission. See DisplayPort™ Specification for more information.

5.11.2.6. DP0_SyncVal

Mnemonic	DP0_SYNCVAL (Address = 0x0654)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	vs_pol	vs_width							
Type	RW	RW							
Default	0x1	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	vs_width								
type	RW								
Default	0x02								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	hs_pol	hs_width							
Type	R/W	RW							
Default	0x1	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	hs_width								
type	RW								
Default	0x60								

Table 5.72 DP0_SyncVal Register

Register Field	Bit	Default	Description
vs_pol	[31]	0x1	This input specifies the polarity of vsync input to DPTX and is used to detect hsync edge transitions and to form the Main Stream Attribute packet. 0: Active high 1: Active low
vs_width	[30:16]	0x002	This signal is the Vsync width in number of lines based on the video timing input to DPTX. This input serves only as valid data to be sent during Main Stream Attribute packet transmission. See DisplayPort™ Specification for more information.
hs_pol	[15]	0x1	This input specifies the polarity of hsync input to DPTX and is used to detect hsync edge transitions and to form the Main Stream Attribute packet. 0: Active high 1: Active low
hs_width	[14:0]	0x060	This signal specifies hsync width based on the video timing input to DPTX. This input serves only as valid data to be sent during Main Stream Attribute packet transmission. See DisplayPort™ Specification for more information.

5.11.2.7. DP0_Misc

Mnemonic	DP0_MISC (Address = 0x0658)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved			max_tu_symbol					
Type	RO			RW					
Default	0x0			0x0B					
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	max_tu_symbol	Reserved	tu_size						
type	RW	RO	RW						
Default	0x0	0x0	0x3F						
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved					vid_attr	int_size		
Type	RO					RW	RW		
Default	0x0					0x0	0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	bpc			clrmtry	dyn	fmt	sync_m		
type	RW			RW	RW	RW	RW		
Default	0x0			0x0	0x0	0x0	0x0		

Table 5.73 DP0_Misc Register

Register Field	Bit	Default	Description
Reserved	[31:29]	0x0	Reserved
max_tu_symbol	[28:23]	0x16	<p>This value gives the maximum number of symbols that may be transferred in a transfer unit. The last transfer unit may have number of symbols less than max_tu_symbol. The effective number of symbols that will be transmitted in on transfer unit is max_tu_symbol + 1. The recommended value for max_tu_symbol is roundup ((input active video bandwidth in bytes/output active video bandwidth in bytes) x tu_size).</p> <p>0-62: valid all other values: reserved</p> <p>Note that max_tu_symbol will always be less than tu_size.</p>
Reserved	[22]	0x0	Reserved
tu_size	[21:16]	0x3F	<p>This value determines the number of LSCLK cycles that make one transfer unit. The recommended value for tu_size is 63.</p> <p>The number of LSCLK cycles that is needed to send one active line is then given as the following,</p> <p>rounddown (number of bytes per active line/tu_size) * tu_size + [number of bytes per active line – rounddown(number of bytes per active line/tu_size) * tu_size]</p> <p>Where rounddown () returns the closest integer after rounding down.</p> <p>31-63: valid all other values: reserved</p>
Reserved	[15:11]	0x0	Reserved
vid_attr	[10:9]	0x0	-

int_size	[8]	0x0	This input serves only as a valid data to be sent during Main Stream Attribute packet transmission. See DisplayPort™ Specification for more information.
bpc	[7:5]	0x0	<p>This input defines the number of bits per color component of output video data.</p> <p>000: 6 001: 8 others: (not supported)</p> <p>This input is used in DPTX for packing parallel data as per DisplayPort™ specification and is also used for generating Main Stream Attribute packets. See DisplayPort™ Specification for more information.</p>
clrmtry	[4]	0x0	This input serves only as a valid data to be sent during Main Stream Attribute packet transmission. See DisplayPort™ Specification for more information.
dyn	[3]	0x0	This signal specifies the valid range of pixel data. This input serves only as a valid data to be sent during Main Stream Attribute packet transmission. See DisplayPort™ Specification for more information.
fmt	[2:1]	0x0	<p>This field indicates the type of data input to DPTX. This field is used to determine the packing order and to form the main stream attribute packet.</p> <p>00: RGB 01: YCbCr (4:2:2) 10: YCbCr (4:4:4) Others: reserved</p>
sync_m	[0]	0x0	<p>This signal is set to specify the clock relationship between LSCLK and STRMCLK.</p> <p>This input serves only as data to be sent during Main Stream Attribute packet transmission. See DisplayPort™ Specification for more information.</p>

5.11.3. DisplayPort0 AUX Channel Registers

5.11.3.1. DP0_AuxCfg0

DP0_AUXCFG0 (Address = 0x0660)									
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved				bsize				
Type	RO				RW				
Default	0x0				0x0				
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved			addr_only	cmd				
Type	RO			RW	RW				
Default	0x0			0x0	0x0				

Table 5.74 DP0_AuxCfg0 Register

Register Field	Bit	Default	Description
Reserved	[31:12]	0x0	Reserved
bsize	[11:8]	0x0	Number of bytes requested for the AUX channel transaction. Maximum of 16 bytes may be requested in a single transaction. 0-15: valid values This field is ignored when addr_only bit is set.
Reserved	[7:5]	0x0	Reserved
addr_only	[4]	0x0	If set, Aux channel transaction stops after the AUX transaction address phase i.e., the burst size is not transmitted over the Aux channel. "bsize" value is ignored when this is set.
cmd	[3:0]	0x0	AUX command to be transmitted during an AUX transaction. 4'b1000: AUX native write transaction 4'b1001: AUX native read transaction 4'b0000: I ² C write transaction 4'b0100: I ² C write transaction (middle of transaction) 4'b0001: I ² C read transaction 4'b0101: I ² C read transaction (middle of transaction) 4'b0010: I ² C status request 4'b0110: I ² C status request (middle of transaction) All others: reserved

5.11.3.2. DP0_AuxCfg1

Mnemonic	DP0_AUXCFG1 (Address = 0x0664)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved								
Type	RO								
Default	0x0								

Table 5.75 DP0_AuxCfg1 Register

Register Field	Bit	Default	Description
Reserved	[31:17]	0x0	Reserved
FilterEn	[16]	0x1	Aux Rx Filter Enable Aux Receiver ignores any pulses smaller than 1 UI on AUX channel 0: Disable filter (all transitions received) 1: Enable filter (default)
Reserved	[15:12]	0x0	Reserved
Threshold	[11:8]	0x7	Aux Bit Period Calculator Threshold Provides a period (value * 100 ns) for which subsequent transitions on AUX data lines from a reference transition are ignored. The time period between the transition after value * 100 ns and the reference transition is used to calculate the AUX bit period.
Reserved	[7:6]	0x0	Reserved
Timer	[5:0]	0x32	Aux Response Timeout Timer Timer used to track time between two Aux request transactions. <ul style="list-style-type: none"> - Uses byte clock derived from Aux clock for counting @125 kHz. - Value used for counting is double the one programmed here. - Timer starts counting when the “aux_stop” is sent over the Aux I/F while TC358867XBG is in “Talk” mode on Aux interface. - Timer resets on the first valid data byte returned over the PHY. - If the counter expires before any response from the Sink is received, TC358867XBG will retry the transaction before setting aux_timeout. - Any response from PHY after a timeout will result in undefined behavior.

5.11.3.3. DP0_AuxAddr

DP0_AUXADDR (Address = 0x0668)									
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved				addr				
type	R/W				R/W				
Default	0x0				0x0				
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	addr				R/W				
Type	R/W				0x0				
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	addr				R/W				
type	R/W				0x0				
Default									

Table 5.76 DP0_AuxAddr Register

Register Field	Bit	Default	Description
Reserved	[31:20]	0x0	Reserved
addr	[19:0]	0x0	20 bit address that is to be transmitted over the AUX interface. In case of I ² C transactions, only bit [6:0] are valid with I ² C slave address. Bits[19:7] are set to 0 when performing I ² C transactions.

5.11.3.4. DP0_AuxWData0

DP0_AUXWDATA0 (Address = 0x066C)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	aux_wdata0							
Type	R/W							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	aux_wdata0							
Type	R/W							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	aux_wdata0							
Type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aux_wdata0							
type	R/W							
Default	0x0							

Table 5.77 DP0_AuxWData0 Register

Register Field	Bit	Default	Description
aux_wdata0	[31:0]	0x0	This is the 8 bit formatted data that will be transmitted over the AUX channel. Data within the 8 bits bus is formatted such that the PHY needs to only shift the 8 bit data with the most significant bit out first and least significant bit last.

5.11.3.5. DP0_AuxWData1

DP0_AUXWDATA1 (Address = 0x0670)								
Mnemonic	B31	B30	B29	B28	B27	B26	B25	B24
Name	aux_wdata1							
Type	R/W							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	aux_wdata1							
type	R/W							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	aux_wdata1							
type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aux_wdata1							
type	R/W							
Default	0x0							

Table 5.78 DP0_AuxWData1 Register

Register Field	Bit	Default	Description
aux_wdata1	[31:0]	0x0	—

5.11.3.6. DP0_AuxWData2

DP0_AUXWDATA2 (Address = 0x0674)								
Mnemonic	B31	B30	B29	B28	B27	B26	B25	B24
Name	aux_wdata2							
Type	R/W							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	aux_wdata2							
type	R/W							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	aux_wdata2							
Type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aux_wdata2							
type	R/W							
Default	0x0							

Table 5.79 DP0_AuxWData2 Register

Register Field	Bit	Default	Description
aux_wdata2	[31:0]	0x0	—

5.11.3.7. DP0_AuxWData3

Mnemonic	DP0_AUXWDATA3 (Address = 0x0678)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	aux_wdata3							
Type	R/W							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	aux_wdata3							
Type	R/W							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	aux_wdata3							
Type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aux_wdata3							
Type	R/W							
Default	0x0							

Table 5.80 DP0_AuxWData3 Register

Register Field	Bit	Default	Description
aux_wdata3	[31:0]	0x0	—

5.11.3.8. DP0_AuxRData0

Mnemonic	DP0_AUXRDATA0 (Address = 0x067C)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	aux_rdata0							
Type	RO_S							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	aux_rdata0							
Type	RO_S							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	aux_rdata0							
Type	RO_S							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aux_rdata0							
Type	RO_S							
Default	0x0							

Table 5.81 DP0_AuxRData0 Register

Register Field	Bit	Default	Description
aux_rdata0	[31:0]	0x0	Data received by the PHY over the AUX channel when the PHY is in “Listen mode”. Data is packed such that the first bit received is treated as the most significant bit of the byte.

5.11.3.9. DP0_AuxRData1

Mnemonic	DP0_AUXRDATA1 (Address = 0x0680)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	aux_rdata1							
Type	RO_S							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	aux_rdata1							
Type	RO_S							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	aux_rdata1							
Type	RO_S							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aux_rdata1							
Type	RO_S							
Default	0x0							

Table 5.82 DP0_AuxRData1 Register

Register Field	Bit	Default	Description
aux_rdata1	[31:0]	0x0	—

5.11.3.10. DP0_AuxRData2

Mnemonic	DP0_AUXRDATA2 (Address = 0x0684)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	aux_rdata2							
Type	RO_S							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	aux_rdata2							
Type	RO_S							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	aux_rdata2							
Type	RO_S							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aux_rdata2							
Type	RO_S							
Default	0x0							

Table 5.83 DP0_AuxRData2 Register

Register Field	Bit	Default	Description
aux_rdata2	[31:0]	0x0	—

5.11.3.11. DP0_AuxRData3

DP0_AUXRDATA3 (Address = 0x0688)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	aux_rdata3							
Type	RO_S							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	aux_rdata3							
Type	RO_S							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	aux_rdata3							
Type	RO_S							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aux_rdata3							
Type	RO_S							
Default	0x0							

Table 5.84 DP0_AuxRData3 Register

Register Field	Bit	Default	Description
aux_rdata3	[31:0]	0x0	—

5.11.3.12. DP0_AuxStatus

Mnemonic	DP0_AUXSTATUS (Address = 0x068C)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved	retry		Reserved	Err_Align	Err_Stop	Err_Sync	
Type	RO	RO_S		RO	RO_S	RO_S	RO_S	
Default	0x0	0x0		0x0	0x0	0x0	0x0	
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	aux_bytes							
Type	RO_S							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aux_status			Reserved	aux_timeout		aux_busy	
type	RO_S			RO	RO_S		RO_S	
Default	0x0			0x0	0x0		0x0	

Table 5.85 DP0_AuxStatus Register

Register Field	Bit	Default	Description
Reserved	[31:23]	0x0	Reserved
retry	[22:20]	0x0	Indicates the number of attempts DPTX made to complete the current transaction over auxiliary channel when the aux transaction ends with a no reply.
Reserved	[19]	0x0	Reserved
Err_Align	[18]	0x0	AUX data received was not aligned to byte boundaries.
Err_Stop	[17]	0x0	AUX data received ended with an illegal stop sequence.
Err_Sync	[16]	0x0	AUX data could not be synced with current Threshold value in DP0_AuxCfg1 register.
aux_bytes	[15:8]	0x0	<p>For AUX native Transactions</p> <p>Write requests:</p> <p>When aux_status = 4'bxx01, aux_bytes has the number of bytes that was successfully written by the DP sink</p> <p>Read requests:</p> <p>When aux_status = 4'bxx00, aux_bytes has the number of bytes returned by the DP sink following the response byte.</p> <p>For I²C over AUX transactions</p> <p>Write requests:</p> <p>When aux_status = 4'b0000 or 4'b0100, aux_bytes has the number of bytes that were successfully written to the I²C slave.</p> <p>In the case when aux_status = 4'b0100 for the I²C Address phase, aux_bytes is to be ignored.</p> <p>Read requests:</p> <p>When aux_status = 4'b0000, aux_bytes has the number of bytes returned by the DP sink following the response byte.</p> <p>aux_bytes shall be ignored for all states of aux_status not specified in the description above.</p>

aux_status	[7:4]	0x0	<p>This bus is the response returned by the DP sink to the AUX transaction. The status is valid only after busy is de-asserted. When cmd[3] is 1'b0.</p> <p>4'b0000: I²C ACK 4'b0100: I²C NACK 4'b1000: I²C DEFER</p> <p>When cmd[3] is 1'b1.</p> <p>4'b xx00: AUX ACK 4'b xx01: AUX NACK 4'b xx10: AUX DEFER all others: not valid</p>
Reserved	[3:2]	0x0	Reserved
aux_timeout	[1]	0x0	If the DP0_AuxCfg1.timer expires before any response from the Sink is received, TC358867XBG will retry the transaction for retry count (max 3) attempts before setting this bit.
aux_busy	[0]	0x0	This bit is asserted when TC358867XBG is not actively transmitting/receiving any transaction.

5.11.3.13. DP0_AuxI2CAdr

DP0_AUXI2CADR (Address = 0x0698)								
Mnemonic	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	i2c_adr						
Type	RO	R/W						
Default	0x0	0x0						

Table 5.86 DP0_AuxI2CAdr Register

Register Field	Bit	Default	Description
Reserved	[31:7]	0x0	Reserved
i2c_adr	[6:0]	0x0	I ² C address register If the incoming I ² C address matches this address, the transaction is mapped over DisplayPort TM Aux channel and sent to the DP Sink

5.11.4. DisplayPort0 Link Training Control & Status Registers

5.11.4.1. DP0_SrcCtrl Register

Mnemonic	DP0_SRCCTRL (Address = 0x06A0)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved		Pre1		Reserved		Swg1	
Type	RO		R/W		RO		R/W	
Default	0x0		0x00		0x0		0x00	
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved		Pre0		Reserved		Swg0	
Type	RO		R/W		RO		R/W	
Default	0x0		0x00		0x0		0x0	
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved		SCRMBL	EN810B	Reserved		TrainPat	
Type	RO		R/W	R/W	RO		R/W	
Default	0x0		0x1	0x1	0x0		0x00	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Lane_skew	Reserved			SSCG	Lanes	BW	AutoCorrect
Type	RW	RO			R/W	R/W	R/W	R/W
Default	0x1	0x0			0x0	0x0	0x0	0x0

Table 5.87 DP0_SrcCtrl Register

Field Name	Bit	Description
Reserved	[31:30]	Reserved
Pre1	[29:28]	Pre-Emphasis Settings for DisplayPort™ Port1 0x0: No Pre-emphasis (0 dB) 0x1: 3.5 dB pre-emphasis 0x2: 6 dB pre-emphasis others: Reserved
Reserved	[27:26]	Reserved
Swg1	[25:24]	Voltage Swing Settings for DisplayPort™ Port1 0x0: 0.4V Vdiff_pp (default) 0x1: 0.6V Vdiff_pp 0x2: 0.8V Vdiff_pp 0x3: 1.2V Vdiff_pp
Reserved	[23:22]	Reserved
Pre0	[21:20]	Pre-Emphasis Settings for DisplayPort™ Port0 0x0: No Pre-emphasis (0 dB) 0x1: 3.5 dB pre-emphasis 0x2: 6 dB pre-emphasis others: Reserved
Reserved	[19:18]	Reserved

Swg0	[17:16]	Voltage Swing Settings for DisplayPort™ Port0 0x0: 0.4V Vdiff_pp (default) 0x1: 0.6V Vdiff_pp 0x2: 0.8V Vdiff_pp 0x3: 1.2V Vdiff_pp
Reserved	[15:14]	Reserved
SCRMBL	[13]	Scrambler Disabled 0: Scrambler Enabled 1: Scrambler Disabled
EN810B	[12]	Enable for 8/10B Encoder in DP PHY 0: Disable 8/10B Encoder 1: Enable 8/10B Encoder (TxData[19:16] not used)
Reserved	[11:10]	Reserved
TrainPat	[9:8]	Link Training Pattern to be sent 00 – Training not in progress (or disabled) 01 – Training Pattern 1 10 – Training Pattern 2 11 – Use pattern programmed in TPatDat0 to TPatDat3
Lane_skew	[7]	This bit selects if data between lane 0 and lane 1 is to be skewed by 2 LSCLK cycles. 0: no skew 1: skew lane 1 data by two LSCLK cycles with respect to lane 0 data.
Reserved	[6:4]	Reserved
SSCG	[3]	Spread Spectrum Enable 0: Spread Spectrum Disabled (default) 1: Spread Spectrum Enabled
Lanes	[2]	Number of Main Channel Lanes in DisplayPort™ Link 0: Single Main Channel Lane 1: Two Main Channel Lanes
BW	[1]	Link Bandwidth Setting: 0: 1.62 Gbps link 1: 2.7 Gbps link (default)
AutoCorrect	[0]	AutoCorrect Mode Host interference not needed to re-adjust Link parameters for next Link Training Loop 0: Host needs to adjust settings for each Training Loop (default) 1: Host sets initial settings and then waits for completion of link training (all loops done)

5.11.4.2. DP0_LTStat Register

Mnemonic	DP0_LTSTAT (Address = 0x06D0)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved		LoopDone	Status					
Type	RO		RO	RO					
Default	0x0		0x1	0x0					
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved	SymLck1	EQDone1	CRDone1	ILAlign	SymLck0	EQDone0	CRDone0	
Type	RO	RO	RO	RO	RO	RO	RO	RO	
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	

Table 5.88 DP0_LTStat Register

Field Name	Bit	Description
Reserved	[31:14]	Reserved
LoopDone	[13]	Loop Done (valid only for auto_correct = 1 mode) 0: Link Training Loop not done 1: Link Training Loop done (default)
Status	[12:8]	Link Training Status (valid only for auto_correct = 1 mode) Status[4:3]: 2'b1: Pattern1 Status in Status[2:0] 2'b2: Pattern2 Status in Status[2:0] Others: Reserved Status[2:0]: Pattern1 Error Codes 3'b0: No errors 3'b1: Aux write error 3'b2: Aux read error 3'b3: Max voltage reached error 3'b4: Loop counter expired error (same voltage returned for loop iter count) Others: Reserved Status[2:0]: Pattern2 Error Codes 3'b0: No errors 3'b1: Aux write error 3'b2: Aux read error 3'b3: Clock recovery failed error 3'b4: Loop counter expired error Others: Reserved

Reserved	[7]	Reserved
SymLck1	[6]	Lane1 Symbol Locked (valid only for auto_correct = 1 mode) 0: Symbol not Locked. 1: Symbol Locked.
EQDone1	[5]	Lane1 Channel EQ Done (valid only for auto_correct = 1 mode) 0: EQ not Done. 1: EQ Done.
CRDone1	[4]	Lane1 CR Done (valid only for auto_correct = 1 mode) 0: CR not Done. 1: CR Done.
ILAlign	[3]	Inter-lane align done (valid only for auto_correct = 1 mode) 0: Inter-lane align not Done. 1: Inter-lane align Done.
SymLck0	[2]	Lane0 Symbol Locked (valid only for auto_correct = 1 mode) 0: Symbol not Locked. 1: Symbol Locked.
EQDone0	[1]	Lane0 Channel EQ Done (valid only for auto_correct = 1 mode) 0: EQ not Done. 1: EQ Done.
CRDone0	[0]	Lane0 CR Done (valid only for auto_correct = 1 mode) 0: CR not Done. 1: CR Done.

5.11.4.3. DP0_SnkLTChReq Register

Mnemonic	DP0_SNKLTCHGREQ (Address = 0x06D4)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x00								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved								
Type	RO								
Default	0x00								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	RO								
Default	0x00								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	PreAmp1	Swng1		PreAmp0		Swng0			
Type	RO	RO		RO		RO			
Default	0x0	0x0		0x0		0x0			

Table 5.89 DP0_SnkLTChgReq Register

Field Name	Bit	Description
Reserved	[31:8]	Reserved
PreAmp1	[7:6]	Pre-Emphasis Setting Request for Lane1 Refer DisplayPort™ Specification.
Swng1	[5:4]	Voltage Swing Setting Request for Lane1 Refer DisplayPort™ Specification.
PreAmp0	[3:2]	Pre-Emphasis Setting Request for Lane0 Refer DisplayPort™ Specification.
Swng0	[1:0]	Voltage Swing Setting Request for Lane0 Refer DisplayPort™ Specification.

5.11.4.4. DP0_LTLoopCtrl Register

Mnemonic	DP0_LTLOOPCTRL (Address = 0x06D8)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Deferlter					Looplter			
Type	R/W					R/W			
Default	0x7					0x5			
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved								
Type	RO								
Default	0x00								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	LoopTimer[15:8]								
Type	R/W								
Default	0x00								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	LoopTimer[7:0]								
Type	R/W								
Default	0x00								

Table 5.90 DP0_SnkLTLoopCtrl Register

Field Name	Bit	Description
Deferlter	[31:28]	Defer Iteration Count (valid only for auto_correct = 1 mode) Number of times TC358867XBG will retry current link training loop in case of "DEFER" response from the sink.
Looplter	[27:24]	Loop Iteration Count (valid only for auto_correct = 1 mode) Starting value for Loop Iteration Counter. Refer Link Training Section for details on decrement/reset usage of this counter.
Reserved	[23:16]	Reserved
LoopTimer	[15:0]	Loop Timer Delay Loop Timer Counter used as delay before reading Link Training loop status from Sink. Value programmed here is divided by 4 for use during Link Training Pattern1 loops. Value programmed here is used as it is during Link Training Pattern2 loop. Loop Counter uses LSCLK for counting.

5.11.4.5. DP0_SnkLTCtrl

Mnemonic	DP0_SNKLTCtrl (Address = 0x06E4)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
type	RO								
Default	0x00								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved								
type	RO								
Default	0x00								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	RO								
Default	0x00								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	SnkLTCfg								
Type	RW								
Default	0x00								

Table 5.91 DP0_SnkLTCtrl Register

Register Field	Bit	Default	Description
Reserved	[31:8]	0x0	Reserved
SnkLTCfg	[7:0]	0x0	Data to be written to Sink Link Training Control register. Refer DisplayPort™ Specification.

5.11.4.6. DP0_TPATDAT0

Mnemonic	DP0_TPATDAT0 (Address = 0x06E8)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	LoopCtrl		tpat_data0						
Type	RW		RW						
Default	0x0		0x0						
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name			tpat_data0						
Type			RW						
Default			0x0						
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name			tpat_data0						
Type			RW						
Default			0x0						
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name			tpat_data0						
Type			RW						
Default			0x0						

Table 5.92 DP0_TPATDAT0 Register

Register Field	Bit	Default	Description
LoopCtrl	[31:30]	0x0	<p>Training Pattern Loop Control</p> <p>Controls the last symbol of the training pattern loop</p> <p>0: Symbol 0 [bits 9:0] is the last symbol of the loop</p> <p>1: Symbol 0 [bits 19:10] is the last symbol of the loop</p> <p>2: Symbol 0 [bits 29:20] is the last symbol of the loop</p> <p>3: Last symbol of the loop in next TPatDat register</p>
tpat_data0	[29:0]	0x0	Test Pat bits 29 to 0

5.11.4.7. DP0_TPATDAT1

Mnemonic	DP0_TPATDAT1 (Address = 0x06EC)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	LoopCtrl								
Type	RW								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	tpat_data1								
Type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	tpat_data1								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	tpat_data1								
type	RW								
Default	0x0								

Table 5.93 DP0_TPATDAT1 Register

Register Field	Bit	Default	Description
LoopCtrl	[31:30]	0x0	Training Pattern Loop Control Controls the last symbol of the training pattern loop 0: Symbol 0 [bits 9:0] is the last symbol of the loop 1: Symbol 0 [bits 19:10] is the last symbol of the loop 2: Symbol 0 [bits 29:20] is the last symbol of the loop 3: Last symbol of the loop in next TPATDAT register
tpat_data1	[29:0]	0x0	Test Pattern bits 59 to 30

5.11.4.8. DP0_TPATDAT2

Mnemonic	DP0_TPATDAT2 (Address = 0x06F0)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	LoopCtrl								tpat_data2
Type	RW								RW
Default	0x0								0x0
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	tpat_data2								
type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	tpat_data2								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	tpat_data2								
type	RW								
Default	0x0								

Table 5.94 DP0_TPATDAT2 Register

Register Field	Bit	Default	Description
LoopCtrl	[31:30]	0x0	<p>Training Pattern Loop Control</p> <p>Controls the last symbol of the training pattern loop</p> <p>0: Symbol 0 [bits 9:0] is the last symbol of the loop</p> <p>1: Symbol 0 [bits 19:10] is the last symbol of the loop</p> <p>2: Symbol 0 [bits 29:20] is the last symbol of the loop</p> <p>3: Last symbol of the loop in next TPATDAT register</p>
tpat_data2	[29:0]	0x0	Test Pattern bits 89 to 60

5.11.4.9. DP0_TPATDAT3

Mnemonic	DP0_TPATDAT3 (Address = 0x06F4)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	LoopCtrl								
Type	RW								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	tpat_data3								
Type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	tpat_data3								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	tpat_data3								
Type	RW								
Default	0x0								

Table 5.95 DP0_TPATDAT3 Register

Register Field	Bit	Default	Description
LoopCtrl	[31:30]	0x0	Training Pattern Loop Control Controls the last symbol of the training pattern loop 0: Symbol 0 [bits 9:0] is the last symbol of the loop 1: Symbol 0 [bits 19:10] is the last symbol of the loop 2: Symbol 0 [bits 29:20] is the last symbol of the loop 3: Reserved
tpat_data3	[29:0]	0x0	Test Pattern bits 119 to 90

5.11.5. DisplayPort™ Audio Registers

5.11.5.1. AudCfg0

Mnemonic	AUDCFG0 (Address = 0x0700)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							aud_mute
Type	RO							R/W
Default	0x00							0x0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
type	R/O							
Default	0x00							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							aud_num_ch
Type	RO							R/W
Default	0x0							0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aud_pkt_id							
type	RW							
Default	0x0							

Table 5.96 AudCfg0 Register

Register Field	Bit	Default	Description
Reserved	[31:25]	0x0	Reserved
aud_mute	[24]	0x0	Audio Muting Control
Reserved	[23:9]	0x0	Reserved
aud_num_ch	[8]	0x0	Number of audio channels per sample Number of audio channels = aud_num_ch +1.
aud_pkt_id	[7:0]	0x0	This provides the audio packet id to be transmitted with the secondary packet headers byte for Audio Info Frame packet, Audio Time Stamp packet and Audio Data Stream packets. (Same packet Id to be used for 3 different kind of packets). Refer to DisplayPort™ Specification for more information on packet id.

5.11.5.2. AudCfg1

AUDCFG1 (Address = 0x0704)								
Mnemonic	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
type	RO							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aud_if_type							
type	RW							
Default	0x0							

Table 5.97 AudCfg1 Register

Register Field	Bit	Default	Description
Reserved	[31:8]	0x0	Reserved
aud_if_type	[7:0]	0x0	This provides the info Frame Type Value to be transmitted with the secondary packet header. Refer to DisplayPort™ specification for more information.

5.11.5.3. AudIFData0

AUDIFDATA0 (Address = 0x0708)								
Mnemonic	B31	B30	B29	B28	B27	B26	B25	B24
Name	aud_if_data0							
Type	RW							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	aud_if_data0							
type	RW							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	aud_if_data0							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aud_if_data0							
type	RW							
Default	0x0							

Table 5.98 AudIFData0 Register

Register Field	Bit	Default	Description
aud_if_data0	[31:0]	0x0	Data to be transmitted in the info Frame secondary packet. Refer to DisplayPort™ specification for more information. aud_if_data0 is sent first in the data set.

5.11.5.4. AudiFData1

Mnemonic	AUDIFDATA1 (Address = 0x070C)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	aud_if_data1							
Type	RW							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	aud_if_data1							
Type	RW							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	aud_if_data1							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aud_if_data1							
Type	RW							
Default	0x0							

Table 5.99 AudiFData1 Register

Register Field	Bit	Default	Description
aud_if_data1	[31:0]	0x0	—

5.11.5.5. AudiFData2

Mnemonic	AUDIFDATA2 (Address = 0x0710)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	aud_if_data2							
Type	RW							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	aud_if_data2							
Type	RW							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	aud_if_data2							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aud_if_data2							
Type	RW							
Default	0x0							

Table 5.100 AudiFData2 Register

Register Field	Bit	Default	Description
aud_if_data2	[31:0]	0x0	—

5.11.5.6. AudIFData3

AUDIFDATA3 (Address = 0x0714)								
Mnemonic	B31	B30	B29	B28	B27	B26	B25	B24
Name	aud_if_data3							
Type	RW							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	aud_if_data3							
type	RW							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	aud_if_data3							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aud_if_data3							
type	RW							
Default	0x0							

Table 5.101 AudIFData3 Register

Register Field	Bit	Default	Description
aud_if_data3	[31:0]	0x0	—

5.11.5.7. AudIFData4

AUDIFDATA4 (Address = 0x0718)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	aud_if_data4							
Type	RW							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	aud_if_data4							
type	RW							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	aud_if_data4							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aud_if_data4							
type	RW							
Default	0x0							

Table 5.102 AudIFData4 Register

Register Field	Bit	Default	Description
aud_if_data4	[31:0]	0x0	—

5.11.5.8. AudIFData5

Mnemonic	AUDIFDATA5 (Address = 0x071C)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	aud_if_data5								
Type	RW								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	aud_if_data5								
type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	aud_if_data5								
type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	aud_if_data5								
type	RW								
Default	0x0								

Table 5.103 AudIFData5 Register

Register Field	Bit	Default	Description
aud_if_data5	[31:0]	0x0	—

5.11.5.9. AudIFData6

Mnemonic	AUDIFDATA6 (Address = 0x0720)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	aud_if_data6								
Type	RW								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	aud_if_data6								
type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	aud_if_data6								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	aud_if_data6								
type	RW								
Default	0x0								

Table 5.104 AudIFData6 Register

Register Field	Bit	Default	Description
aud_if_data6	[31:0]	0x0	—

5.11.6. DisplayPort™ PHY Registers

5.11.6.1. DP_PHY_Ctrl Register

Mnemonic	DP_PHY_CTRL (Address = 0x0800)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved			DP_PHY_Rst	Reserved		BGREN	Pwr_Sw_En
Type	RO			R/W	RO		R/W	R/W
Default	0x0			0x0	0x0		0x1	0x1
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							PHY_Rdy
Type	RO							RO
Default	0x0							0xX
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved			PHY_M1_Rst	Reserved			PHY_M0_Rst
Type	RO			R/W	RO			R/W
Default	0x0			0x0	0x0			0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			PHY_M1_En	Reserved	Reserved	PHY_A0_En	PHY_M0_En
Type	RO			R/W	RO	R/W	R/W	R/W
Default	0x0			0x0	0x0	0x1	0x0	0x0

Table 5.105 DP_PHY_Ctrl Register

Field Name	Bit	Description
Reserved	[31:29]	Reserved
DP_PHY_Rst	[28]	DP PHY Global Soft Reset Controls the global reset to DP PHY modules including Tx0, Tx1, PLL0, PLL1, PMTM and associated circuits 0: Normal Operation 1: Reset
Reserved	[27:26]	Reserved
BGREN	[25]	AUX PHY BGR Enable 0: Disabled 1: Enabled (default)
Pwr_Sw_En	[24]	PHY Power Switch Enable Controls the power for Tx0 & Tx1 drivers, PLL0 & PLL1 and associated circuits 0: Power disabled 1: Power Enabled
Reserved	[23:17]	Reserved
PHY_Rdy	[16]	PHY Main Channels Ready Status 0: Main Channels not ready (not enabled or auto-calibrating) 1: Main Channels ready for Link Training/Main Tx
Reserved	[15:13]	Reserved

PHY_M1_Rst	[12]	PHY Main Channel1 Reset This is a level active bit. 0: Normal operation 1: Reset DP PHY1 Main Channel
Reserved	[11:9]	Reserved
PHY_M0_Rst	[8]	PHY Main Channel0 Reset This is a level active bit. 0: Normal operation 1: Reset DP PHY0 Main Channel
Reserved	[7:5]	Reserved
PHY_M1_En	[4]	PHY Main Channel1 Enable 0: Disabled (default) 1: Enabled
Reserved	[3:2]	Reserved
PHY_A0_En	[1]	PHY Aux Channel0 Enable 0: Disabled (default) 1: Enabled
PHY_M0_En	[0]	PHY Main Channel0 Enable 0: Disabled (default) 1: Enabled

5.11.6.2. DP_PHY_CFG_WR Register

0x0810 is DP_PHY_CFG_WR test register. Don't access the register.
Keep default value.

5.11.6.3. DP_PHY_CFG_RD Register

0x0814 is DP_PHY_CFG_RD test register. Don't access the register.
Keep default value.

5.11.6.4. DP0_AUX_PHY_Ctrl Register

Mnemonic	DP0_AUX_PHY_CTRL (Address = 0x0820)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved						HSEN		
Type	RO						R/W		
Default	0x0						0x1		

Table 5.106 DP0_AUX_PHY_Ctrl Register

Field Name	Bit	Description
Reserved	[31:2]	Reserved
HSEN	[1:0]	High Swing Enable for Aux PHY Drivers 00: Low swing (610 mV Vdiffp_p) 01: Normal swing (730 mV Vdiffp_p) (Default) 10: High swing (950 mV Vdiffp_p) 11: High swing (1050 mV Vdiffp_p)

5.11.6.5. DP0_Main_PHY_Db Debug Register

0x0840 is DP0_MAIN_PHY_DBG test register. Don't access the register.

Keep default value.

5.12. I2S Registers

5.12.1. I2SCfg

Mnemonic	I2SCFG (Address = 0x0880)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
type	R/O							
Default	0x00							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	aud_sample_width				Reserved	Valid	IEC60958_En	Audio_En
type	R/W				RO	R/W	R/W	R/W
Default	0x0				0x0	0x0	0x0	0x0

Table 5.107 I2SCfg Register

Register Field	Bit	Default	Description
Reserved	[31:10]	0x0	Reserved
Align	[9:8]	0x0	Audio bits alignment within sample slot 0: Standard 1: Left Justified 2: Right Justified Others: Reserved
Aud_Sample_Width	[7:4]	0x0	Audio sample width (per channel) in bits Width of audio sample = aud_sample_width + 16. Valid values: 0, 2, 4 or 8 Others: Reserved
Reserved	[3]	0x0	Reserved
Valid	[2]	0x0	Validity bit to be used for IEC60958-like framing
IEC60958_En	[1]	0x0	IEC60958-like control bits generation Enable
Audio_En	[0]	0x0	Audio Input Enable – start of 192 frames clock

5.12.2. I2SCH0Stat0

Mnemonic	I2SCH0STAT0 (Address = 0x0888)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	i2s_ch_stat0								
Type	RW								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	i2s_ch_stat0								
type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	i2s_ch_stat0								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	i2s_ch_stat0								
type	RW								
Default	0x0								

Table 5.108 I2SCH0STAT0 Register

Register Field	Bit	Default	Description
i2s_ch_stat0	[31:0]	0x0	This provides the bits 31 to 0 of the 192 bit channel status.

5.12.3. I2SCH0Stat1

Mnemonic	I2SCH0STAT1 (Address = 0x088C)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	i2s_ch_stat1								
Type	RW								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	i2s_ch_stat1								
type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	i2s_ch_stat1								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	i2s_ch_stat1								
type	RW								
Default	0x0								

Table 5.109 I2SCH0STAT1 Register

Register Field	Bit	Default	Description
i2s_ch_stat1	[31:0]	0x0	This provides the bits 63 to 32 of the 192 bit channel status.

5.12.4. I2SCH0Stat2

Mnemonic	I2SCH0STAT2 (Address = 0x0890)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	i2s_ch_stat2								
Type	RW								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	i2s_ch_stat2								
type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	i2s_ch_stat2								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	i2s_ch_stat2								
type	RW								
Default	0x0								

Table 5.110 I2SCH0STAT2 Register

Register Field	Bit	Default	Description
i2s_ch_stat2	[31:0]	0x0	This provides the bits 95 to 64 of the 192 bit channel status.

5.12.5. I2SCH0Stat3

Mnemonic	I2SCH0STAT3 (Address = 0x0894)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	i2s_ch_stat3								
Type	RW								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	i2s_ch_stat3								
type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	i2s_ch_stat3								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	i2s_ch_stat3								
type	RW								
Default	0x0								

Table 5.111 I2SCH0STAT3 Register

Register Field	Bit	Default	Description
i2s_ch_stat3	[31:0]	0x0	This provides the bits 127 to 96 of the 192 bit channel status.

5.12.6. I2SCH0Stat4

Mnemonic	I2SCH0STAT4 (Address = 0x0898)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	i2s_ch_stat4								
Type	RW								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	i2s_ch_stat4								
type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	i2s_ch_stat4								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	i2s_ch_stat4								
type	RW								
Default	0x0								

Table 5.112 I2SCH0STAT4 Register

Register Field	Bit	Default	Description
i2s_ch_stat4	[31:0]	0x0	This provides the bits 159 to 128 of the 192 bit channel status.

5.12.7. I2SCH0Stat5

Mnemonic	I2SCH0STAT5 (Address = 0x089C)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	i2s_ch_stat5								
Type	RW								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	i2s_ch_stat5								
type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	i2s_ch_stat5								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	i2s_ch_stat5								
type	RW								
Default	0x0								

Table 5.113 I2SCH0STAT5 Register

Register Field	Bit	Default	Description
i2s_ch_stat5	[31:0]	0x0	This provides the bits 191 to 160 of the 192 bit channel status.

5.12.8. I2SCH1Stat0

Mnemonic	I2SCH1STAT0 (Address = 0x08A0)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	i2s_ch_stat0								
Type	RW								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	i2s_ch_stat0								
Type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	i2s_ch_stat0								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	i2s_ch_stat0								
Type	RW								
Default	0x0								

Table 5.114 I2SCH1STAT0 Register

Register Field	Bit	Default	Description
i2s_ch_stat0	[31:0]	0x0	This provides the bits 31 to 0 of the 192 bit channel status.

5.12.9. I2SCH1Stat1

Mnemonic	I2SCH1STAT1 (Address = 0x08A4)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	i2s_ch_stat1								
Type	RW								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	i2s_ch_stat1								
Type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	i2s_ch_stat1								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	i2s_ch_stat1								
Type	RW								
Default	0x0								

Table 5.115 I2SCH1STAT1 Register

Register Field	Bit	Default	Description
i2s_ch_stat1	[31:0]	0x0	This provides the bits 63 to 32 of the 192 bit channel status.

5.12.10. I2SCH1Stat2

Mnemonic	I2SCH1STAT2 (Address = 0x08A8)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	i2s_ch_stat2							
Type	RW							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	i2s_ch_stat2							
type	RW							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	i2s_ch_stat2							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	i2s_ch_stat2							
type	RW							
Default	0x0							

Table 5.116 I2SCH1STAT2 Register

Register Field	Bit	Default	Description
i2s_ch_stat2	[31:0]	0x0	This provides the bits 95 to 64 of the 192 bit channel status.

5.12.11. I2SCH1Stat3

Mnemonic	I2SCH1STAT3 (Address = 0x08AC)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	i2s_ch_stat3							
Type	RW							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	i2s_ch_stat3							
type	RW							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	i2s_ch_stat3							
Type	RW							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	i2s_ch_stat3							
type	RW							
Default	0x0							

Table 5.117 I2SCH1STAT3 Register

Register Field	Bit	Default	Description
i2s_ch_stat3	[31:0]	0x0	This provides the bits 127 to 96 of the 192 bit channel status.

5.12.12. I2SCH1Stat4

Mnemonic	I2SCH1STAT4 (Address = 0x08B0)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	i2s_ch_stat4								
Type	RW								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	i2s_ch_stat4								
type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	i2s_ch_stat4								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	i2s_ch_stat4								
type	RW								
Default	0x0								

Table 5.118 I2SCH1STAT4 Register

Register Field	Bit	Default	Description
i2s_ch_stat4	[31:0]	0x0	This provides the bits 159 to 128 of the 192 bit channel status.

5.12.13. I2SCH1Stat5

Mnemonic	I2SCH1STAT5 (Address = 0x08B4)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	i2s_ch_stat5								
Type	RW								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	i2s_ch_stat5								
type	RW								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	i2s_ch_stat5								
Type	RW								
Default	0x0								
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	i2s_ch_stat5								
type	RW								
Default	0x0								

Table 5.119 I2SCH1STAT5 Register

Register Field	Bit	Default	Description
i2s_ch_stat5	[31:0]	0x0	This provides the bits 191 to 160 of the 192 bit channel status.

5.13. DP1 Source Control Register

5.13.1. DP1_SrcCtrl Register

DP1_SRCCTRL (Address = 0x07A0)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved		Pre		Reserved		Swg	
Type	RO		R/W		RO		R/W	
Default	0x0		0x0		0x0		0x0	
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved		SCRMBL	EN810B	Reserved		TrainPat	
Type	RO		R/W	R/W	RO		R/W	
Default	0x0		0x1	0x1	0x0		0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				SSCG	Reserved	BW	AutoCorrect
Type	RO				R/W	RO	R/W	R/W
Default	0x0				0x0	0x0	0x0	0x0

Table 5.120 DP1_SrcCtrl Register

Field Name	Bit	Description
Reserved	[31:22]	Reserved
Pre	[21:20]	Pre-Emphasis Settings for lane split mode 0x0: No Pre-emphasis (0 dB) 0x1: 3.5 dB pre-emphasis 0x2: 6 dB pre-emphasis others: Reserved
Reserved	[19:18]	Reserved
Swg	[17:16]	Voltage Swing Settings for lane split mode 0x0: 0.4V Vdiff_pp (default) 0x1: 0.6V Vdiff_pp 0x2: 0.8V Vdiff_pp 0x3: 1.2V Vdiff_pp
Reserved	[15:14]	Reserved
SCRMBL	[13]	Scrambler Disabled 0: Scrambler Enabled 1: Scrambler Disabled
EN810B	[12]	Enable for 8/10B Encoder in DP PHY 0: Disable 8/10B Encoder 1: Enable 8/10B Encoder (TxData[19:16] not used)
Reserved	[11:10]	Reserved

TrainPat	[9:8]	Link Training Pattern to be sent for lane split mode 00 – Training not in progress (or disabled) 01 – Training Pattern 1 10 – Training Pattern 2 11 – Use pattern programmed in TPatDat0 to TPatDat3
Reserved	[7:4]	Reserved
SSCG	[3]	Spread Spectrum Enable 0: Spread Spectrum Disabled (default) 1: Spread Spectrum Enabled
Reserved	[2]	Reserved
BW	[1]	Link Bandwidth Setting: 0: 1.62 Gbps link 1: 2.7 Gbps link (default)
AutoCorrect	[0]	AutoCorrect Mode for lane split mode Host interference not needed to re-adjust Link parameters for next Link Training Loop 0: Host needs to adjust settings for each Training Loop (default) 1: Host sets initial settings and then waits for completion of link training (all loops done)

5.14. PLL Registers

5.14.1. DP0_PLLCTRL Register

Mnemonic	DP0_PLLCTRL (Address = 0x0900)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					Pllupdate	PLLbyp	PLLEn
Type	RO					WO	R/W	R/W
Default	0x0					0x0	0x1	0x0

Table 5.121 DP0_PLLCTRL Register

Field Name	Bit	Description
Reserved	[31:3]	Reserved
PllUpdate	[2]	Force PLL parameter update register Writing 1 to this bit will copy PLL parameters to shadow registers and force a pll update. Chip should not be accessed until PLL lock time is reached. Writing 0 has not effect.
Pllbyp	[1]	PLL Bypass (BYPCKEN) PLL is bypassed when this bit is set. 0: PLL bypass disabled 1: PLL bypass enabled
Pllen	[0]	Enable entire PLL 0: Power down PLL 1: Enable PLL

5.14.2. PXL_PLLCTRL Register

Mnemonic	PXL_PLLCTRL (Address = 0x0908)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					PlIupdate	PLLByp	PLLEn
Type	RO					WO	R/W	R/W
Default	0x0					0x0	0x1	0x0

Table 5.122 PXL_PLLCTRL Register

Field Name	Bit	Description
Reserved	[31:3]	Reserved
PlIUpdate	[2]	Force PLL parameter update register Writing 1 to this bit will copy PLL parameters to shadow registers and force a pll update. Chip should not be accessed until PLL lock time is reached. Writing 0 has not effect.
PlIByp	[1]	PLL Bypass (BYPCKEN) PLL is bypassed when this bit is set. 0: PLL bypass disabled 1: PLL bypass enabled
PlLEn	[0]	Enable entire PLL 0: Power down PLL 1: Enable PLL

5.14.3. PXL_PLLPARAM Register

Mnemonic	PXL_PLLPARAM (Address = 0x0914)							
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							LBWS
Type	RO							R/W
Default	0x0							0x0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved	EXT_PRE_DIV			Reserved	EXT_POST_DIV		
Type	RO	R/W			RO	R/W		
Default	0x0	0x3			0x0	0x3		
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	IN_SEL		Reserved		PRE_DIV			
Type	R/W		RO		R/W			
Default	0x0		0x0		0x4			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	FBD						
Type	RO	R/W						
Default	0x0	0x1A						

Table 5.123 PXL_PLLPARAM Register

Field Name	Bit	Description
Reserved	[31:25]	Reserved
LBWS	[24]	Low Bandwidth Select 0: For PLL VCO < 300 MHz 1: For PLL VCO \geq 300 MHz
Reserved	[23]	Reserved
EXT_PRE_DIV	[22:20]	External Pre-divider External pre-divider for PLL input clock 1, 2, 3, 5, 7: Valid values. Others: Reserved
Reserved	[19]	Reserved
EXT_POST_DIV	[18:16]	External Post-divider External post-divider for PLL output clock 1, 2, 3, 5, 7: Valid values. Others: Reserved
IN_SEL	[15:14]	2'b00: Use RefClk 2'b01: Use HSCK clock from DSI Clock lane Rx 2'b10: Use HSCKBY2 clock from DSI Clock lane Rx 2'b11: Use HSCKBY4 clock from DSI Clock lane Rx
Reserved	[13:12]	Reserved

PRE_DIV	[11:8]	PLL RefClk divider Divider for PLL RefClk. 0: Divider = 16 1-15: Divider = Pre_Div value (1 – 15). Others: Reserved
Reserved	[7]	Reserved
FBD	[6:0]	PLL feedback divider Multiplier for PLL. 0: Multiplier = 128 1-127: Multiplier = FBD value (1 – 127). Others: Reserved

Note:

$$f_{PCLK} = f_{RefClk} * FBD / (EXT_PRE_DIV * PRE_DIV * EXT_POST_DIV)$$

Where:

f_{RefClk} = Frequency of input reference clock (depending upon IN_SEL setting)

f_{PCLK} = Pixel Clock required based on frame resolution and frame rate

Restrictions:

f_{RefClk} / EXT_PRE_DIV should be in 1 to 200 MHz range

$f_{RefClk} * FBD / (EXT_PRE_DIV * PRE_DIV)$ should be in 150 to 650 MHz range

5.14.4. SYS_PLLPARAM Register

Mnemonic	SYS_PLLPARAM (Address = 0x0918)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B23	B22	B21	B20	B19	B18	B17	B16	
Name	Reserved								
Type	RO								
Default	0x0								
Bit	B15	B14	B13	B12	B11	B10	B9	B8	
Name	Reserved						REF_FREQ		
Type	RO						R/W		
Default	0x0						0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B0	
Name	Reserved			SYSCLK_SEL	Reserved			LSCLK_DIV	
Type	RO			R/W	RO			R/W	
Default	0x0			0x0	0x0			0x0	

Table 5.124 SYS_PLLPARAM Register

Field Name	Bit	Description
Reserved	[31:10]	Reserved
REF_FREQ	[9:8]	RefClk frequency 2'b00: RefClk frequency is 38.4 MHz 2'b01: RefClk frequency is 19.2 MHz 2'b10: RefClk frequency is 26 MHz 2'b11: RefClk frequency is 13 MHz
Reserved	[7:5]	Reserved
SYSCLK_SEL	[4]	SYSCLK Source Select 0: Use LSCLK based source 1: Use DSI Clock HSBYTECLK
Reserved	[3:1]	Reserved
LSCLK_DIV	[0]	LSCLK divider for SYSCLK 0: Divide by 1 1: Divide by 2

Note:

These bits are in RefClk domain.

$$f_{SYSCLK} = (\text{SYSCLK_SEL} ? \text{HSBYTECLK} : \text{LSCLK}) / (\text{LSCLK_DIV} + 1)$$

When LSCLK = 270 MHz, LSCLK_DIV should be set to " 1" .

5.15. HDCP Block Registers (Optional)

Register area from 0x0980 to 0x09AC is prepared for HDCP control.

Don't access this area on Non HDCP supported chip.

5.16. Debug Registers

5.16.1. Test control register (TestCtl)

TSTCTL (Address = 0x0A00)								
Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Color_R							
Type	R/W							
Default	0xFF							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Color_G							
Type	R/W							
Default	0xFF							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Color_B							
Type	R/W							
Default	0xFF							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			ENI2CFILTER	Reserved		ColorBarMode	
Type	RO			R/W	RO		R/W	
Default	0x0			0x1	0x0		0x0	

Table 5.125 TC358867XBG Test Control Register

Field Name	Bit	Description
Color_R	[31:24]	Red Color component value Default: 255 Provides Red color component value for color bar mode
Color_G	[23:16]	Green Color component value Default: 255 Provides Green color component value for color bar mode
Color_B	[15:8]	Blue Color component value Default: 255 Provides Blue color component value for color bar mode
Reserved	[7:5]	Reserved
ENI2CFILTER	[4]	Enable I²C Filter 0: Disable 1: Enable

Field Name	Bit	Description
Reserved	[3:2]	Reserved
ColorBarMode	[1:0]	Color bar Mode 2'b0: Normal operation 2'b1: Select TC358867XBG solid color mode to DisplayPort™ o/p 2'b2: Select TC358867XBG color bar mode to DisplayPort™ o/p 2'b3: Select TC358867XBG color checkers mode to DisplayPort™ o/p

5.16.2. PLL_DBG Debug Register

0x0A04 is PLL_DBG test register. Don't access the register.

Keep default value.

6. Package

The package for TC358867XBG is described in the figure below.

P-VFBGA80-0707-0.65-001

"Unit: mm"

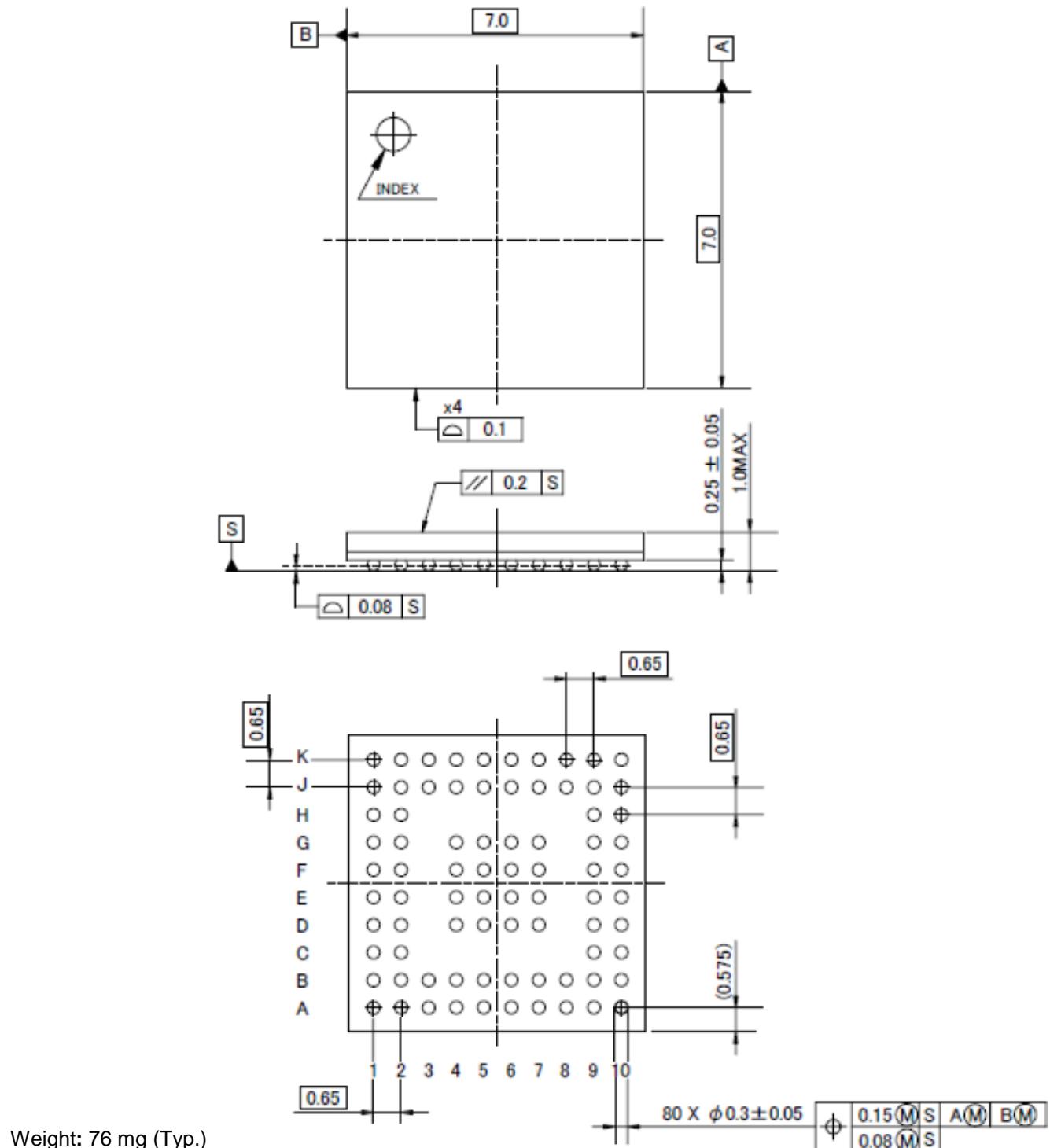


Figure 6.1 80 ball TC358867XBG package

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

VSS/VSS_DP = 0V reference

VDD18 used for VDDS, VDD_DP18 and VDD_PLL18; VDD12 used for VDDC, VDD_DSI12, VDD_DP12 and VDD_PLL912.

Table 7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V)	VDD18	-0.3 to +3.5	V
Supply voltage (1.2V)	VDD12	-0.3 to +2.0	V
Supply voltage (IO)	VDD18	-0.3 to +3.5	V
	VREF	-0.3 to +3.5	V
Input voltage	VIN	-0.3 to VDDS+0.3	V
Output voltage	VOUT	-0.3 to VDDS+0.3	V
Storage temperature	Tstg	-40 to +125	°C

7.2. Operating Condition

VSS/VSS_DP = 0V reference

VDD18 used for VDDS, VDD_DP18 and VDD_PLL18; VDD12 used for VDDC, VDD_DSI12, VDD_DP12 and VDD_PLL912.

Table 7.2 Operating Condition

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8V)	VDD18	1.71	1.8	1.89	V
Supply voltage (1.2V)	VDD12	1.14	1.2	1.26	V
Operating frequency (internal)	Fopr	—	—	200	MHz
Operating temperature	Ta	-20	—	+85	°C

7.3. DC Electrical Specification

VSS/VSS_DP = 0V reference

Table 7.3 DC Electrical Specification

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage High level CMOS input (Note1)	VIH	0.7 VDDS	—	VDDS	V
Input voltage Low level CMOS input (Note1)	VIL	0	—	0.3 VDDS	V
Input voltage High level CMOS Schmitt Trigger (Note1)	VIHS	0.7 VDDS	—	VDDS	V
Input voltage Low level CMOS Schmitt Trigger (Note1)	VILS	0	—	0.3 VDDS	V
Output voltage High level (Note1), (Note2)	VOH	0.8 VDDS	—	VDDS	V
Output voltage Low level (Note1), (Note2)	VOL	0	—	0.2 VDDS	V
Input leak current High level	I _{IIH1} (Note3)	-10	—	10	µA
Input leak current Low level	I _{IIL1} (Note4)	-10	—	10	µA
	I _{IIL2} (Note5)	-200	—	-10	µA

Note1: VDDS within recommended operating condition.

Note2: Output current value is according to each IO buffer specification. Output voltage changes with output current value.

Note3: Normal pin, or Pull-up I/O pin applied VDDS supply voltage to input pin

Note4: Normal pin applied VSS (0V) to input pin

Note5: Pull-up I/O pin applied VSS (0V) to input pin

7.4. Power Consumption (Typical value based on estimation)

Power consumption as measured for the power-down modes and for normal operation are provided below:

- Power-down mode (DSI-Rx in ULPS, DP PHY & PLLs disabled, clocks stopped):
 - DSI Rx: 0.01 mW
 - DP PHY: 2.34 mW
 - PLL9: 0.01 mW
 - Core: 0.96 mW
 - Rest: 0.01 mW
- Normal operation (1920 x 1080 resolution with DSI-Rx in 4-lane @925 Mbps per lane, DP PHY in dual lane link @2.7 Gbps per lane):
 - DSI Rx: 21.79 mW
 - DP PHY: 142.70 mW
 - PLL9: 2.42 mW
 - Core: 87.64 mW
 - IOs: 1.68 mW

8. Timing Definitions

8.1. MIPI DSI Timings

8.1.1. LP Transmitter DC Specifications

The low power transmitter is used for driving the lines in all low-power operating modes. The DC characteristics of the LP transmitter are given below.

Table 8.1 DSI LP Transmitter DC Specifications

Parameter	Symbol	Min	Typ.	Max	Unit
Thevenin output high level	V_{OH}	1.1	1.2	1.3	V
Thevenin output low level	V_{OL}	-50	—	50	mV

8.1.2. HS Receiver DC Specifications

The high-speed receiver is a differential line receiver with a switchable parallel input termination. It is used to receive data during high speed transmission from the host. The DC characteristics of the HS receiver are given below.

Table 8.2 DSI HS Receiver DC Specifications

Parameter	Symbol	Min	Typ.	Max	Unit
Common-mode voltage HS receive mode	$V_{CMRX(DC)}$	70	—	330	mV
Differential input high threshold	V_{IDTH}	—	—	70	mV
Differential input low threshold	V_{IDTL}	-70	—	—	mV
Single-ended input high voltage	V_{IHHS}	—	—	460	mV
Single-ended input low voltage	V_{ILHS}	-40	—	—	mV
Single-ended threshold for HS termination enable	$V_{TERM-EN}$	—	—	450	mV
Differential input impedance	Z_{ID}	80	100	125	Ω

8.1.3. LP Receiver DC Specifications

The low-power receiver is used to detect the Low-Power state on each pin. It is used to receive data during low speed transmission from the host. The DC characteristics of the LP receiver are given below.

Table 8.3 DSI LP Receiver DC Specifications

Parameter	Symbol	Min	Typ.	Max	Unit
Logic 1 input voltage	V_{IH}	880	—	—	mV
Logic 0 input voltage, not in ULP state	V_{IL}	—	—	550	mV
Logic 0 input voltage, ULP state	$V_{IL-ULPS}$	—	—	300	mV
Input hysteresis	V_{HYST}	25	—	—	mV

8.2. DPI Interface Timings

Table 8.4 DPI timing

Parameter	Symbol	Min	Typ.	Max	Unit
Vsync Setup Time	VSST	2.5	—	—	ns
Vsync Hold Time	VSHT	1.5	—	—	ns
Hsync Setup Time	HSST	2.5	—	—	ns
Hsync Hold Time	HSHT	1.5	—	—	ns
Pixel Clock Period	PCLKCYC	6.5	—	—	ns
Pixel Clock Duty Cycle	—	—	—	55	%
Pixel Clock Low Duration	PCLKLT	2.95	—	—	ns
Pixel Clock High Duration	PCLKHT	2.95	—	—	ns
Data Setup Time	DST	2.5	—	—	ns
Data Hold Time	DHT	1.5	—	—	ns

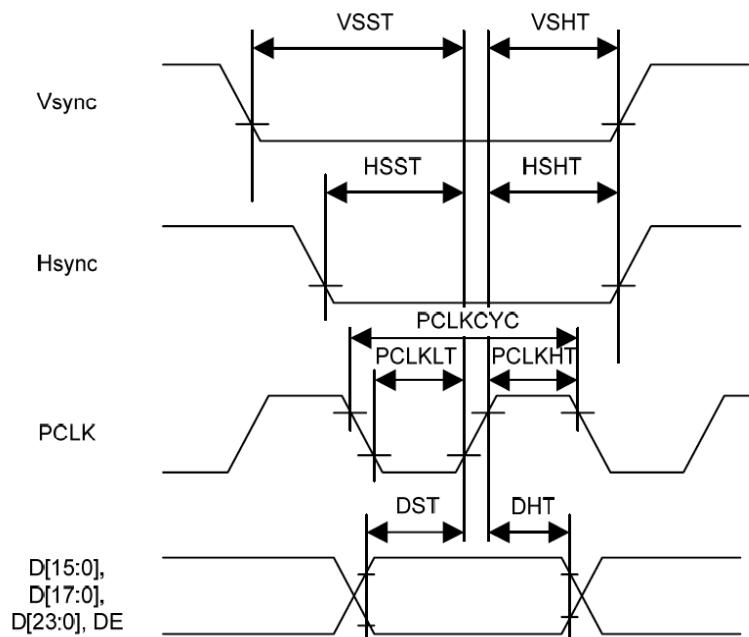


Figure 8.1 DPI Interface timing

8.3. Parallel Output Interface Timings

Table 8.5 Parallel output interface timing

Parameter	Symbol	Min	Typ.	Max	Unit
Vsync Setup Time	VSST	6.0	—	—	ns
Vsync Hold Time	VSHT	0.5	—	—	ns
Hsync Setup Time	HSST	6.0	—	—	ns
Hsync Hold Time	HSHT	0.5	—	—	ns
Pixel Clock Period	PCLKCYC	10	—	—	ns
Pixel Clock Duty Cycle	—	—	—	60	%
Pixel Clock Low Duration	PCLKLT	4.00	—	—	ns
Pixel Clock High Duration	PCLKHT	4.00	—	—	ns
Data Setup Time	DST	6.0	—	—	ns
Data Hold Time	DHT	0.5	—	—	ns

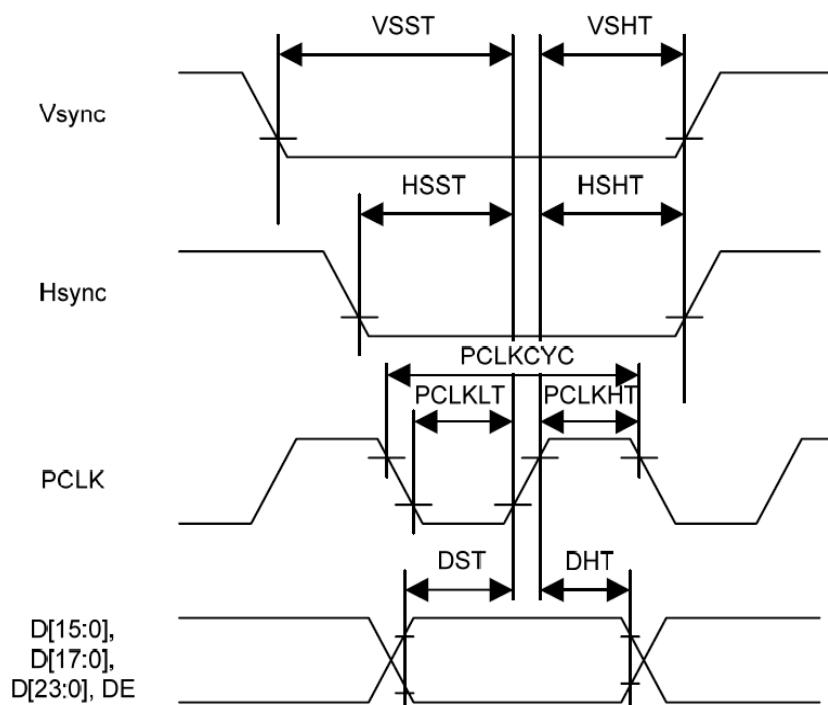


Figure 8.2 Parallel output Interface timing (shown for inverted clock polarity)

8.4. I2S Audio Interface Timings

Table 8.6 I2S timing

Signal	Parameter	Symbol	Min	Typ.	Max	Unit
I2S_BCLK	I2S_Bit Clock Cycle	t_{CYC}	18	—	—	ns
	I2S_Bit Clock High Pulse	t_{CH}	0.4 t_{CYC}	0.5 t_{CYC}	0.6 t_{CYC}	ns
	I2S_Bit Clock Low Pulse	t_{CL}	0.4 t_{CYC}	0.5 t_{CYC}	0.6 t_{CYC}	ns
I2S_LRCLK	I2S_LRCLK hold time to I2S_BCLK rising edge	t_{LRH}	5	—	—	ns
	I2S_LRCLK setup time to I2S_BCLK rising edge	t_{LRS}	5	—	—	ns
I2S_DATA	I2S_DATA hold time to I2S_BCLK rising edge	t_{DH}	5	—	—	ns
	I2S_DATA setup time to I2S_BCLK rising edge	t_{DS}	5	—	—	ns

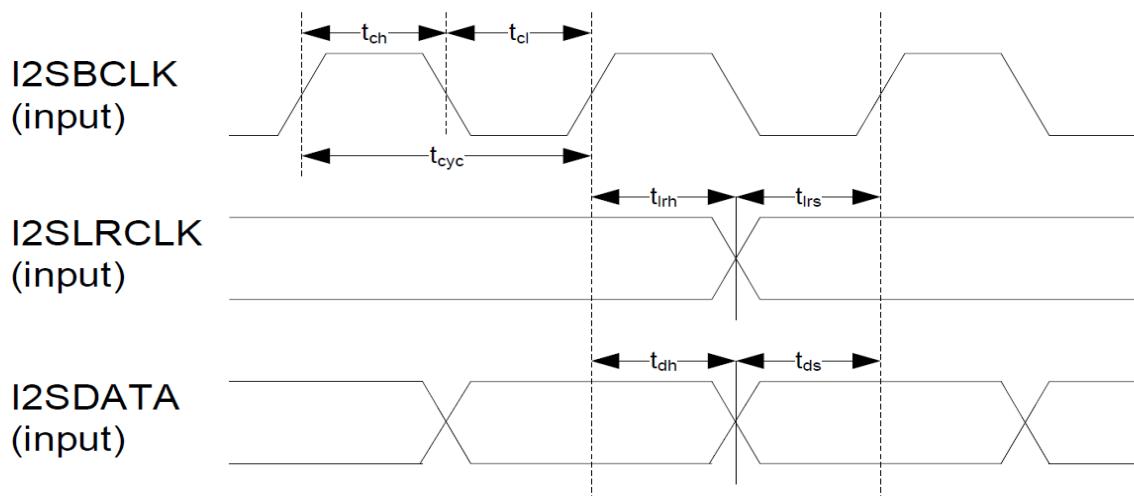


Figure 8.3 I2S timing

8.5. DisplayPort™ Timings

Table 8.7 DisplayPort™ Main Link Transmitter (Main TX) Specifications

Symbol	Parameter	Min	Typ.	Max	Unit	Comment
UI_High_Rate	Unit Interval for high bit rate (2.7 Gbps / lane)	—	370	—	ps	High limit = +300ppm Low limit = -5300ppm
UI_Low_Rate	Unit Interval for low bit rate (1.62 Gbps / lane)	—	617	—	ps	
Down_Spread_Amplitude	Link clock down spreading	0	—	0.5	%	Range: 0% to 0.5% when downspread enabled
Down_Spread_Frequency	Link clock down-spreading frequency	30	—	33	kHz	Range: 30 kHz to 33 kHz when downspread enabled
VTX-DIFFp-p-Level1	Differential Peak-to-peak Output Voltage Level 1	0.34	0.4	0.46	V	
VTX-DIFFp-p-Level2	Differential Peak-to-peak Output Voltage Level 2	0.51	0.6	0.68	V	
VTX-DIFFp-p-Level3	Differential Peak-to-peak Output Voltage Level 3	0.69	0.8	0.92	V	
VTX-DIFFp-p-Level4	Differential Peak-to-peak Output Voltage Level 4	1.02	1.2	1.38	V	
VTX-PREEMP-RATIO	No Pre-emphasis	0.0	0.0	0.0	dB	
	3.5 dB Pre-emphasis Level	2.8	3.5	4.2	dB	
	6.0 dB Pre-emphasis Level	4.8	6.0	7.2	dB	
VTX-DC-CM	TX DC Common Mode Voltage	0	—	2.0	V	Common mode voltage is equal to Vbias_Tx voltage.

8.6. I²C Timings

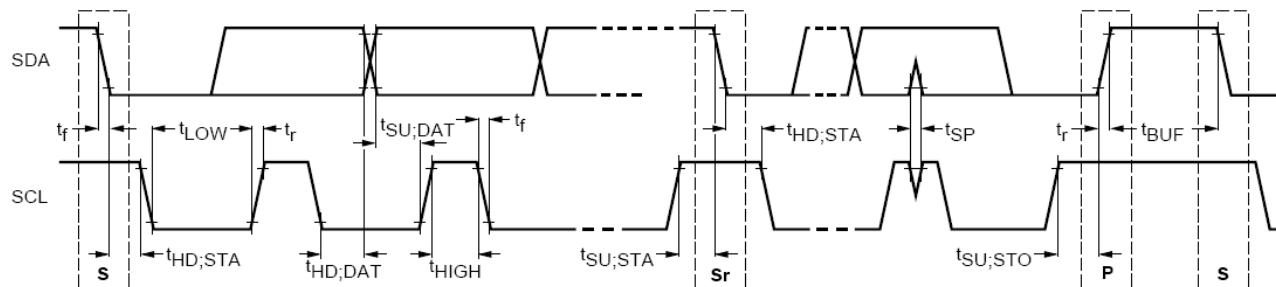


Figure 8.4 I²C timing

Table 8.8 I²C Timing

Item	Symbol	Min	Max	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD,STA}$	0.6	—	μs
LOW period of the SCL clock	t_{LOW}	1.3	—	μs
HIGH period of the SCL clock	t_{HIGH}	0.6	—	μs
Set-up time for a repeated START condition	$t_{SU,STA}$	0.6	—	μs
Data hold time: for I ² C-bus devices	$t_{HD,DAT}$	0	0.9	μs
Data set-up time	$t_{SU,DAT}$	100	—	ns
Rise time of both SDA and SCL signals	t_r	20+0.1Cb	300	ns
Fall time of both SDA and SCL signals	t_f	20+0.1Cb	300	ns
Set-up time for STOP condition	$t_{SU,STO}$	0.6	—	μs
Bus free time between a STOP and START condition	t_{BUFS}	1.3	—	μs

Note: C_b = Capacitive load for each bus line (400 pF max.)

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as "TOSHIBA". Hardware, software and systems described in this document are collectively referred to as "Product".

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**