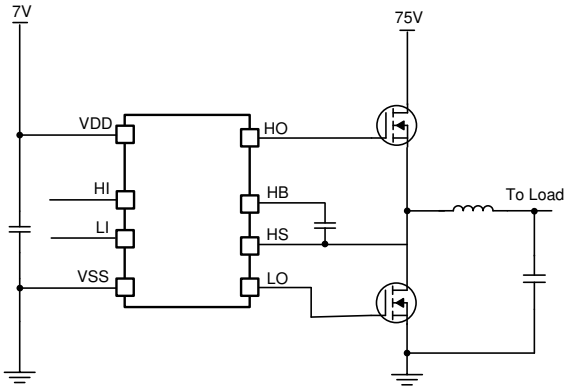
UCC27284-Q1 Automotive 120-V Half-Bridge Driver with Negative Voltage Handling and Low Switching Losses

1 Features

- AEC-Q100 qualified with following results
  - Temperature grade 1 (T_j = –40°C to 150°C)
  - Device HBM ESD classification level 1B
  - Device CDM ESD classification level C3
- Drives two N-channel MOSFETs in high-side low-side configuration
- 5-V typical under voltage lockout
- 16-ns typical propagation delay
- 12-ns rise, 10-ns fall time with 1.8-nF load
- 1-ns typical delay matching
- 5-V negative voltage handling on inputs
- 14-V negative voltage handling on HS
- 3.5-A sink, 2.5-A Source output currents
- Absolute maximum boot voltage 120 V
- Integrated bootstrap diode

2 Applications

- Automotive DC/DC converters
- Electric power steering
- On-board charger (OBC)
- Integrated belt starter generator (iBSG)
- Automotive HVAC compressor modules



Simplified Application Diagram

3 Description

The UCC27284-Q1 is a robust N-channel MOSFET driver with a maximum switch node (HS) voltage rating of 100 V. It allows for two N-channel MOSFETs to be controlled in half-bridge or synchronous buck configuration based topologies. Its 3.5-A peak sink current and 2.5-A peak source current along with low pull-up and pull-down resistance allows the UCC27284-Q1 to drive large power MOSFETs with minimum switching losses during the transition of the MOSFET Miller plateau. Since the inputs are independent of the supply voltage, UCC27284-Q1 can be used in conjunction with both analog and digital controllers. Two inputs, and therefore outputs, can be overlapped, if needed, in applications such as secondary side full-bridge synchronous rectification.

The input pins as well as the HS pin are able to tolerate significant negative voltage, which improves system robustness. 5-V UVLO allows systems to operate at lower bias voltages, which is necessary in many high frequency applications and improves system efficiency in certain operating modes. Small propagation delay and delay matching specifications minimize the dead-time requirement which further improves efficiency.

Under voltage lockout (UVLO) is provided for both the high-side and low-side driver stages forcing the outputs low if the VDD voltage is below the specified threshold. An integrated bootstrap diode eliminates the need for an external discrete diode in many applications, which saves board space and reduces system cost. UCC27284-Q1 is offered in SOIC package for harsh system environments.

Device Information (1)

PART NUMBER	PACKAGE (DESIGNATOR) (SIZE)
UCC27284-Q1	SOIC8 (D) (6 mm x 5mm)
	SOIC8-PowerPAD (DDA) (6 mm x 5mm)

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

Changes from Revision * (March 2020) to Revision A (October 2020)	Page
• Changed marketing status from Advance Information to initial release	1

5 Pin Configuration and Functions

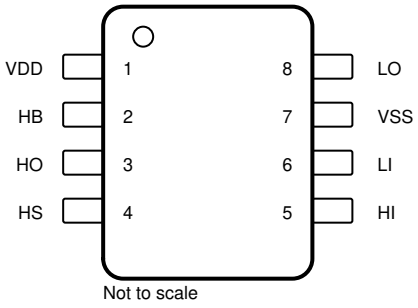


Figure 5-1. D Package 8-Pin SOIC Top View

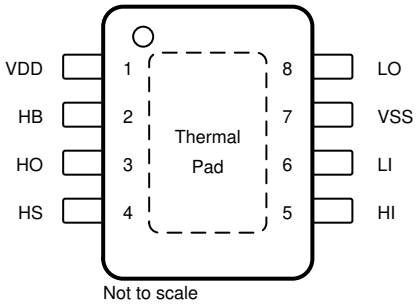


Figure 5-2. DDA Package 8-Pin SOIC with PowerPAD Top View

Pin Functions

PIN			I/O[1]	DESCRIPTION
Name	D	DDA		
HB	2	2	P	High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical recommended value of HB bypass capacitor is 0.1 µF, This value primarily depends on the gate charge of the high-side MOSFET. When using external boot diode, connect cathode of the diode to this pin.
HI	5	5	I	High-side input.
HO	3	3	O	High-side output. Connect to the gate of the high-side power MOSFET or one end of external gate resistor, when used.
HS	4	4	P	High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
LI	6	6	I	Low-side input
LO	8	8	O	Low-side output. Connect to the gate of the low-side power MOSFET or one end of external gate resistor, when used.
VDD	1	1	P	Positive supply to the low-side gate driver. Decouple this pin to VSS. Typical decoupling capacitor value is 1 µF. When using an external boot diode, connect the anode to this pin.
Thermal Pad	n/a	Pad	-	Connect to a large thermal mass trace (generally IC ground plane, VSS) to improve thermal performance. This can only be electrically connected to VSS.

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input/Output

6 Specifications

6.1 Absolute Maximum Ratings

All voltages are with respect to V_{ss} (1) (2)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.3	20	V
V_{HI}, V_{LI}	Input voltages on HI and LI		–5	20	V
V_{LO}	Output voltage on LO	DC	–0.3	V_{DD} + 0.3	V
		Pulses < 100 ns(3)	–2	V_{DD} + 0.3	
V_{HO}	Output voltage on HO	DC	V_{HS} – 0.3	V_{HB} + 0.3	V
		Pulses < 100 ns(3)	V_{HS} – 2	V_{HB} + 0.3	
V_{HS}	Voltage on HS	DC	–10	100	V
		Pulses < 100 ns(3)	–14	100	
V_{HB}	Voltage on HB		–0.3	120	V
V_{HB-HS}	Voltage on HB with respect to HS		–0.3	20	V
T_J	Operating junction temperature		–40	150	°C
	Lead temperature (soldering, 10 sec.)			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to V_{ss}. Currents are positive into, negative out of the specified terminal.
(3) Values are verified by characterization only.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1) (2)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification..
(2) Pins HS, HB and HO are rated at 500V HBM

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	5.5	12	16	V
V_{HI}, V_{LI}	Input Voltage	0		V_{DD}	
V_{LO}	Low side output voltage	0		V_{DD}	
V_{HO}	High side output voltage	V_{HS}		V_{HB}	
V_{HS}	Voltage on HS(1)	–8		100	V
	Voltage on HS (Pulses < 100 ns)(1)	–12		100	
V_{HB}	Voltage on HB	V_{HS} + 5.5		V_{HS}+16	V
V_{sr}	Voltage slew rate on HS			50	V/ns
T_J	Operating junction temperature	–40		150	°C

(1) V_{HB-HS} < 16V (Voltage on HB with respect to HS must be less than 16V)

6.4 Thermal Information

THERMAL METRIC(1)		UCC27284-Q1		UNIT
		D	DDA	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.3	40.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	54.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.1	16.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.7	4.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.1	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	4.9	°C/W

(1) For more information about thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953

6.5 Electrical Characteristics

V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, No load on LO or HO, T_J = –40°C to +150°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{DD}	VDD quiescent current	V_{LI} = V_{HI} = 0		0.3	0.4	mA
I_{DDO}	VDD operating current	f = 500 kHz, C_{LOAD} = 0		2.2	4.5	mA
I_{HB}	HB quiescent current	V_{LI} = V_{HI} = 0 V		0.2	0.4	mA
I_{HBO}	HB operating current	f = 500 kHz, C_{LOAD} = 0		2.5	4	mA
I_{HBS}	HB to VSS quiescent current	V_{HS} = V_{HB} = 110 V		5.0	50	µA
I_{HBSO}	HB to VSS operating current(1)	f = 500 kHz, C_{LOAD} = 0		0.1		mA
INPUT						
V_{HIT}	Input rising threshold		1.9	2.1	2.4	V
V_{LIT}	Input falling threshold		0.9	1.1	1.3	V
V_{IHYS}	Input voltage Hysteresis			1.0		V
R_{IN}	Input pulldown resistance		100	250	350	kΩ
UNDERVOLTAGE LOCKOUT PROTECTION (UVLO)						
V_{DDR}	VDD rising threshold		4.7	5.0	5.4	V
V_{DDF}	VDD falling threshold		4.2	4.5	4.9	V
V_{DDHYS}	VDD threshold hysteresis			0.5		V
V_{HBR}	HB rising threshold with respect to HS pin		3.3	3.7	4.7	V
V_{HBF}	HB falling threshold with respect to HS pin		3.0	3.3	4.4	V
V_{HBHYS}	HB threshold hysteresis			0.3		V
BOOTSTRAP DIODE						
V_F	Low-current forward voltage	I_{VDD-HB} = 100 µA		0.65	0.85	V
V_{FI}	High-current forward voltage	I_{VDD-HB} = 80 mA		0.85	1.0	V
R_D	Dynamic resistance, $\Delta V_F/\Delta I$	I_{VDD-HB} = 100 mA and 80 mA		1.5	2.5	Ω
LO GATE DRIVER						
V_{LOL}	Low level output voltage	I_{LO} = 100 mA		0.085	0.4	V
V_{LOH}	High level output voltage	I_{LO} = -100 mA, V_{LOH} = V_{DD} – V_{LO}		0.13	0.42	V
	Peak pullup current (1)	V_{LO} = 0 V		2.5		A
	Peak pulldown current (1)	V_{LO} = 12 V		3.5		A

V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, No load on LO or HO, T_J = –40°C to +150°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HO GATE DRIVER						
V_{HOL}	Low level output voltage	I_{HO} = 100 mA		0.1	0.4	V
V_{HOH}	High level output voltage	I_{HO} = –100 mA, V_{HOH} = V_{HB}- V_{HO}		0.12	0.42	V
	Peak pullup current (1)	V_{HO} = 0 V		2.5		A
	Peak pulldown current (1)	V_{HO} = 12 V		3.5		A

(1) Parameter not tested in production

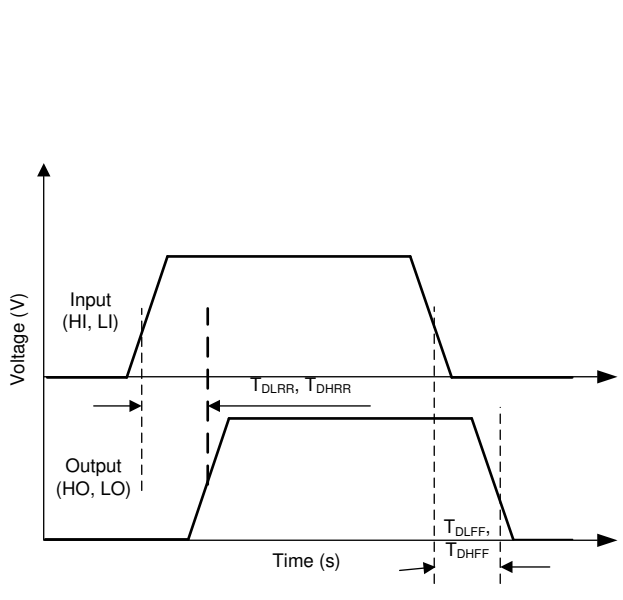
6.6 Switching Characteristics

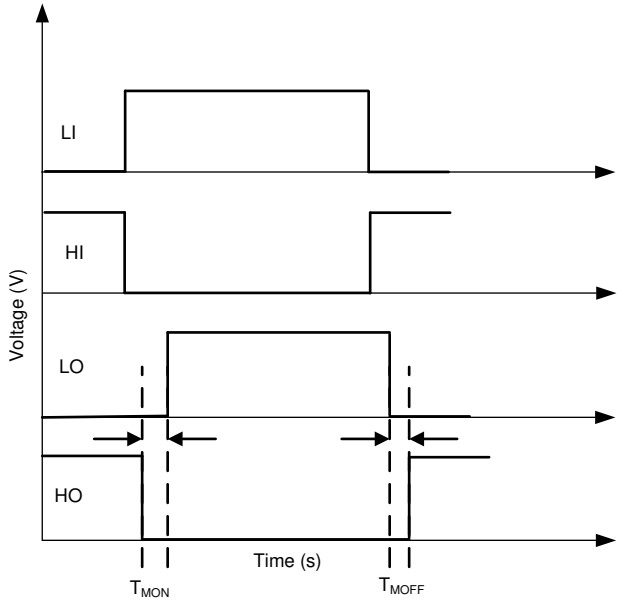
V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, No load on LO or HO, T_J = –40°C to +150°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROPAGATION DELAYS						
t_{DLFF}	V_{LI} falling to V_{LO} falling	See Section 6.7		16	30	ns
t_{DHFF}	V_{HI} falling to V_{HO} falling	See Section 6.7		16	30	ns
t_{DLRR}	V_{LI} rising to V_{LO} rising	See Section 6.7		16	30	ns
t_{DHRR}	V_{HI} rising to V_{HO} rising	See Section 6.7		16	30	ns
DELAY MATCHING						
t_{MON}	From LO being ON to HO being OFF	See Section 6.7		1	7	ns
t_{MOFF}	From LO being OFF to HO being ON	See Section 6.7		1	7	ns
OUTPUT RISE AND FALL TIME						
t_R	LO, HO rise time	C_{LOAD} = 1800 pF, 10% to 90%		12		ns
t_F	LO, HO fall time	C_{LOAD} = 1800 pF, 90% to 10%		10		ns
t_R	LO, HO (3 V to 9 V) rise time	C_{LOAD} = 0.1 µF, 30% to 70%		0.33	0.6	µs
t_F	LO, HO (3 V to 9 V) fall time	C_{LOAD} = 0.1 µF, 70% to 30%		0.23	0.6	µs
MISCELLANEOUS						
$T_{PW,min}$	Minimum input pulse width that changes the output			20		ns
	Bootstrap diode turnoff time(1)	I_F = 20 mA, I_{REV} = 0.5 A		50		ns

(1) Parameter not tested in production

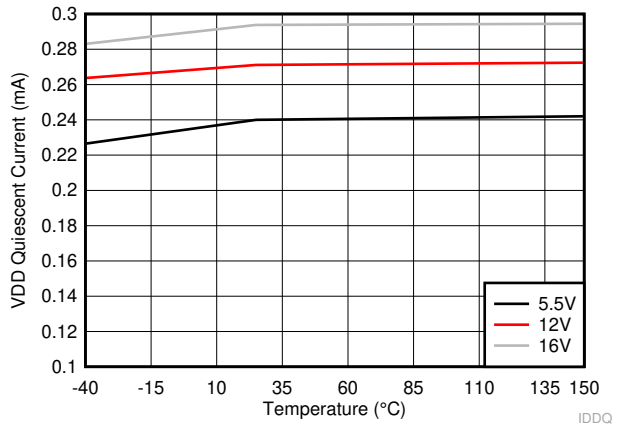
6.7 Timing Diagrams





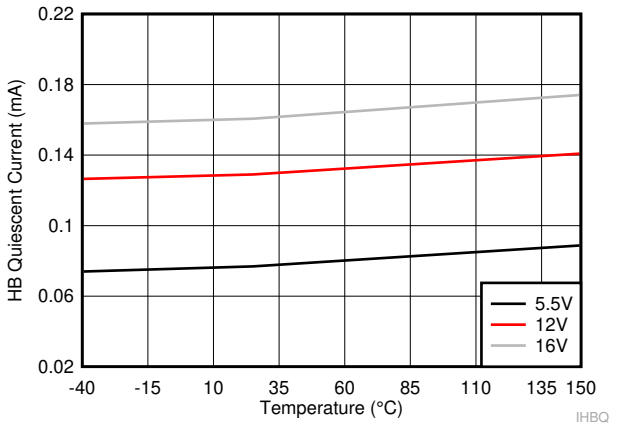
6.8 Typical Characteristics

Unless otherwise specified V_{VDD}=V_{HB} = 12 V, V_{HS}=V_{VSS} = 0 V, No load on outputs



A. V_{HI} = V_{LI} = 0 V

Figure 6-1. VDD Quiescent Current



A. V_{HI} = V_{LI} = 0 V

Figure 6-2. HB Quiescent Current

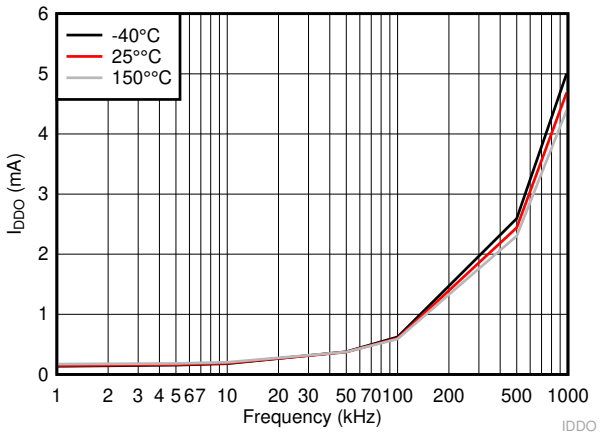


Figure 6-3. VDD Operating Current

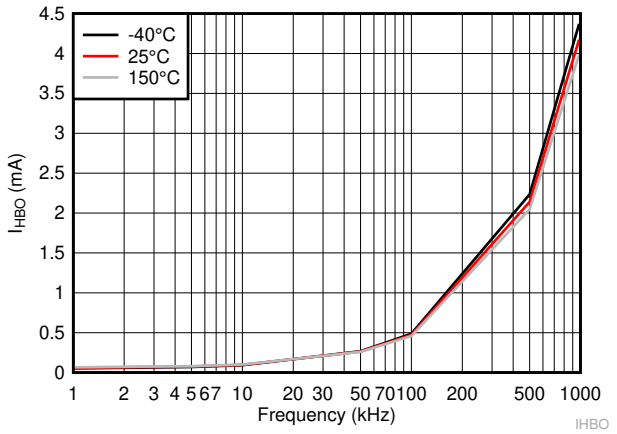
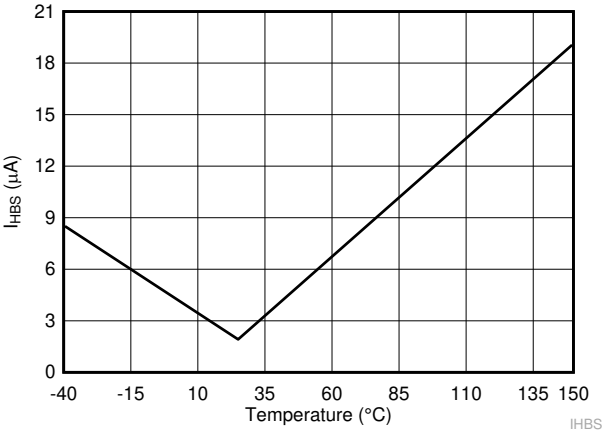


Figure 6-4. HB Operating Current



A. V_{HB}=V_{HS}=100V

Figure 6-5. HB to VSS Quiescent Current

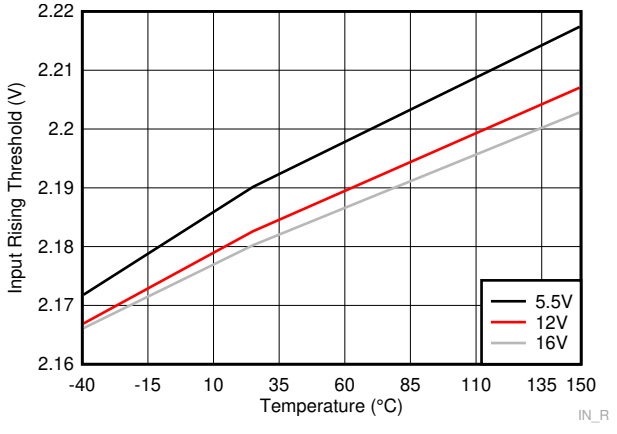


Figure 6-6. Input Rising Threshold

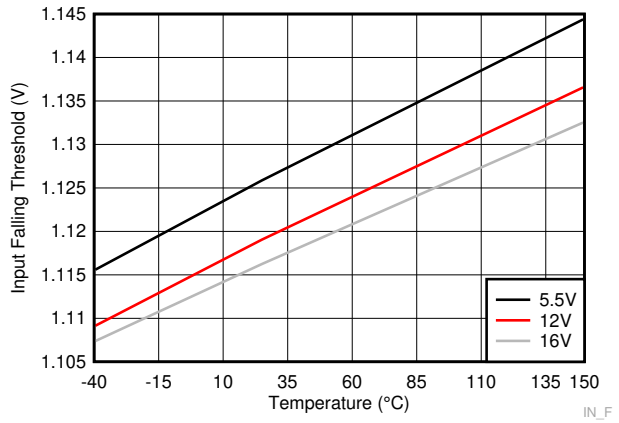


Figure 6-7. Input Falling Threshold

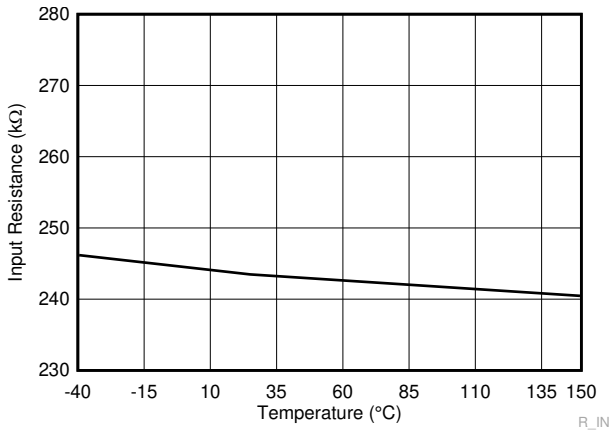


Figure 6-8. Input Pull-down Resistor

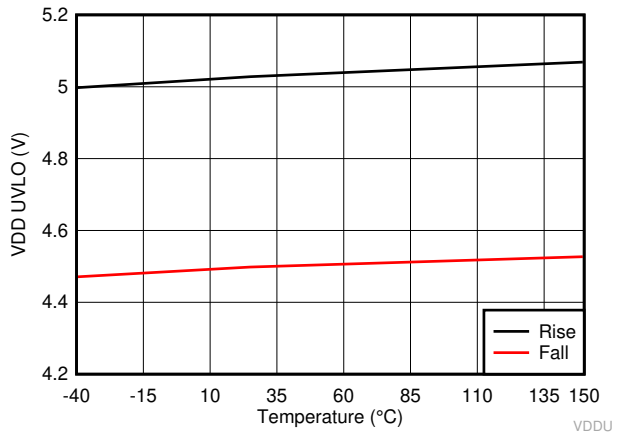


Figure 6-9. VDD UVLO Threshold

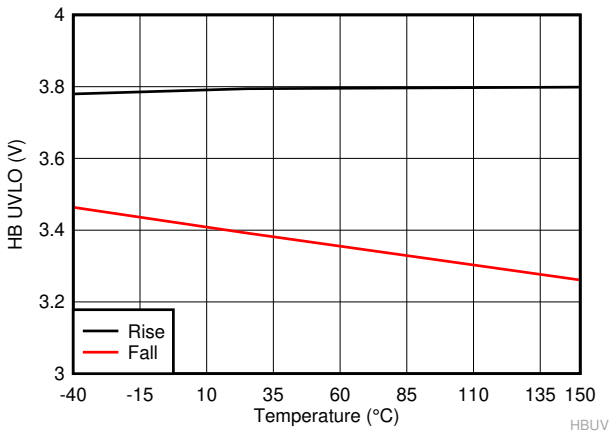


Figure 6-10. HB UVLO Threshold

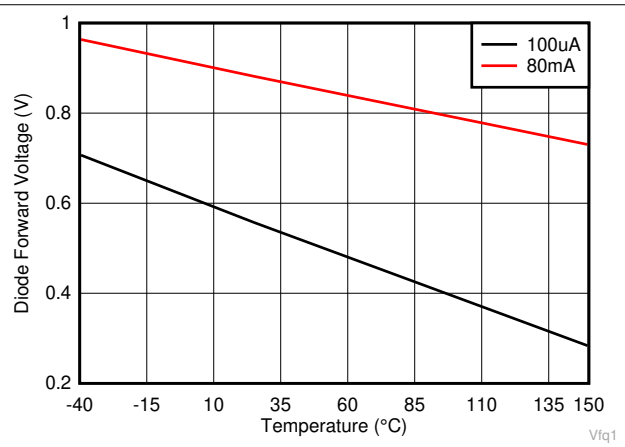


Figure 6-11. Boot Diode Forward Voltage Drop

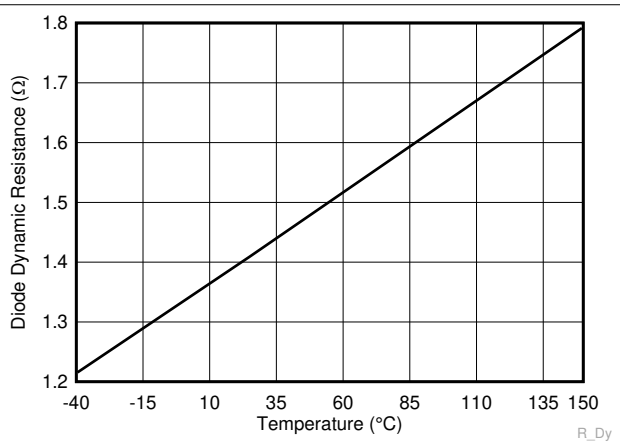
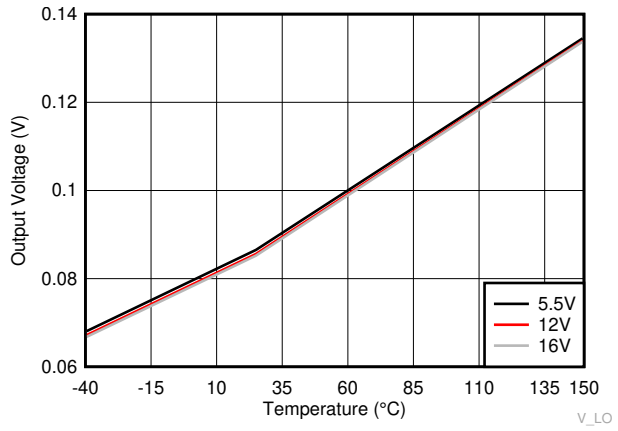
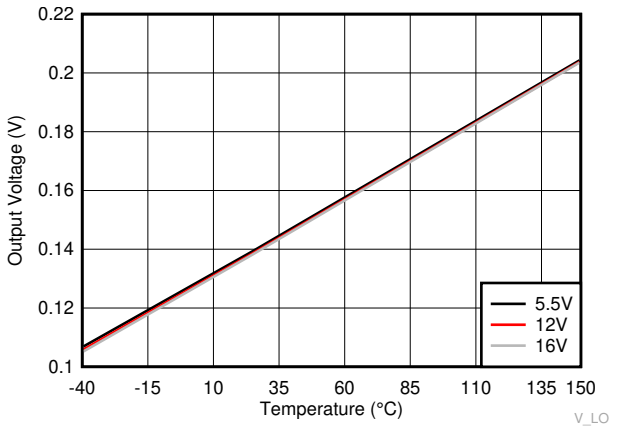


Figure 6-12. Boot Diode Dynamic Resistance



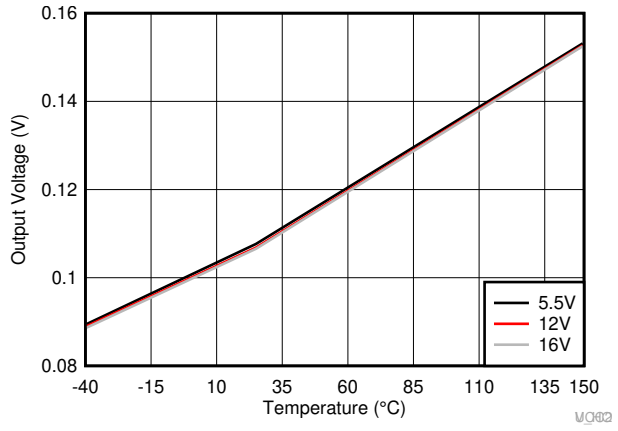
A. I_O=100mA

Figure 6-13. LO Low Output Voltage (V_{LOL})



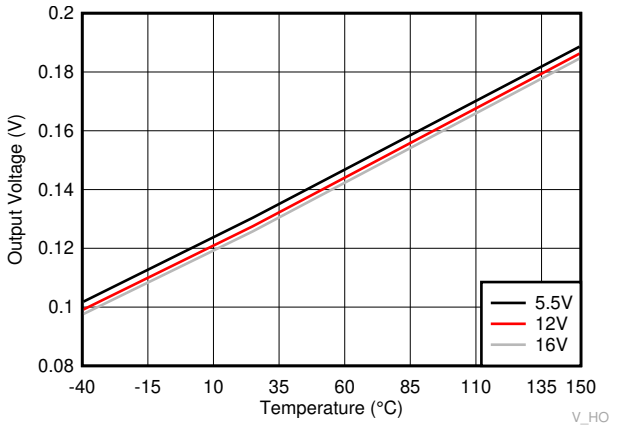
A. I_O=-100mA

Figure 6-14. LO High Output Voltage (V_{LOH})



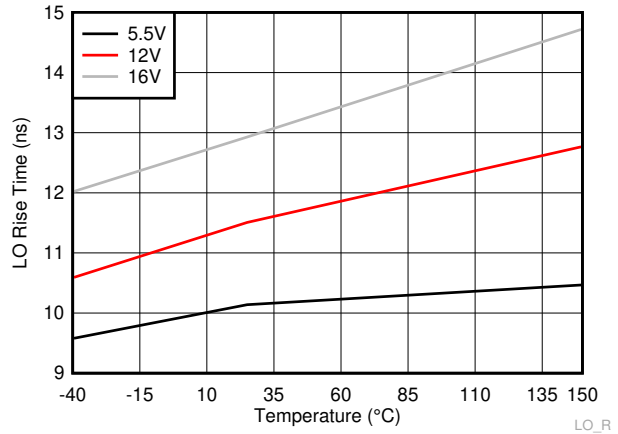
A. I_O=100mA

Figure 6-15. HO Low Output Voltage (V_{HOL})



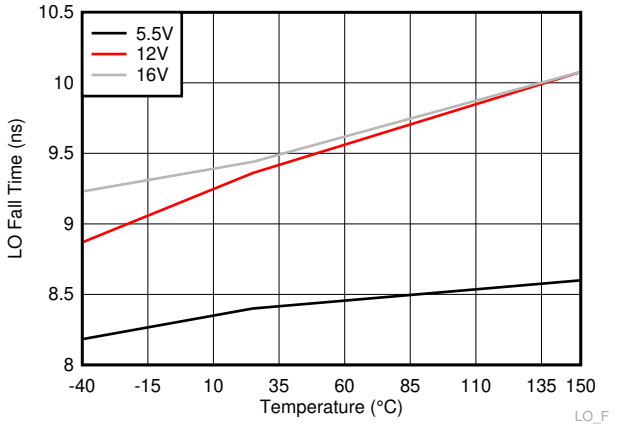
A. I_O=-100mA

Figure 6-16. HO High Output Voltage (V_{HOH})



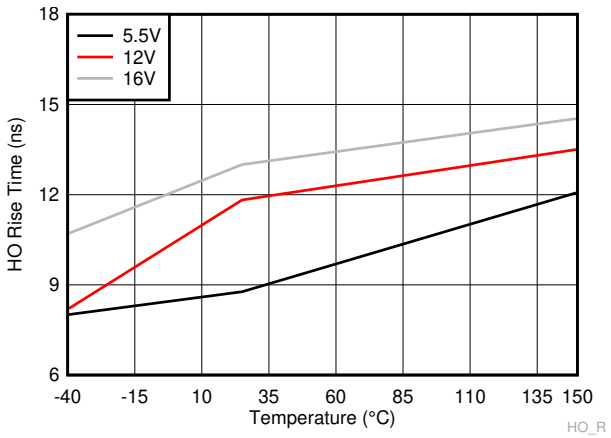
A. C_L=1800pF

Figure 6-17. LO Rise Time



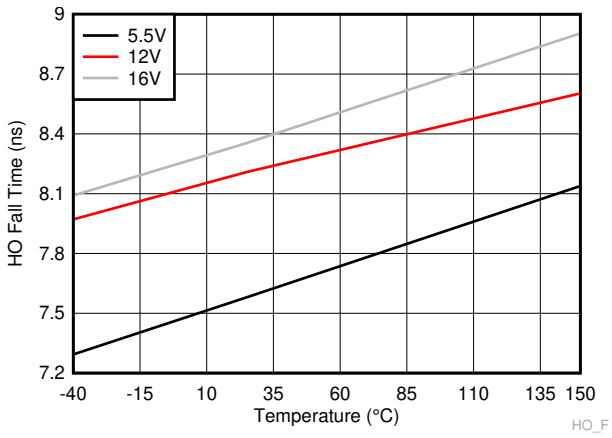
A. C_L=1800pF

Figure 6-18. LO Fall Time



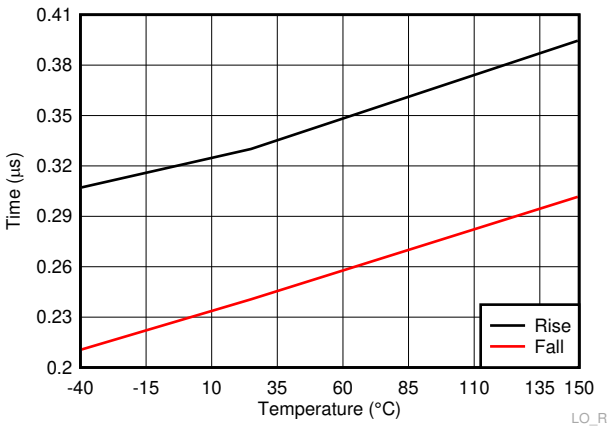
A. C_L=1800pF

Figure 6-19. HO Rise Time



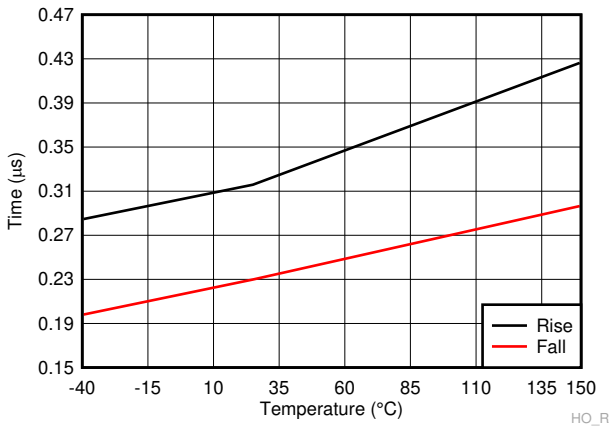
A. C_L=1800pF

Figure 6-20. HO Fall Time



A. C_L=100nF

Figure 6-21. LO Rise & Fall Time



A. C_L=100nF

Figure 6-22. HO Rise & Fall Time

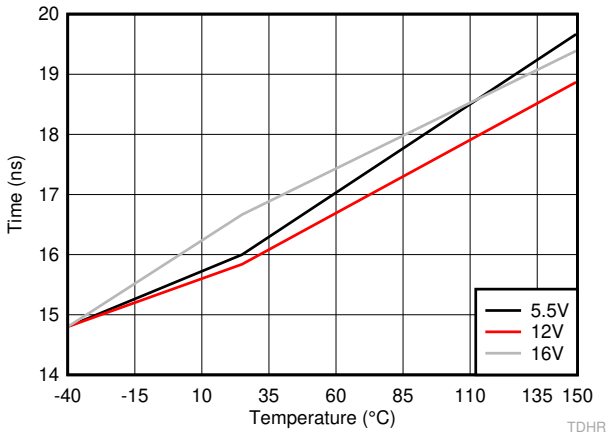


Figure 6-23. HO Rising Propagation Delay (TDHRR)

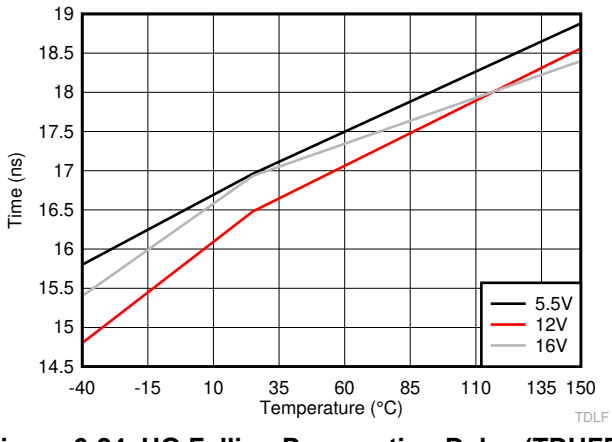


Figure 6-24. HO Falling Propagation Delay (TDHFF)

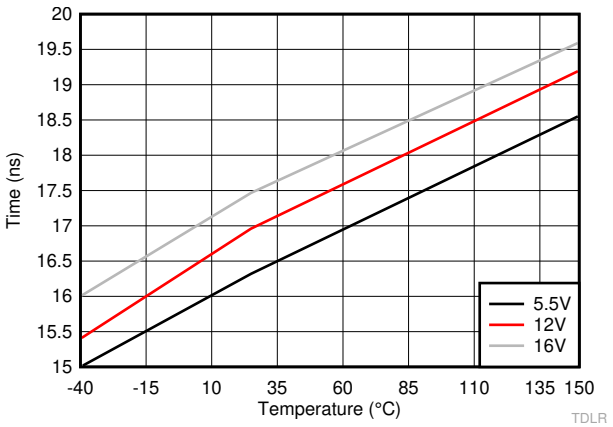


Figure 6-25. LO Rising Propagation Delay (TDLRR)

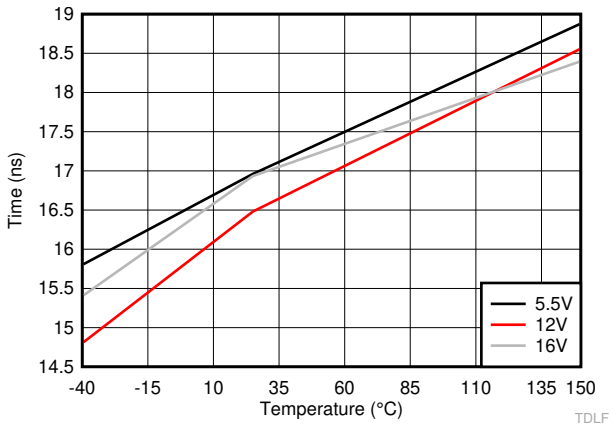


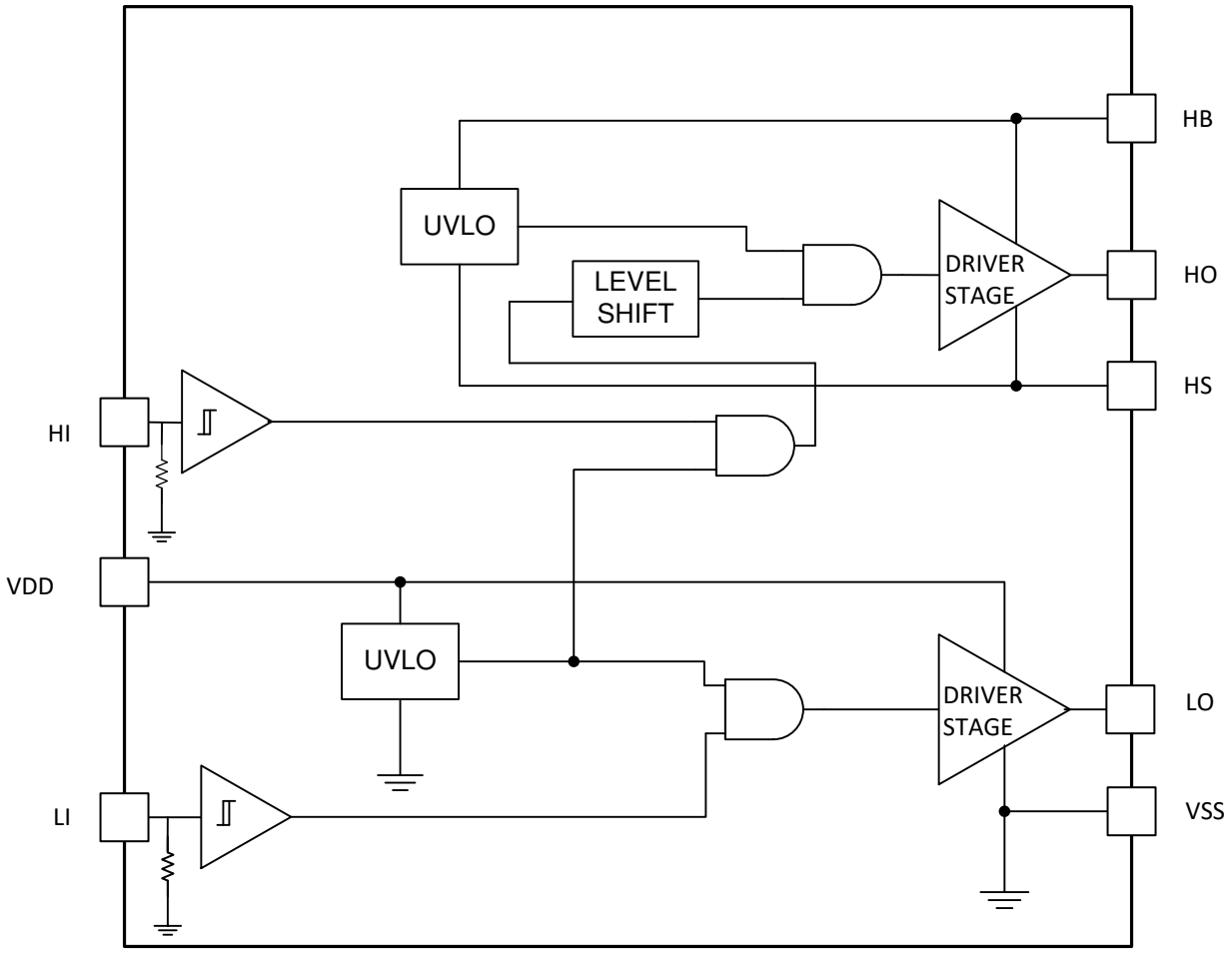
Figure 6-26. LO Falling Propagation Delay (TDLFF)

7 Detailed Description

7.1 Overview

The UCC27284-Q1 is a high-voltage gate driver designed to drive both the high-side and the low-side N-channel FETs in a synchronous buck or a half-bridge configurations. The two outputs are independently controlled with two TTL-compatible input signals. The device can also work with CMOS type control signals at its inputs as long as signals meet turn-on and turn-off threshold specifications of the UCC27284-Q1. The floating high-side driver is capable of working with HS voltage up to 100 V with respect to VSS. A 100 V bootstrap diode is integrated in the UCC27284-Q1 device to charge high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and provides clean level transitions from the control logic to the high-side gate driver. Undervoltage lockout (UVLO) is provided on both the low-side and the high-side power rails.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Start-up and UVLO

Both the high-side and the low-side driver stages include UVLO protection circuitry which monitors the supply voltage (V_{DD}) and the bootstrap capacitor voltage ($V_{HB–HS}$). The UVLO circuit inhibits each output until sufficient supply voltage is available to turn on the external MOSFETs. The built-in UVLO hysteresis prevents chattering during supply voltage variations. When the supply voltage is applied to the VDD pin of the device, both the outputs are held low until VDD exceeds the UVLO threshold, typically 5 V. Any UVLO condition on the bootstrap capacitor ($V_{HB–HS}$) disables only the high- side output (HO).

Table 7-1. VDD UVLO Logic Operation

Condition (V_{HB-HS} > V_{HBR}	HI	LI	HO	LO
V_{DD}-V_{SS} < V_{DDR} during device start-up	H	L	L	L
	L	H	L	L
	H	H	L	L
	L	L	L	L
V_{DD}-V_{SS} < V_{DDR} – V_{DDH} after device start-up	H	L	L	L
	L	H	L	L
	H	H	L	L
	L	L	L	L

Table 7-2. HB UVLO Logic Operation

Condition (V_{DD} > V_{DDR}	HI	LI	HO	LO
V_{HB-HS} < V_{HBR} during device start-up	H	L	L	L
	L	H	L	H
	H	H	L	H
	L	L	L	L
V_{HB-HS} < V_{HBR} – V_{HBH} after device start-up	H	L	L	L
	L	H	L	H
	H	H	L	H
	L	L	L	L

7.3.2 Input Stage

The two inputs operate independent of each other and also independent of VDD. The independence allows for full control of two outputs compared to the gate drivers that have a single input. The overlap of inputs and therefore respective outputs allow the use in applications such as secondary side synchronous rectification. Whenever both the inputs are high, both the outputs shall be high as well. In other words, the outputs follow the input logic in all operating conditions except when the driver is in UVLO mode. There is no fixed time de-glitch filter implemented in the device and therefore propagation delay and delay matching are not sacrificed. In other words, there is no built-in dead-time feature. Because the inputs are independent of supply voltage, they can be connected to outputs of either digital controller or analog controller. Inputs can accept wide slew rate signals and input can withstand negative voltage to increase the robustness. Small filter at the inputs of the driver further improves system robustness in noise prone applications. The inputs have internal pull down resistors with typical value of 250 kΩ. Thus, when the inputs are floating, the outputs are held low.

7.3.3 Level Shifter

The level shift circuit is the interface from the high-side input, which is a VSS referenced signal, to the high-side driver stage which is referenced to the switch node (HS pin). The level shift allows control of the HO output which is referenced to the HS pin. The delay introduced by the level shifter is kept as low as possible and therefore the device provides excellent propagation delay characteristic and delay matching with the low-side driver output. Low delay matching allows power stages to operate with less dead time. The reduction in dead-time is very important in applications where high efficiency is required.

7.3.4 Output Stage

The output stages are the interface from level shifter output to the power MOSFETs in the power train. High slew rate, low resistance, and high peak current capability of both outputs allow for efficient switching of the power MOSFETs. The low-side output stage is referenced to VSS and the high-side is referenced to HS. The device output stages are robust to handle harsh environment, such as –2 V transient for 100 ns. The device can also sustain positive transients on the outputs. The device output stages feature a pull-up structure which delivers the highest peak source current when it is most needed, during the Miller plateau region of the power switch turn on transition. The output pull-up and pull-down structure of the device is totem pole NMOS-PMOS structure.

7.3.5 Negative Voltage Transients

In most applications, the body diode of the external low-side power MOSFET clamps the HS node to ground. In some situations, board capacitances and inductances can cause the HS node to transiently swing several volts below ground, before the body diode of the external low-side MOSFET clamps this swing. When used in conjunction with the UCC27284-Q1, the HS node can swing below ground as long as specifications are not violated and conditions mentioned in this section are followed.

HS must always be at a lower potential than HO. Pulling HO more negative than specified conditions can activate parasitic transistors which may result in excessive current flow from the HB supply. This may result in damage to the device. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and VSS to protect the device from this type of transient. The diode must be placed as close to the device pins as possible in order to be effective.

Ensure that the HB to HS operating voltage is 16 V or less. Hence, if the HS pin transient voltage is –5 V, then VDD (and thus HB) is ideally limited to 11 V to keep the HB to HS voltage below 16 V. Generally when HS swings negative, HB follows HS instantaneously and therefore the HB to HS voltage does not significantly overshoot.

Low ESR bypass capacitors from HB to HS and from VDD to VSS are essential for proper operation of the gate driver device. The capacitor should be located at the leads of the device to minimize series inductance. The peak currents from LO and HO can be quite large. Any series inductances with the bypass capacitor causes voltage ringing at the leads of the device which must be avoided for reliable operation.

Based on application board design and other operating parameters, along with HS pin, other pins such as inputs, HI and LI, might also transiently swing below ground. To accommodate such operating conditions UCC27284-Q1 input pins are capable of handling absolute maximum of -5V. As explained earlier, based on the layout and other design constraints, some times the outputs, HO and LO, might also see transient voltages for short durations. Therefore, UCC27284-Q1 gate drivers can also handle -2 V 100 ns transients on output pins, HO and LO.

7.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See Section 7.3.1 for more information on UVLO operation mode. In normal mode when the V_{DD} and $V_{HB–HS}$ are above UVLO threshold, the output stage is dependent on the states of the HI and LI pins. The output HO and LO will be low if input state is floating.

Table 7-3. Input/Output Logic in Normal Mode of Operation

HI	LI	HO (1)	LO (2)
H	H	H	H
L	H	L	H
H	L	H	L
L	L	L	L
Floating	L	L	L
Floating	H	L	H
L	Floating	L	L
H	Floating	H	L
Floating	Floating	L	L

(1) HO is measured with respect to HS
(2) LO is measured with respect to VSS

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Most electronic devices and applications are becoming more and more power hungry. These applications are also reducing in overall size. One way to achieve both high power and low size is to improve the efficiency and distribute the power loss optimally. Most of these applications employ power MOSFETs and they are being switched at higher and higher frequencies. To operate power MOSFETs at high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gates of the power semiconductor devices, such as power MOSFETs, IGBTs, SiC FETs, and GaN FETs. Many of these applications require proper UVLO protection so that power semiconductor devices are turned ON and OFF optimally. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. A level-shift circuit is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V or 5 V) in order to fully turn-on the power device, minimize conduction losses, and minimize the switching losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement prove inadequate with digital power because they lack level-shifting capability and under voltage lockout protection. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also solve other problems such as minimizing the effect of high-frequency switching noise (by placing the high-current driver device physically close to the power switch), driving gate-drive transformers and controlling floating power device gates. This helps reduce power dissipation and thermal stress in controllers by moving gate charge power losses from the controller IC to the gate driver.

UCC27284-Q1 gate drivers offer high voltage (100 V), small delays (16 ns), and good driving capability (2.5 A/3.5 A) in a single device. The floating high-side driver is capable of operating with switch node voltages up to 100 V. This allows for N-channel MOSFETs control in half-bridge, full-bridge, synchronous buck, synchronous boost, and active clamp topologies. UCC27284-Q1 gate driver IC also has built-in bootstrap diode to help power supply designers optimize PWB area and to help reduce bill of material cost in most applications. Each channel is controlled by its respective input pins (HI and LI), allowing flexibility to control ON and OFF state of the output.

Switching power devices such as MOSFETs have two main loss components; switching losses and conduction losses. Conduction loss is dominated by current through the device and ON resistance of the device. Switching losses are dominated by gate charge of the switching device, gate voltage of the switching device, and switching frequency. Applications where operating switching frequency is very high, the switching losses start to significantly impact overall system efficiency. In such applications, to reduce the switching losses it becomes essential to reduce the gate voltage. The gate voltage is determined by the supply voltage the gate driver ICs, therefore, the gate driver IC needs to operate at lower supply voltage in such applications. UCC27284-Q1 gate driver has typical UVLO level of 5V and therefore, they are perfectly suitable for such applications. There is enough UVLO hysteresis provided to avoid any chattering or nuisance tripping which improves system robustness.

8.2 Typical Application

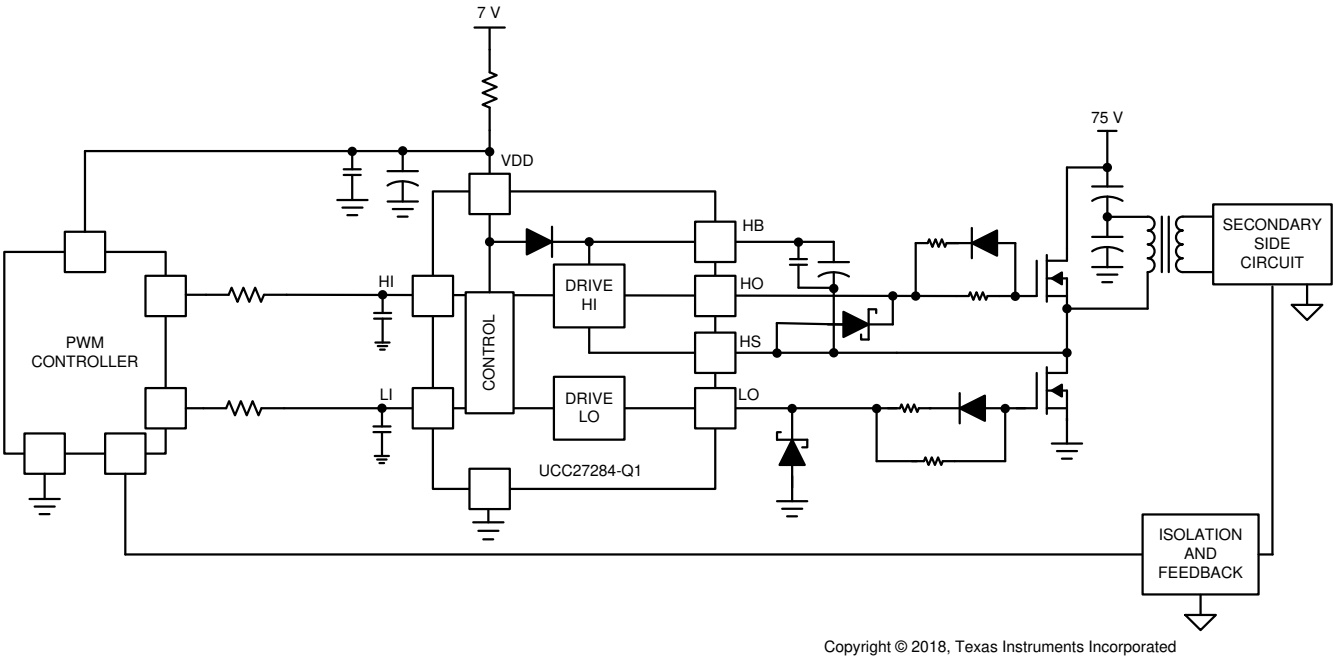


Figure 8-1. Typical Application

8.2.1 Design Requirements

Table below lists the system parameters. UCC27284-Q1 needs to operate satisfactorily in conjunction with them.

Table 8-1. Design Requirements

Parameter	Value
MOSFET	CSD19535KTT
Maximum Bus/Input Voltage, V_{in}	75V
Operating Bias Voltage, V_{DD}	7V
Switching Frequency, Fsw	300kHz
Total Gate Charge of FET at given VDD, Q_G	52nC
MOSFET Internal Gate Resistance, R_{GFET_Int}	1.4
Maximum Duty Cycle, D_{Max}	0.5
Gate Driver	UCC27284-Q1

8.2.2 Detailed Design Procedure

8.2.2.1 Select Bootstrap and VDD Capacitor

The bootstrap capacitor must maintain the V_{HB-HS} voltage above the UVLO threshold for normal operation. Calculate the maximum allowable drop across the bootstrap capacitor, ΔV_{HB}, with Equation 1.

$$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL} = (7\text{ V} - 1\text{ V} - (4.4\text{ V} - 0.37\text{ V})) = 1.97\text{ V} \quad (1)$$

where

- V_{DD} is the supply voltage of gate driver device
- V_{DH} is the bootstrap diode forward voltage drop
- V_{HBL} is the HB falling threshold ($V_{HBR(max)} - V_{HBH}$)

In this example the allowed voltage drop across bootstrap capacitor is 1.97 V.

It is generally recommended that ripple voltage on both the bootstrap capacitor and VDD capacitor should be minimized as much as possible. Many of commercial, industrial, and automotive applications use ripple value of 0.5 V.

Use Equation 2 to estimate the total charge needed per switching cycle from bootstrap capacitor.

$$Q_{TOTAL} = Q_G + I_{HBS} \times \left(\frac{D_{MAX}}{f_{SW}}\right) + \left(\frac{I_{HB}}{f_{SW}}\right)$$
$$= 52\ nC + 0.083\ nC + 1.33\ nC = 53.41\ nC \quad (2)$$

where

- Q_G is the total MOSFET gate charge
- I_{HBS} is the HB to VSS leakage current from datasheet
- D_{Max} is the converter maximum duty cycle
- I_{HB} is the HB quiescent current from the datasheet

The caculated total charge is 53.41 nC.

Next, use Equation 3 to estimate the minimum bootstrap capacitor value.

$$C_{BOOT\ (min)} = \frac{Q_{TOTAL}}{\Delta V_{HB}} = \frac{53.41\ nC}{1.97\ V} = 27.11\ nF \quad (3)$$

The calculated value of minimum bootstrap capacitor is 27.11 nF. It should be noted that, this value of capacitance is needed at full bias voltage. In practice, the value of the bootstrap capacitor must be greater than calculated value to allow for situations where the power stage may skip pulse due to various transient conditions. It is recommended to use a 100-nF bootstrap capacitor in this example. It is also recommenced to include enough margin and place the bootstrap capacitor as close to the HB and HS pins as possible. Also place a small size, 0402, low value, 1000 pF, capacitor to filter high frequency noise, in parallel with main bypass capacitor.

For this application, choose a C_{BOOT} capacitor that has the following specifications: 0.1 µF, 25 V, X7R

As a general rule the local VDD bypass capacitor must be greater than the value of bootstrap capacitor value (generally 10 times the bootstrap capacitor value). For this application choose a C_{VDD} capacitor with the following specifications: 1 µF , 25 V, X7R

C_{VDD} capacitor is placed across VDD and VSS pin of the gate driver. Similar to bootstrap capacitors, place a small size and low value capacitor in parallel with the main bypass capacitor. For this application, choose 0402, 1000 pF, capacitance in parallel with main bypass capacitor to filter high frequency noise.

The bootstrap and bias capacitors must be ceramic types with X7R dielectric or better. Choose a capacitor with a voltage rating at least twice the maximum voltage that it will be exposed to. Choose this value because most ceramic capacitors lose significant capacitance when biased. This value also improves the long term reliability of the system.

8.2.2.2 Estimate Driver Power Losses

The total power loss in gate driver device such as the UCC27284-Q1 is the summation of the power loss in different functional blocks of the gate driver device. These power loss components are explained in this section.

1. Equation 4 describes how quiescent currents (I_{DD} and I_{HB}) affect the static power losses, P_{QC}.

$$P_{QC} = (V_{DD} \times I_{DD}) + (V_{DD} - V_{DH}) \times I_{HB}$$
$$= 7\ V \times 0.4\ mA + 6\ V \times 0.4\ mA = 5.2\ mW \quad (4)$$

   it is not shown here, but for better approximation, add no load operating current, I_{DDO} and I_{HBO} in above equation.
2. Equation 5 shows how high-side to low-side leakage current (I_{HBS}) affects level-shifter losses (P_{IHBS}).

$$P_{HBS} = V_{HB} \times I_{HBS} \times D = 82\,V \times 50\,\mu A \times 0.5 = 2.05\,mW \quad (5)$$

where

- D is the high-side MOSFET duty cycle
- V_{HB} is the sum of input voltage and voltage across bootstrap capacitor.

3. Equation 6 shows how MOSFETs gate charge (Q_G) affects the dynamic losses, P_{QG}.

$$P_{QG} = 2 \times V_{DD} \times Q_G \times f_{SW} \times \frac{R_{GD\_R}}{R_{GD\_R} + R_{GATE} + R_{GFET\,(int)}}$$
$$= 2 \times 7\,V \times 52\,nC \times 300\,kHz \times 0.74 = 0.16\,W \quad (6)$$

where

- Q_G is the total MOSFET gate charge
- f_{SW} is the switching frequency
- R_{GD_R} is the average value of pullup and pulldown resistor
- R_{GATE} is the external gate drive resistor
- $R_{GFET(int)}$ is the power MOSFETs internal gate resistor

Assume there is no external gate resistor in this example. The average value of maximum pull-up and pull down resistance of the driver output section is approximately 4 Ω. Substitute the application values to calculate the dynamic loss due to gate charge, which is 160 mW here.

4. Equation 7 shows how parasitic level-shifter charge (Q_P) on each switching cycle affects dynamic losses, (P_{LS}) during high-side switching.

$$P_{LS} = V_{HB} \times Q_P \times f_{SW} \quad (7)$$

For this example and simplicity, it is assumed that value of parasitic charge Q_P is 1 nC. Substituting values results in 24.6 mW as level shifter dynamic loss. This estimate is very high for level shifter dynamic losses.

The sum of all the losses is 191.85 mW as a total gate driver loss. As shown in this example, in most applications the dynamic loss due to gate charge dominates the total power loss in gate driver device. For gate drivers that include bootstrap diode, one should also estimate losses in bootstrap diode. Diode forward conduction loss is computed as product of average forward voltage drop and average forward current.

Equation 8 estimates the maximum allowable power loss of the device for a given ambient temperature.

$$P_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \quad (8)$$

where

- P_{MAX} is the maximum allowed power dissipation in the gate driver device
- T_J is the recommended maximum operating junction temperature
- T_A is hte ambient temperature of the gate driver device
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance

To better estimate the junction temperature of the gate driver device in the application, it is recommended to first accurately measure the case temperature and then determine the power dissipation in a given application. Then use ψ_{JT} to calculate junction temperature. After estimating junction temperature and measuring ambient temperature in the application, calculate $\theta_{JA(effective)}$. Then, if design parameters (such as the value of an external gate resistor or power MOSFET) change during the development of the project, use $\theta_{JA(effective)}$ to estimate how these changes affect junction temperature of the gate driver device.

For detailed information regarding the thermal information table, please refer to the *Semiconductor and Device Package Thermal Metrics* application report.

8.2.2.3 Selecting External Gate Resistor

In high-frequency switching power supply applications where high-current gate drivers such as the UCC27284-Q1 are used, parasitic inductances, parasitic capacitances and high-current loops can cause noise and ringing on the gate of power MOSFETs. Often external gate resistors are used to damp this ringing and noise. In some applications the gate charge, which is load on gate driver device, is significantly larger than gate driver peak output current capability. In such applications external gate resistors can limit the peak output current of the gate driver. it is recommended that there should be provision of external gate resistor whenever the layout or application permits.

Use Equation 9 to calculate the driver high-side pull-up current.

$$I_{OHH} = \frac{V_{DD} - V_{DH}}{R_{HOH} + R_{GATE} + R_{GFET(int)}} \quad (9)$$

where

- I_{OHH} is the high-side, peak pull-up current
- V_{DH} is the bootstrap diode forward voltage drop
- R_{HOH} is the gate driver internal high-side pull-up resistor. Value either directly provided in datasheet or can be calculated from test conditions ($R_{HOH} = V_{HOH}/I_{HO}$)
- R_{GATE} is the external gate resistance connected between driver output and power MOSFET gate
- $R_{GFET(int)}$ is the MOSFET internal gate resistance provided by MOSFET datasheet

Use Equation 10 to calculate the driver high-side sink current.

$$I_{OLH} = \frac{V_{DD} - V_{DH}}{R_{HOL} + R_{GATE} + R_{GFET(int)}} \quad (10)$$

where

- R_{HOL} is the gate driver internal high-side pull-down resistance

Use Equation 11 to calculate the driver low-side source current.

$$I_{OHL} = \frac{V_{DD}}{R_{LOH} + R_{GATE} + R_{GFET(int)}} \quad (11)$$

where

- R_{LOH} is the gate driver internal low-side pull-up resistance

Use Equation 12 to calculate the driver low-side sink current.

$$I_{OLL} = \frac{V_{DD}}{R_{LOL} + R_{GATE} + R_{GFET(int)}} \quad (12)$$

where

- R_{LOL} is the gate driver internal low-side pull-down resistance

Typical peak pull up and pull down current of the device is 2.5 A and 3.5 A respectively. These equations help reduce the peak current if needed. To establish different rise time value compared to fall time value, external gate resistor can be anti-paralleled with diode-resistor combination as shown in Section 8.2. Generally selecting an optimal value or configuration of external gate resistor is an iterative process. For additional information on selecting external gate resistor please refer to External Gate Resistor Design Guide for Gate Drivers

8.2.2.4 Delays and Pulse Width

The total delay encountered in the PWM, driver and power stage need to be considered for a number of reasons, primarily delay in current limit response. Also to be considered are differences in delays between the drivers which can lead to various concerns depending on the topology. The synchronous buck topology switching requires careful selection of dead-time between the high-side and low-side switches to avoid cross conduction as well as excessive body diode conduction.

Bridge topologies can be affected by a volt-second imbalance on the transformer if there is imbalance in the high-side and low-side pulse widths in any operating condition. The UCC27284-Q1 device has maximum propagation delay, across process, and temperature variation, of 30 ns and delay matching of 7 ns, which is one of the best in the industry.

Narrow input pulse width performance is an important consideration in gate driver devices, because output may not follow input signals satisfactorily when input pulse widths are very narrow. Although there may be relatively wide steady state PWM output signals from controller, very narrow pulses may be encountered under following operating conditions.

- soft-start period
- large load transients
- short circuit conditions

These narrow pulses appear as an input signal to the gate driver device and the gate driver device need to respond properly to these narrow signals.

Figure 8-2 shows that the UCC27284-Q1 device produces reliable output pulse even when the input pulses are very narrow and bias voltages are very low. The propagation delay and delay matching do not get affected when the input pulse width is very narrow.

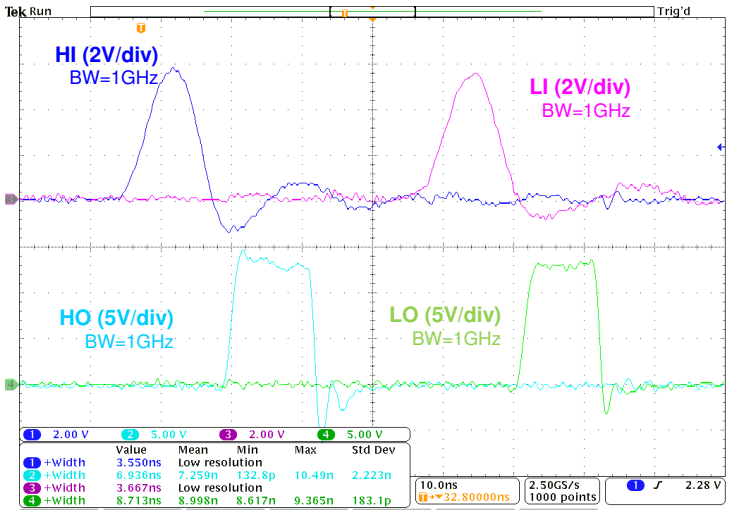


Figure 8-2. Input and Output Pulse Width

8.2.2.5 External Bootstrap Diode

The UCC27284-Q1 incorporates the bootstrap diode necessary to generate the high-side bias for HO to work satisfactorily. The characteristics of this diode are important to achieve efficient, reliable operation. The characteristics to consider are forward voltage drop and dynamic resistance. Generally, low forward voltage drop diodes are preferred for low power loss during charging of the bootstrap capacitor. The device has a boot diode forward voltage drop rated at 0.85 V and dynamic resistance of 1.5 Ω for reliable charge transfer to the bootstrap capacitor. The dynamic characteristics to consider are diode recovery time and stored charge. Diode recovery times that are specified without operating conditions, can be misleading. Diode recovery times at no forward current (I_F) can be noticeably less than with forward current applied. The UCC27284-Q1 boot diode recovery is specified as 50 ns at I_F = 20 mA, I_{REV} = 0.5 A. Dynamic impedance of UCC27284-Q1 bootstrap diode naturally

limits the peak forward current and prevents any damage if repetitive peak forward current pulses exist in the system for most applications.

In applications where switching frequencies are very high, for example in excess of 1 MHz, and the low-side minimum pulse widths are very small, the diode peak forward current could be very high and peak reverse current could also be very high, specifically if high bootstrap capacitor value has been chosen. In such applications it might be advisable to use external Schottkey diode as bootstrap diode. It is safe to at least make a provision for such diode on the board if possible.

8.2.2.6 VDD and Input Filter

Some switching power supply applications are extremely noisy. Noise may come from ground bouncing and ringing at the inputs, (which are the HI and LI pins of the gate driver device). To mitigate such situations, the UCC27284-Q1 offers both negative input voltage handling capability and wide input threshold hysteresis. If these features are not enough, then the application might need an input filter. Small filter such as 10-Ω resistor and 47-pF capacitor might be sufficient to filter noise at the inputs of the gate driver device. This RC filter would introduce delay and therefore need to be considered carefully. High frequency noise on bias supply can cause problems in performance of the gate driver device. To filter this noise it is recommended to use 1-Ω resistor in series with bias supply as shown in Typical Application diagram. This resistor also acts as a current limiting element. In the event of short circuit on the bias rail, this resistor opens up and prevents further damage. This resistor can also be helpful in debugging the design during development phase.

8.2.2.7 Transient Protection

As mentioned in previous sections, high power high switching frequency power supplies are inherently noisy. High dV/dt and dI/dt in the circuit can cause negative voltage on different pins such as HO, LO, and HS. The device tolerates negative voltage on all of these pins as mentioned in specification tables. If parasitic elements of the circuit cause very large negative swings, circuit might require additional protection. In such cases fast acting and low leakage type Schottky diode should be used. This diode must be placed as close to the gate driver device pin as possible for it to be effective in clamping excessive negative voltage on the gate driver device pin. To avoid the possibility of driver device damage due to over-voltage on its output pins or supply pins, low leakage Zener diode can be used. A 15-V Zener diode is often sufficient to clamp the voltage below the maximum recommended value of 16 V.

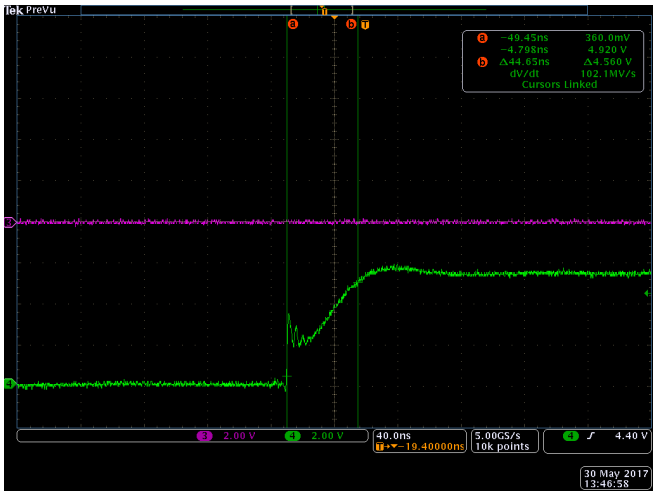
8.2.3 Application Curves

To minimize the switching losses in power supplies, turn-ON and turn-OFF of the power MOSFETs need to be as fast as possible. Higher the drive current capability of the driver, faster the switching. Therefore, the UCC27284-Q1 is designed with high drive current capability and low resistance of the output stages. One of the common way to test the drive capability of the gate driver device , is to test it under heavy load. Rise time and fall time of the outputs would provide idea of drive capability of the gate driver device. There must not be any resistance in this test circuit. Figure 8-3 and Figure 8-4 shows rise time and fall time of HO respectively of UCC27284-Q1. Figure 8-5 and Figure 8-6 shows rise time and fall time of LO respectively of UCC27284-Q1. For accuracy purpose, the VDD and HB pin of the gate driver device were connected together. HS and VSS pins are also connected together for this test.

Peak current capability can be estimated using the fastest dV/dt along the rise and fall curve of the plot. This method is also useful in comparing performance of two or more gate driver devices.

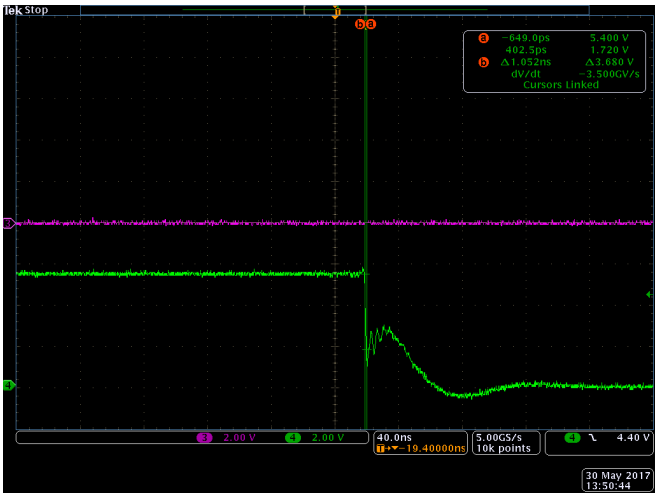
As explained in Section 8.2.2.4, propagation delay plays an important role in reliable operation of many applications. Figure 8-7 and Figure 8-8

Figure 8-8 shows propagation delay and delay matching of UCC27284-Q1. Figure 8-9 shows input negative voltage handling capability of UCC27284-Q1.



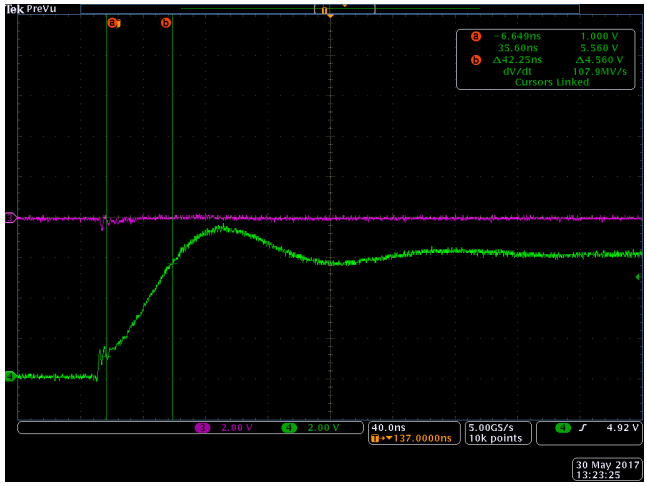
V_{DD} = V_{HB} = 6 V, HS = VSS C_{LOAD} = 10 nF Ch4 = HO

Figure 8-3. HO Rise Time



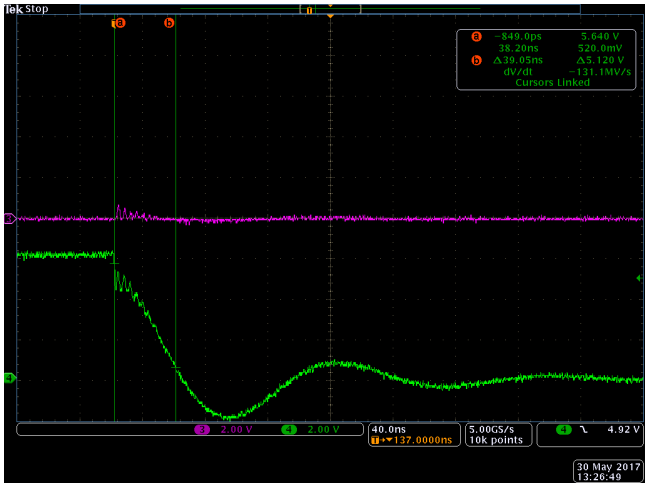
V_{DD} = V_{HB}=6 V, HS = VSS C_{LOAD} = 10 nF Ch4 = HO

Figure 8-4. HO Fall Time



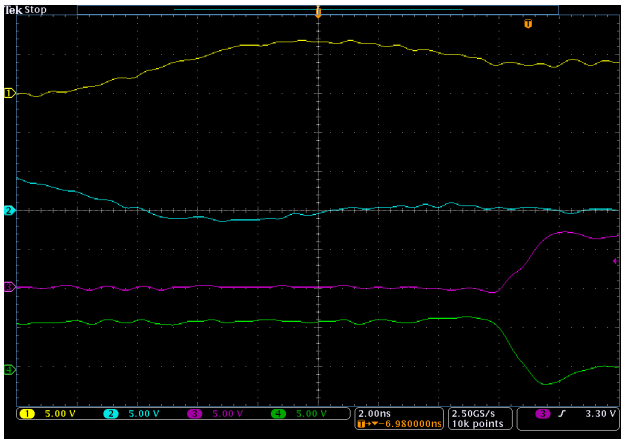
V_{DD} = V_{HB} = 6 V, HS = VSS C_{LOAD} = 10 nF Ch4 = LO

Figure 8-5. LO Rise Time



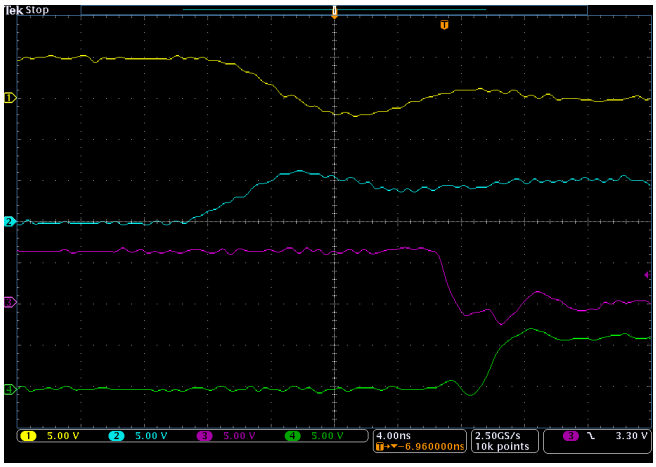
V_{DD} = V_{HB} = 6 V, HS = VSS C_{LOAD} = 10 nF Ch4 = LO

Figure 8-6. LO Fall Time



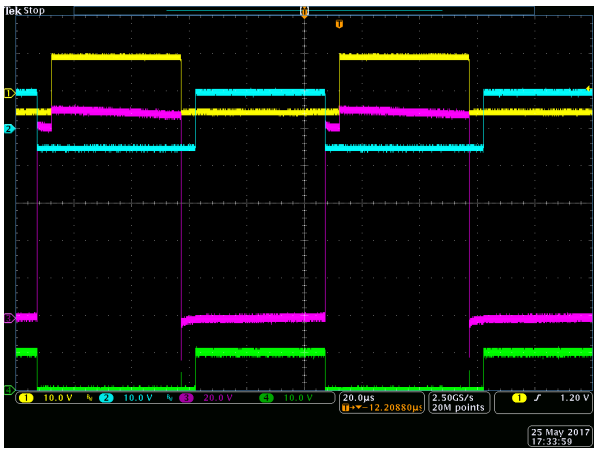
V_{DD} = 6 V C_{LOAD} = 2 nF Ch1 = HI Ch2 = LI Ch3 = HO Ch4 = LO

Figure 8-7. Propagation Delay and Delay Matching



V_{DD} = 6 V C_{LOAD} = 2 nF Ch1 = HI Ch2 = LI Ch3 = HO Ch4 = LO

Figure 8-8. Propagation Delay and Delay Matching



V_{DD} = 10 V V_{in} = 100 V C_L = 1 nF Ch1 = HI Ch2 = LI Ch3 = HO Ch4 = LO

Figure 8-9. Input Negative Voltage

9 Power Supply Recommendations

The recommended bias supply voltage range for UCC27284-Q1 is from 5.5 V to 16 V. The lower end of this range is governed by the internal under voltage-lockout (UVLO) protection feature, 5 V typical, of the V_{DD} supply circuit block. The upper end of this range is driven by the 16-V recomended maximum voltage rating of the V_{DD}. It is recommended that voltage on VDD pin should be lower than maximum recommended voltage. In some transient condition it is not possible to keep this voltage below recommended maximum level and therefore absolute maximum voltage rating of the UCC27284-Q1 is 20 V.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the V_{DD} voltage drops, the device continues to operate in normal mode as far as the voltage drop do not exceeds the hysteresis specification, V_{DDHYS}. If the voltage drop is more than hysteresis specification, the device shuts down. Therefore, while operating at or near the 5.5-V range, the voltage ripple on the auxiliary power supply output should be smaller than the hysteresis specification of UCC27284-Q1 to avoid triggering device shutdown.

A local bypass capacitor should be placed between the VDD and GND pins. This capacitor should be located as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is recommended to use two capacitors across VDD and GND: a low capacitance ceramic surface-mount capacitor for high frequency filtering placed very close to VDD and GND pin, and another high capacitance value surface-mount capacitor for device bias requirements. In a similar manner, the current pulses delivered by the HO pin are sourced from the HB pin. Therefore, two capacitors across the HB to HS are recommended. One low value small size capacitor for high frequency filtering and another one high capacitance value capacitor to deliver HO pulses.

In power supplies where noise is very dominant and there is space on the PWB (Printed Wiring Board), it is recommended to place a small RC filter at the inputs. This allows for improving the overall performance of the design. In such applications. it is also recommended to have a place holder for power MOSFET external gate resistor. This resistor allows the control of not only the drive capability but also the slew rate on HS, which impacts the performance of the high-side circuit. If diode is used across the external gate resistor, it is recommended to use a resistor in series with the diode, which provides further control of fall time.

In power supply applications such as motor drives, there exist lot of transients through-out the system. This sometime causes over voltage and under voltage spikes on almost all pins of the gate driver device. To increase the robustness of the design, it is recommended that the clamp diode should be used on HO and LO pins. If user does not wish to use power MOSFET parasitic diode, external clamp diode on HS pin is recommended, which needs to be high voltage high current type (same rating as MOSFET) and very fast acting. The leakage of these diodes across the temperature needs to be minimal.

In power supply applications where it is almost certain that there is excessive negative HS voltage, it is recommended to place a small resistor between the HS pin and the switch node. This resistance helps limit current into the driver device up to some extent. This resistor will impact the high side drive capability and therefore needs to be considered carefully.

10 Layout

10.1 Layout Guidelines

To achieve optimum performance of high-side and low-side gate drivers, one must consider following printed wiring board (PWB) layout guidelines.

- Low ESR/ESL capacitors must be connected close to the device between VDD and VSS pins and between HB and HS pins to support high peak currents drawn from VDD and HB pins during the turn-on of the external MOSFETs.
- To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the high side MOSFET drain and ground (VSS).
- In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances between the source of the high-side MOSFET and the source of the low-side MOSFET (synchronous rectifier) must be minimized.
- Overlapping of HS plane and ground (VSS) plane should be minimized as much as possible so that coupling of switching noise into the ground plane is minimized.
- Thermal pad should be connected to large heavy copper plane to improve the thermal performance of the device. Generally it is connected to the ground plane which is the same as VSS of the device. It is recommended to connect this pad to the VSS pin only.
- Grounding considerations:
  - The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This confinement decreases the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. Place the gate driver as close to the MOSFETs as possible.
  - The second consideration is the high current path that includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor, and the low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

10.2 Layout Example

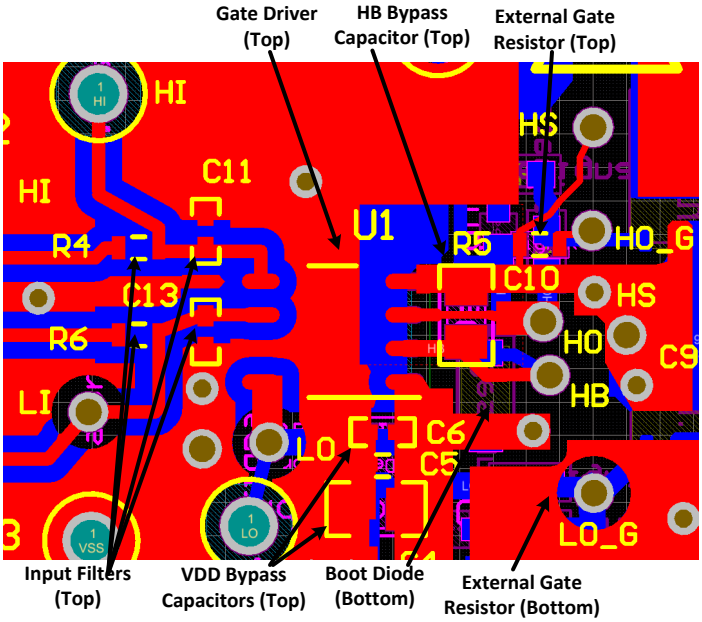


Figure 10-1. Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27284QDQ1	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U284Q	Samples
UCC27284QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U284Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

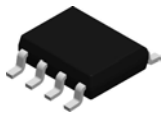
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC27284-Q1 :

- Catalog: UCC27284

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

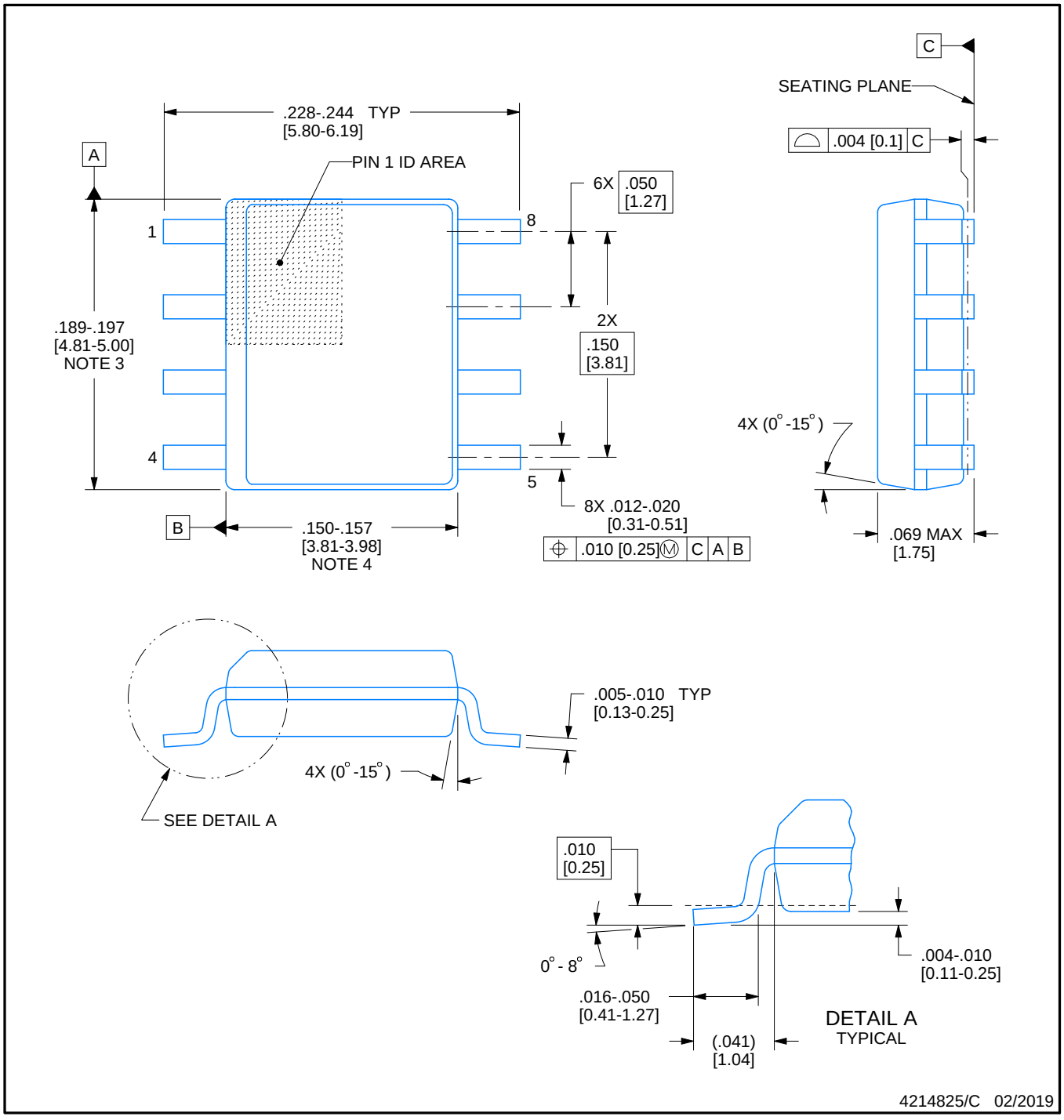


PACKAGE OUTLINE

D0008A

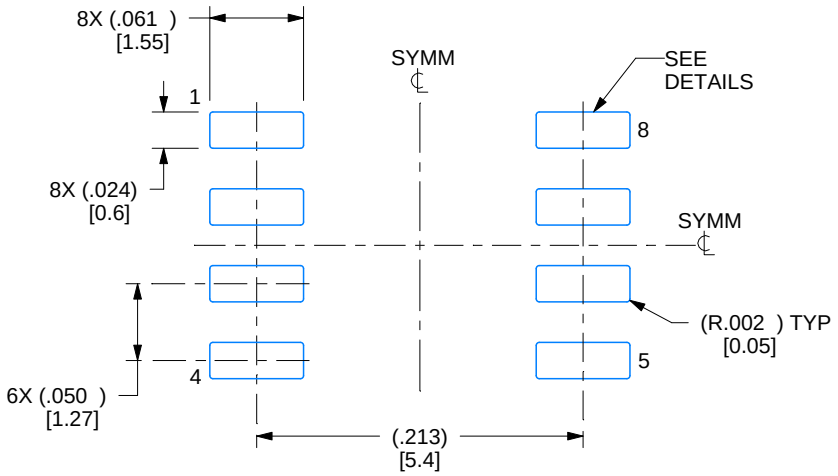
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

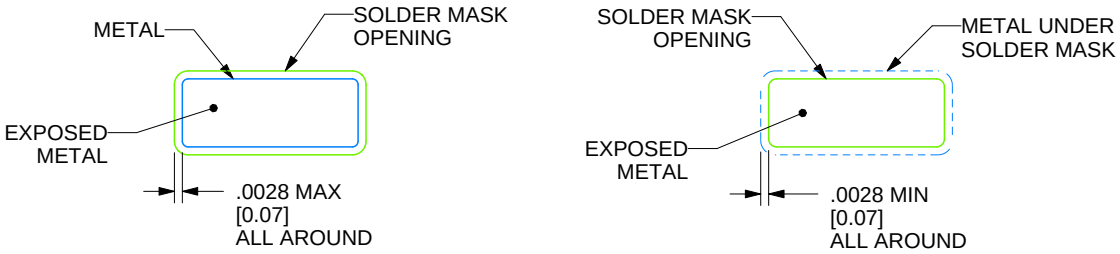


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

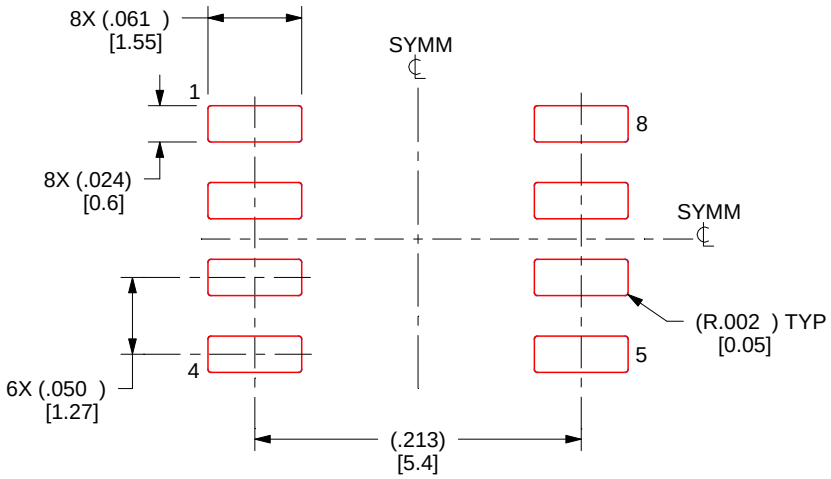
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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