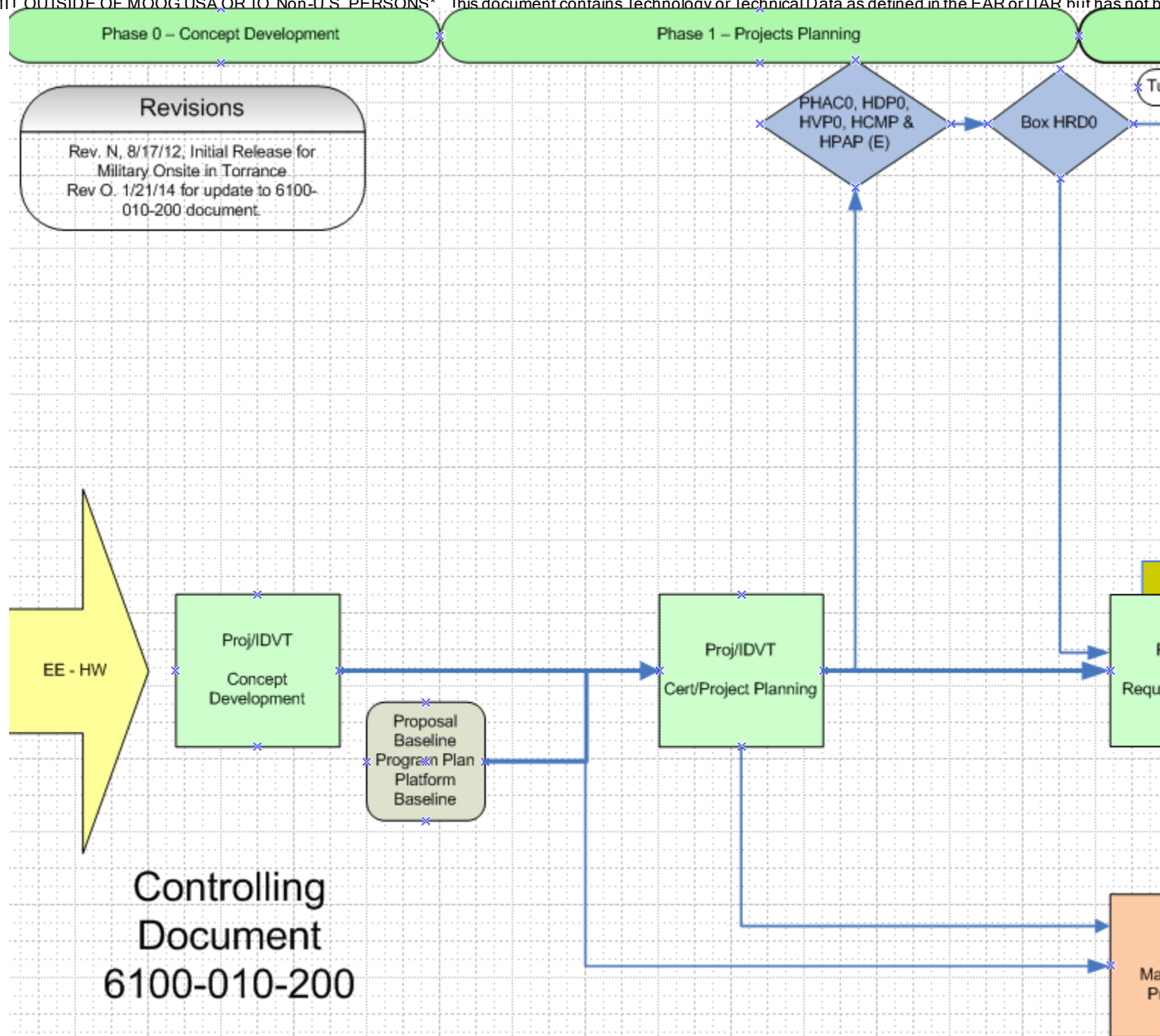
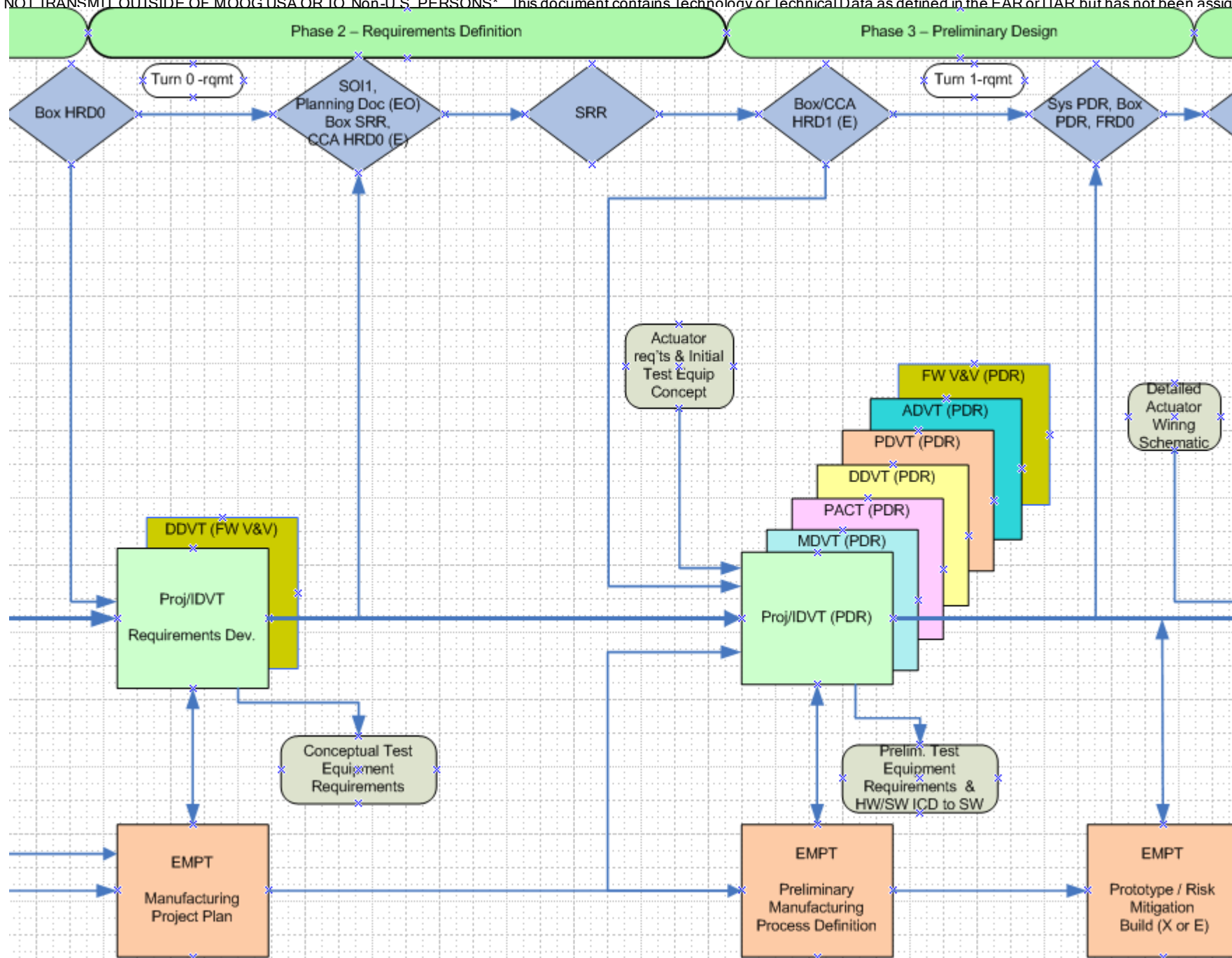
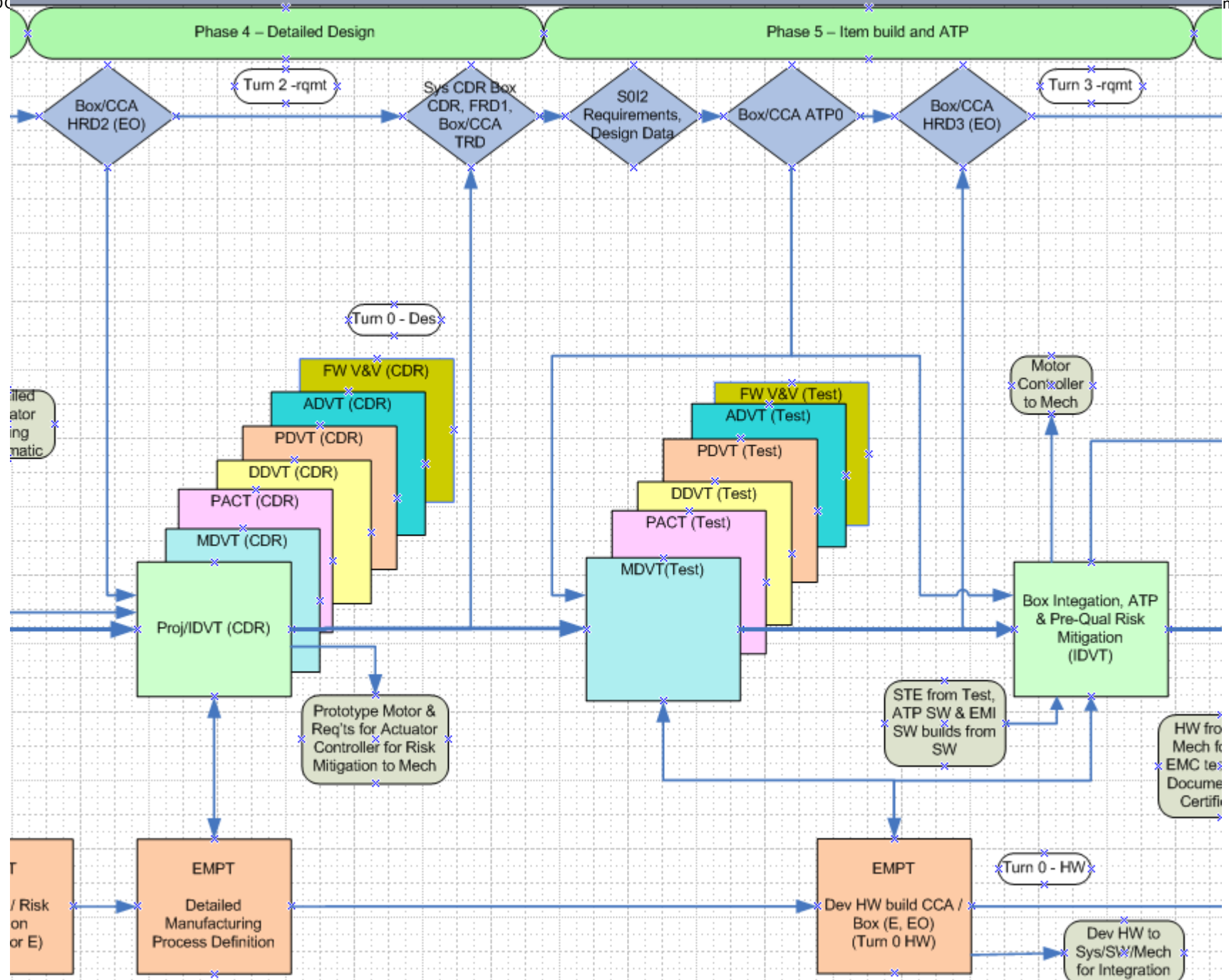
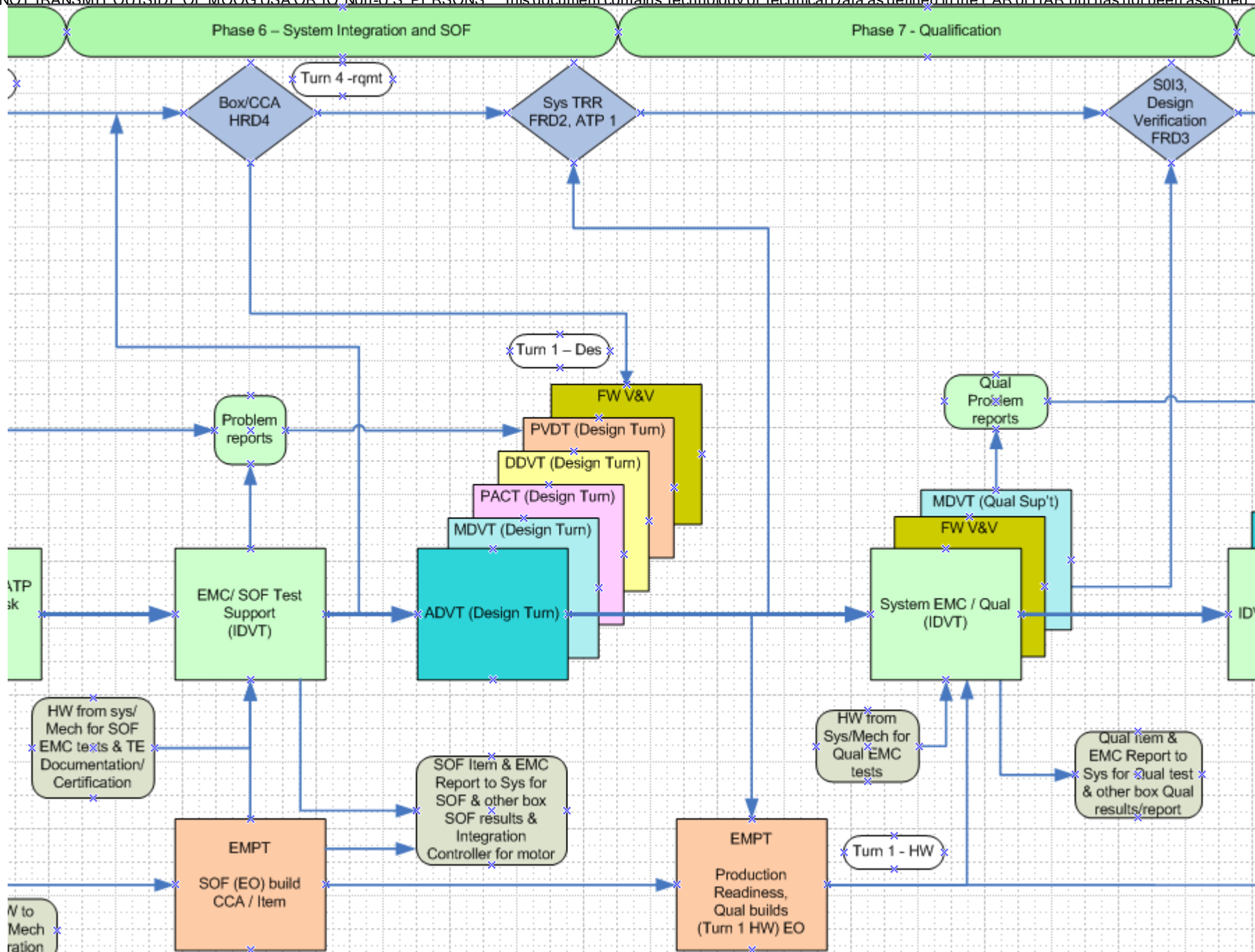


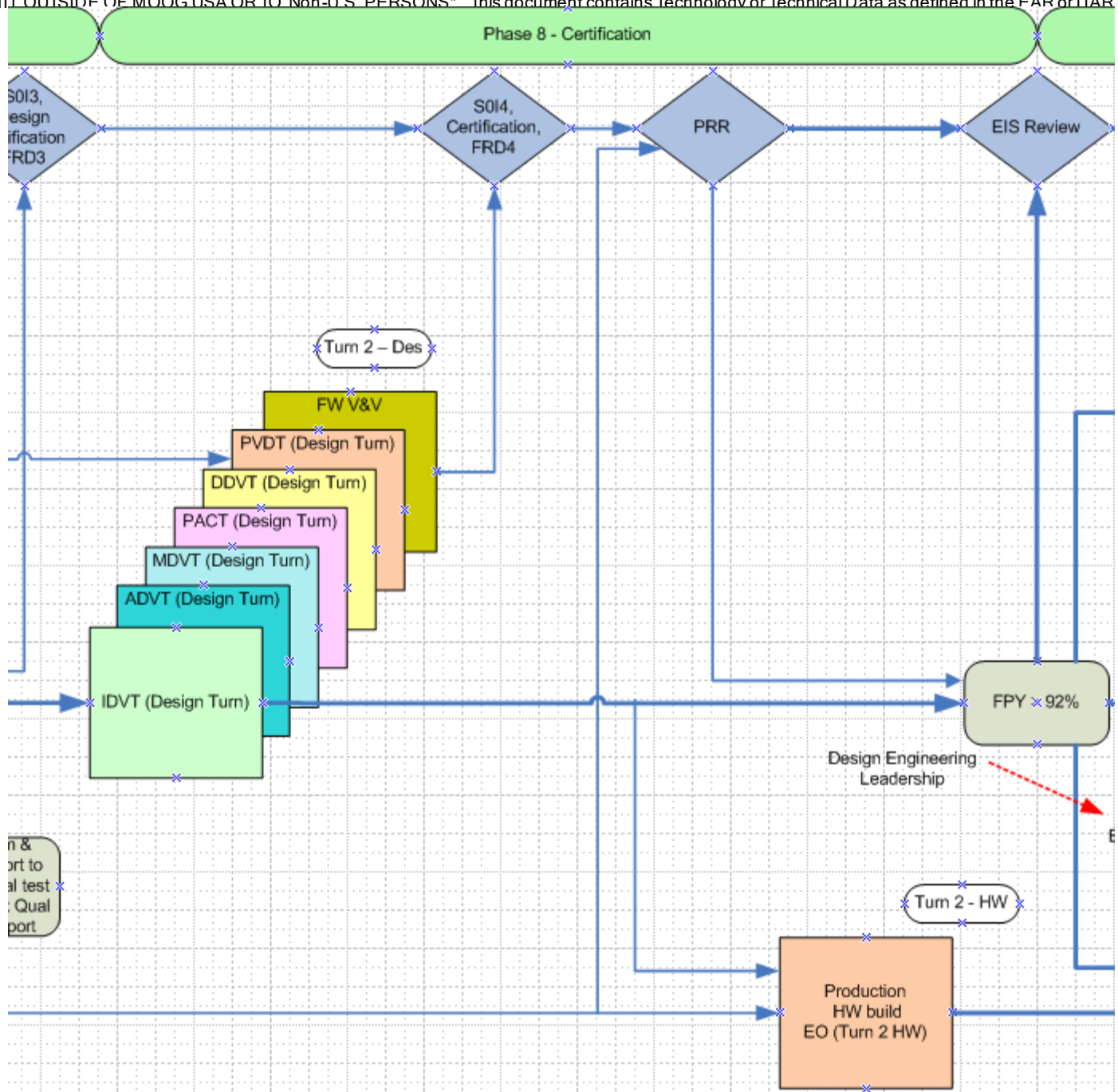
ACG Electronics Swimlane (Common Development Process)

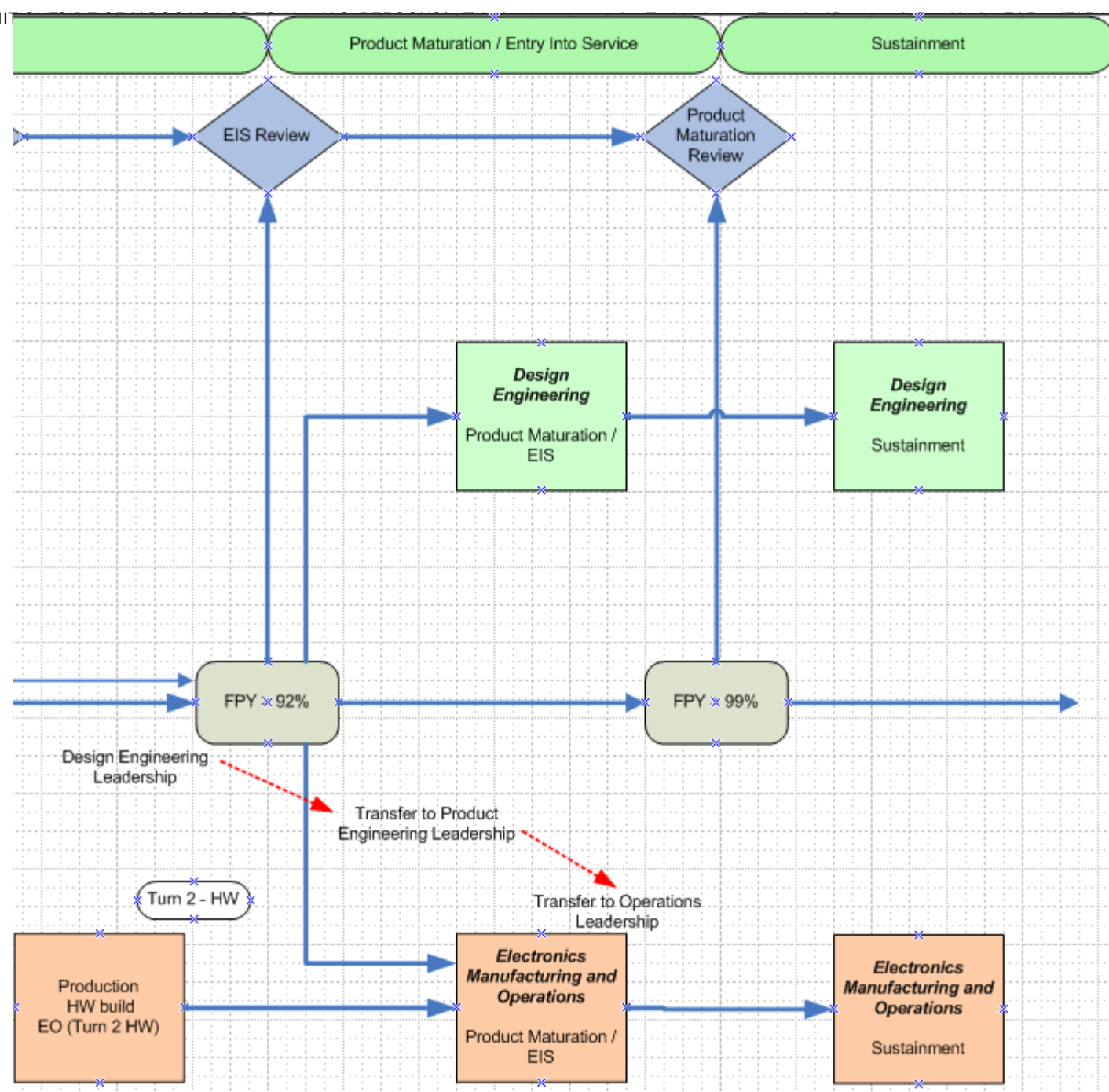












EE Work Packages Summary

Phase	Work Package	
1 (1152 hrs)	Project Planning	IDVT WP1
2 (2712 hrs)	Requirements Definition	IDVT WP2
		DDVT WP3
	Manufacturing Project Planning	EMPT WP4
3 (6574 hrs)	Preliminary Design	IDVT WP5
		DDVT WP6
		Fwr V&V WP7
		ADVT WP8
		PDVT WP9
		PACT WP10
		MDVT WP11
	Preliminary Mfg Process Definition & Prototype/Risk Mitigation Build	EMPT WP12

IDVT	Item Design Verification and Test
DDVT	Digital Design Verification and Test
Fwr V&V	Firmware V&V
ADVT	Analog Design Verification and Test
PDVT	Power Design Verification and Test
PACT	Packaging Design Verification and Test
MDVT	Motor Design Verification and Test
EMPT	Electronics Manufacturing Process and Test

Phase	Work Package	
4 (12462 hrs)	Detailed Design	IDVT WP13
		DDVT WP14
		Fwr V&V WP15
		ADVT WP16
		PDVT WP17
		PACT WP18
		MDVT WP19
	Detailed Mfg Process Definition	EMPT WP20
5 (6456 hrs)	Item Build and ATP	IDVT WP21
		DDVT WP22
		Fwr V&V WP23
		ADVT WP24
		PDVT WP25
		PACT WP26
		MDVT WP27
	Dev HW Build CCA/Item	EMPT WP28

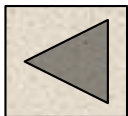
Phase	Work Package	
6 (3650 hrs)	System Integration and SOF	IDVT WP29
		DDVT WP30
		Fwr V&V WP31
		ADVT WP32
		PDVT WP33
		PACT WP34
		MDVT WP35
	SOF Build CCA/Item	EMPT WP36
7 (2520 hrs)	Qualification	IDVT WP37
		Fwr V&V WP38
	Production Readiness, Qual Builds	MDVT WP39
8 (3652 hrs)	Certification Support	EMPT WP40
		IDVT WP41
		DDVT WP42
		ADVT WP43
		PDVT WP44
		Fwr V&V WP45
		PACT WP46
		MDVT WP47
	Production HW Build	EMPT WP48
	Product Maturation / EIS	IDVT WP49
		EMPT WP50
	Sustainment	IDVT WP51
		EMPT WP52

Assumptions – High Voltage EM Box with 90% Reuse, 6 Unique CCAs, DO-254 Level A design, Microprocessor and PLD, BLDC Motor design with reuse of magnetic design (pole/slot)

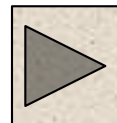


Phase 2 – Requirements Definition Work Packages

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Requirements Definition – VnV (DDVT) WP3

Inputs

Requirements

Board Requirement – HRD

Plans

V&V plans

PHAC, HVP, HDP, HPAP, HCMP

Guidelines / Standards

Requirement & Coding standard

Platform Functional Element –

VHDL core

Tasks / ETC

Preliminary PLD/Firmware definition

Identify the FEs / logic to be implemented in PLD (80)

Generate PLD high level block diagram (40)

Generate IO List (20)

Perform high level Timing analysis (80)

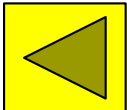
Update Planning Docs (80)

Create FRD0 (120)

Deliverables

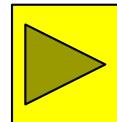
1. PLD block diagram and IO List – project file
2. SOI 1 - audit results in clear case (as required)
3. FRD0 (DDVT activity) – E release
4. 5. Planning Doc's Released (EO)

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summary page



Resources (420 hours)
DDVT (420)

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Phase 2 Exit Criteria

Phase 2 – Requirements Definition

<input type="checkbox"/> Complete, <input type="checkbox"/> N/A:	Box Block Diagram, project file (part of HRD)
<input type="checkbox"/> Complete, <input type="checkbox"/> N/A:	Grounding approach project file (part of HRD)
<input type="checkbox"/> Complete, <input type="checkbox"/> N/A:	ICD project file (part of HRD)
<input type="checkbox"/> Complete, <input type="checkbox"/> N/A:	LRU HRD (E release) - prelim baseline in Doors
<input type="checkbox"/> Complete, <input type="checkbox"/> N/A:	CCA HRDs as required (E release) – in Doors
<input type="checkbox"/> Complete, <input type="checkbox"/> N/A:	Drawing Tree MRE document (E release)
<input type="checkbox"/> Complete, <input type="checkbox"/> N/A:	Checklists / guidelines / templates distribution
<input type="checkbox"/> Complete, <input type="checkbox"/> N/A:	DFX goals project memo
<input type="checkbox"/> Complete, <input type="checkbox"/> N/A:	PLD block diagram and IO List – project file
<input type="checkbox"/> Complete, <input type="checkbox"/> N/A:	SOI 1 - audit results in clear case (as required)
<input type="checkbox"/> Complete, <input type="checkbox"/> N/A:	All Planning Doc's EO Released
<input type="checkbox"/> Complete, <input type="checkbox"/> N/A:	FRD0 (DDVT activity) – E release
<input type="checkbox"/> Complete, <input type="checkbox"/> N/A:	Control Plans (HV, EMC) - project memo



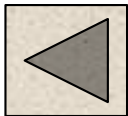
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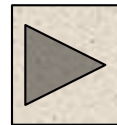


PH 3 – Preliminary Design Work Packages

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Preliminary Design – DDVT WP6

Inputs

Requirements

Box Requirements - HRD
CCA Requirement - HRD

Plans

DTC targets and DFMAT plans
Grounding Approach
Risk Mitigation Plan
Program IMS & ETCs

Guidelines

Platform Functional Elements
Guidelines & Checklists

Tasks / ETC

Design/Analysis

Generate Source Control Drawing as needed (40)
Generate Library models (60)
Generate Schematics (40, 60)
Generate BOM, DTC and Obsolescence report (60)
Perform PLD design activity (120)
Perform preliminary parts placement (80)
Perform Design Analysis / Sim – Stress, derating (80)
Update CCA HRD (80)

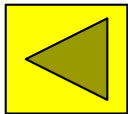
Reviews and other support

Prototype / Risk mitigation plan and testing (80/80)
Generate DFMAT compliance report (40)
Generate CCA Test equipment req't document (40)
Support Reliability / FMEA analysis (20)
Capture design data in repository (40)
Support Peer Review with EMC and SMEs (40)
Prepare PDR package (80)

Deliverables

- 1.Requirements - CCA HRD update as required (E release) Doors REV
- 2.Requirements – Preliminary Compliance Matrix (w ith MOC defined) (E release)
- 3.Trade Study, if needed – project memo
- 4.Area, power estimates, if needed – project memo
- 5.FRD1 REV update
- 6.Schematic Preliminary
Peer review with SME – project memo
- 7.Schematic Preliminary
(E release – if needed for prototype)
- 8.BOM, (E release – if needed for prototype)
- 9.BOM - DTC compliance & Obsolescence summary
project memo
- 10.ABOM – long lead items if needed
project memo or spread sheet
- 11.PDR review package – as required
- 12.PDR DDVT checklists

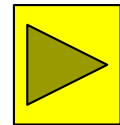
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Resources (1040 hours)

- DDVT (700 hrs)
- Components (120 hrs)
- PWB design (140 hrs)
- EE Tech (80 hrs)

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Phase 3 Exit Criteria

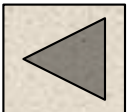
Phase 3 – Preliminary Design

1. ☐ Complete, ☐ N/A: Requirements - Box HRD update as required (E release) Doors REV
2. ☐ Complete, ☐ N/A: Requirements – Preliminary Compliance Matrix (with MOC defined) (E release)
3. ☐ Complete, ☐ N/A: Requirements - Box level requirements check list – clear case
4. ☐ Complete, ☐ N/A: Trade Study – if needed, project memo
5. ☐ Complete, ☐ N/A: Peer Review documentation with SME, project memo
6. ☐ Complete, ☐ N/A: Test Equipment req't document, project memo
7. ☐ Complete, ☐ N/A: DFMAT review with MFG, project memo
8. ☐ Complete, ☐ N/A: Requirements - CCA HRD, update as required (E release) Doors REV
9. ☐ Complete, ☐ N/A: Area, power estimates if needed – project memo
10. ☐ Complete, ☐ N/A: Schematic Preliminary Peer review with SME – project memo

Phase 3 Exit Criteria

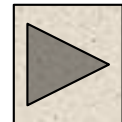
Phase 3 – Preliminary Design, cont...

- 11. ☐Complete, ☐N/A: Schematic Preliminary (E release – if needed for prototype)
- 12. ☐Complete, ☐N/A: BOM (E release – if needed for prototype)
- 13. ☐Complete, ☐N/A: BOM - DTC compliance & Obsolescence summary, project memo
- 14. ☐Complete, ☐N/A: ABOM – long lead items if needed, project memo or spread sheet
- 15. ☐Complete, ☐N/A: FRD1 REV update
- 16. ☐Complete, ☐N/A: Packaging - Preliminary 3D CAD model, (no release)
- 17. ☐Complete, ☐N/A: Packaging - Preliminary board DXF to CAD, (no release)
- 18. ☐Complete, ☐N/A: Packaging - Preliminary Assembly Drawing, (E release)
- 19. ☐Complete, ☐N/A: Packaging – Preliminary Analysis – Thermal, Vib, Fatigue, up
- 20. ☐Complete, ☐N/A: Packaging - Peer Review with SME, project memo
- 21. ☐Complete, ☐N/A: PDR review package – as required



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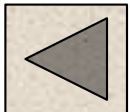
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Phase 3 Exit Criteria

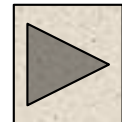
Phase 3 – Preliminary Design, cont...

- 21. ☐Complete, ☐N/A: Prelim. Top-level Assembly drawings – E released
- 22. ☐Complete, ☐N/A: Prelim. Motor Envelope
- 23. ☐Complete, ☐N/A: Prelim. Stator and Rotor Dims & weight
- 24. ☐Complete, ☐N/A: Prelim. Motor Design Data
- 25. ☐Complete, ☐N/A: Prelim Performance Analysis
- 26. ☐Complete, ☐N/A: Prelim Thermal analysis
- 27. ☐Complete, ☐N/A: Prelim. Stress analysis
- 28. ☐Complete, ☐N/A: Mechanical Components Design
- 29. ☐Complete, ☐N/A: Peer review Documentation (project)
- 30. ☐Complete, ☐N/A: Motor PDR package (project)
- 31. ☐Complete, ☐N/A: Prototype Motor BOM and detailed drawings as required (E release)
- 32. ☐Complete, ☐N/A: High Voltage Guideline (E release)
- 33. ☐Complete, ☐N/A: PDR Design Checklists completed



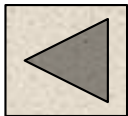
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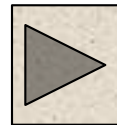


Phase 4 – Detail Design Work Packages

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Detailed Design – DDVT WP14

Inputs

Requirements

Box Requirement - HRD
CCA Req't Document - HRD
Firmware Requirements - FRD

Preliminary Design Documentation

Preliminary design data & Documents
Risk mitigation test results

Plans

V&V plans (PHAC, HVP, HDP)
DTC targets and DFMAT plans
Guidelines & Checklists
Program IMS & ETCs

Tasks

Requirements

Finalize block diagram (80)
Update CCA HRD and FRD (120)

Design

Finalize schematic (240)
Firmware design (360)
Test Benches (120)
Generate EDP (40)
Perform board layout / trace route (360)

Analysis

Finalize Design Analysis, Stress, Timing, Signal integrity (320)
Support Reliability / FMEA analysis (40)
Functional/post-route Simulation (160)
Generate requirement to design compliance matrix (160)

Components

Finalize BOM, DTC and Obsolescence (80)
Generate library models as needed (40)

Test

Generate board test requirements (240)
Finalize prototype risk testing (120)

Reviews / Reports

Schematic, layout and tracing routing review (80)
Update DMFAT compliance report (40)
Prepare CDR package (60)
Generate SDRL documents (60)
Prepare design doc – HDD (160)

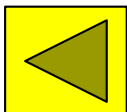
Resources :

- DDVT (2240 hrs)
- Components (120 hrs)
- PWB design (360 hrs)
- EE Tech (120 hrs)

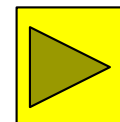
Deliverables

- 1.Design trade study – if needed project memo
- 2.Estimate - Area, power if needed project memo
- 3.Block diagram (CCA)
MRE document (EO release)
- 4.Requirement CCA card HRD – if needed (EO release) REV Doors – clear case
- 5.Requirement FRD2 REV, (EO release) – clear case
- 6.Schematic Peer Review
project memo – results of review with SME
- 7.Schematic checklist data base in team center
error report completed and resolved – team center
E release until built – EO release prior to qual
- 8.Board layout guidelines for each CCA (EDP)
team center
- 9.Board layout Peer Review, part place and trace routing
checklist – project file
- 10.BOM - (E release – EO release prior to qual)
- 11.BOM - DTC compliance and Obsolescence report
memo or spread sheet
- 12.Analysis (initial / final after qual) –
Derating / signal integrity/ timing analysis
project file / clear case
- 13.Test Procedure (E release)
- 14.CDR review package – as required
- 15.PLD Design – PLD source code
Captured in Clear case
- 16.Requirement derived justification - link
in Doors clear case
17. CDR DDVT checklists

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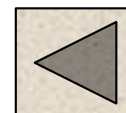


Phase 4 Exit Criteria

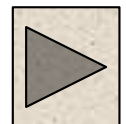
Phase 4 – Detailed Design

1. ☐ Complete, ☐ N/A: Block diagram (Box and Card) MRE document (EO release)
2. ☐ Complete, ☐ N/A: Requirement - Box HRD (EO release) REV Doors - clear case
3. ☐ Complete, ☐ N/A: Requirement - Pin Assignments (ICD / Box pins) spread sheet – project file
4. ☐ Complete, ☐ N/A: Requirement derived justification, link in Doors – clear case
5. ☐ Complete, ☐ N/A: Requirement tracing and review check list, clear case
6. ☐ Complete, ☐ N/A: Design trade study – if needed, project memo
7. ☐ Complete, ☐ N/A: Estimate - Area, power if needed, project memo
8. ☐ Complete, ☐ N/A: PLD source code review checklist – Clear Case
9. ☐ Complete, ☐ N/A: PLD source code traceability – Clear Case
10. ☐ Complete, ☐ N/A: Functional test Benches, Captured in Clear Case
11. ☐ Complete, ☐ N/A: Functional PLD and post route simulation results, captured in project file
12. ☐ Complete, ☐ N/A: Requirement CCA card HRD – if needed (EO release) REV Doors – clear case
13. ☐ Complete, ☐ N/A: Requirement FRD2 REV, (EO release) – clear case
14. ☐ Complete, ☐ N/A: PLD Design – PLD source code, Captured in Clear case
15. ☐ Complete, ☐ N/A: Schematic Peer Review – project memo – results of review with SME
16. ☐ Complete, ☐ N/A: Schematic checklist, error report completed and resolved – team center
17. ☐ Complete, ☐ N/A: Analysis (initial / final after qual) – Derating / signal integrity/ timing analysis
project file / clear case
18. ☐ Complete, ☐ N/A: Detailed Installation Drawings (EO)
19. ☐ Complete, ☐ N/A: Detailed Interface Control Documents (EO)
20. ☐ Complete, ☐ N/A: Detailed Design Drawings (Team Center)
21. ☐ Complete, ☐ N/A: Detailed Part Lists (BOM's) (Team Center)
22. ☐ Complete, ☐ N/A: Schematic (E release until built – EO release prior to qual), data base in team center
23. ☐ Complete, ☐ N/A: Board layout guidelines for each CCA, (EDP) – team center

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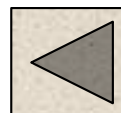
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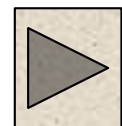
Phase 4 Exit Criteria

Phase 4 – Detailed Design, cont...

- 24. ☐ Complete, ☐ N/A: Board layout Peer Review, part placement and trace routing checklist – project file
- 25. ☐ Complete, ☐ N/A: CCA assembly drawing (E release until built – EO release prior to qual)
- 26. ☐ Complete, ☐ N/A: Box - Top Level Assembly Drawing, E release until built – EO release prior to qual, data base in team center
- 27. ☐ Complete, ☐ N/A: Box - Drawing (3 D exploded view – PDF format, models and drawings in team center
- 28. ☐ Complete, ☐ N/A: Box - Installation Drawing, E release until built – EO release after customer approval, data base in team center
- 29. ☐ Complete, ☐ N/A: Box - Drawing - torque definitions, data base in team center
- 30. ☐ Complete, ☐ N/A: Box - Detailed Size/volume, weight report, memo or power point
- 31. ☐ Complete, ☐ N/A: Box - Peer Review — results of review with SME, project memo, project file
- 32. ☐ Complete, ☐ N/A: Box - Packaging check list / standards, project file
- 33. ☐ Complete, ☐ N/A: BOM – (E release until built – EO release prior to qual)
- 34. ☐ Complete, ☐ N/A: Analysis (initial / final after qual) – Sensitivity and Derating, project memo
- 35. ☐ Complete, ☐ N/A: Test Procedure (E release)
- 36. ☐ Complete, ☐ N/A: CDR review package – as required
- 37. ☐ Complete, ☐ N/A: BOM - DTC compliance and Obsolescence report memo or spread sheet
- 38. ☐ Complete, ☐ N/A: Detailed 3-D Envelope Model (Team Center)
- 39. ☐ Complete, ☐ N/A: Detailed Performance Analysis – Thermal, Vib, Fatigue, Stack up Project Memo
- 40. ☐ Complete, ☐ N/A: DTC Analysis summary – Project Memo
- 41. ☐ Complete, ☐ N/A: Detailed Weights – Project Memo
- 42. ☐ Complete, ☐ N/A: 2D& 3D HV Analysis Report – (E Release)
- 43. ☐ Complete, ☐ N/A: CDR Design Checklists completed



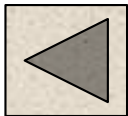
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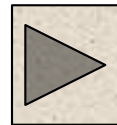
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Phase 5 – Item Build and Test Work Packages

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Item Build and Test – DDVT WP22

Inputs

Tasks / ETC

Deliverables

Design Data

CCA Gerber files
Box Req't & Design Doc – HRD & HDD
Board req't & Design Doc - CCA HRD & HDD
Released Schem's, BOM, CCA & box Assy's
PLD code

Plans

Program IMS & ETCs
CCA DTC target/actuals and DFMAT plans
Test concept / Risk mitigation plan

Hardware

Assembled CCAs
CCA/Box Devel Test equipment & Test SW
CCA/Box Development test plan
Lab equipment for test and troubleshooting

Build

Support CCA procurement and build activities
(40/5/10)

Documents

Develop CCA test procedure (80/20)
Generate design changes, support generation of
rework instructions, retest, & update the design
drawings (80/5/10/10)

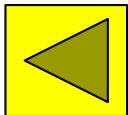
CCA test coverage analysis as appropriate (80)

Test and Integrate

Test CCA, document results and update test
procedure as required (120)
Perform robustness (environmental, voltage,
frequency, etc) tests as appropriate (80/40)
Risk testing prior to formal qual (40)
Support integration of CCA into Box (80)

1. Document Test results
project file - spread sheet or memo
2. Document Test coverage and test limits
project file
3. Risk Mitigation test report – if needed
project memo
4. Successful completion of SOI #2
audit summary in clear case
5. Board test procedure document
E Release
6. PLD design – PLD source code, E release
7. Functional test benches
updated and captured in Clear Case
8. Functional PLD simulation / post route
results captured in project file/clear case

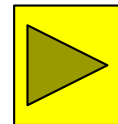
Return to
summary page



Resources :

- DDVT (600 hrs)
- Components (10 hrs)
- PWB design (10 hrs)
- EE Tech (80 hrs)

Return to
swimlane



Phase 5 Exit Criteria

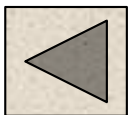
Phase 5 – Item Build & Test

1. ☐Complete, ☐N/A: Document Box ATP (E release with box test software)
2. ☐Complete, ☐N/A: Document Test results, project file - data spread sheet or memo
3. ☐Complete, ☐N/A: Document Test coverage and test limits, project file
4. ☐Complete, ☐N/A: Document SOF ATP (E release)
5. ☐Complete, ☐N/A: Box / System SOF EMC test procedure (E release)
6. ☐Complete, ☐N/A: HALT / HASS procedure – if required (E Release)
7. ☐Complete, ☐N/A: Successful completion of SOI #2, audit summary in clear case
8. ☐Complete, ☐N/A: PLD design – PLD source code tracing, E released
9. ☐Complete, ☐N/A: Functional test benches updated -captured in Clear Case

Phase 5 Exit Criteria

Phase 5 – Item Build & Test, cont...

- 10. ☐ Complete, ☐ N/A: Functional PLD and Post Route simulation results captured in project file and captured in Clear Case
- 11. ☐ Complete, ☐ N/A: PLD design – PLD source code review and tracing review, Clear Case/DOORS
- 12. ☐ Complete, ☐ N/A: Risk Mitigation test report – if needed, project memo
- 13. ☐ Complete, ☐ N/A: Board test procedure document (E Release)
- 14. ☐ Complete, ☐ N/A: Fit check – Project Memo
- 15. ☐ Complete, ☐ N/A: Thermal survey – Project Memo
- 16. ☐ Complete, ☐ N/A: Initial vibe – Project Memo
- 17. ☐ Complete, ☐ N/A: Board test procedure document E Release
- 18. ☐ Complete, ☐ N/A: Motor ATP if required (E Release)
- 19. ☐ Complete, ☐ N/A: DTC Actuals – Project Memo
- 20. ☐ Complete, ☐ N/A: Test Results – Project Memo
- 21. ☐ Complete, ☐ N/A: High Voltage / Altitude Test Reports (E Release)



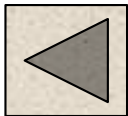
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swimlane**

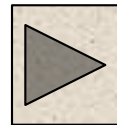


Phase 6 – System Integration and SOF Work Packages

**Return to
summary page**



**Return to
swimlane**



System Integration and SOF – Design Turn [DDVT] WP30

Inputs

Requirements

Design requirements updates causing
Design turns in CCAs

Design Documentation

Updated Hardware Allocation from
System Hardware
SOF CCA Build Hardware
Integrated Box from Build & Test

Tasks / ETC

Test

Support SOF testing as required

Reviews

Support System review and validation of changes (60)
Support peer review of test results
Hold CCA PRR (60)

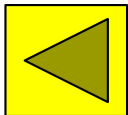
Documents

Create, update and resolve Problem reports (120)
Update design documentation:
 schematics, BOM, timing analysis, simulation, derating,
 updated requirements (120)
Update CCA Test Procedure, as necessary (40)
Update FRD, as required (40)
Update HRD, as required (40)
Generate PLD Programming Files (FCI) (40)

Deliverables

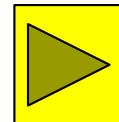
- 1.Problem reports under configuration ctrl
clear quest
- 2.Updated CCA schematic – as required
– EO release for qual
- 3.Update CCA BOM – as required
– EO release for qual
- 4.Update CCA Assembly Drawing – as required
– EO release for qual
- 5.Updated HRD & FRD EO release new REV
- 6.DFx (M,A,T) at Box level report
review project memo with MFG WP
- 7.PLD Design –PLD Source code
EO released / clear case
8. PLD FCI – EO Release

Return to
summary page



Resources (hrs)
- DDVT (480)

Return to
swimlane



Phase 6 Exit Criteria

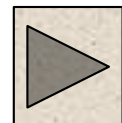
Phase 6 – System Integration & SOF

1. ☐ Complete, ☐ N/A: Problem reports under configuration control, clear quest
2. ☐ Complete, ☐ N/A: Updated ATP – as required, EO release - REV
3. ☐ Complete, ☐ N/A: SOF EMC test procedure, EO release
4. ☐ Complete, ☐ N/A: SOF EMC Test report SDRL
5. ☐ Complete, ☐ N/A: SOF Environmental qual test procedure, EO release
6. ☐ Complete, ☐ N/A: SOF Environmental qual test report, SDRL
7. ☐ Complete, ☐ N/A: DFx (M,A,T) at Box level report, project memo
8. ☐ Complete, ☐ N/A: Updated HRD & FRD, EO release new REV
9. ☐ Complete, ☐ N/A: Updated CCA schematic – as required – EO release for qual
10. ☐ Complete, ☐ N/A: DFx (M,A,T) at Box level report review project memo with MFG WP
11. ☐ Complete, ☐ N/A: FW V&V TRR Checklist
12. ☐ Complete, ☐ N/A: DFx (M,A,T) at Box level report review project memo with MFG WP
13. ☐ Complete, ☐ N/A: Updated Motor Req'ts Doc



**Return to
summary page**

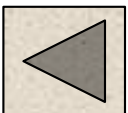
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Phase 6 Exit Criteria

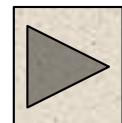
Phase 6 – System Integration & SOF, cont...

- 14. ☐ Complete, ☐ N/A: Update CCA BOM – as required – EO release for qual
- 15. ☐ Complete, ☐ N/A: Update CCA Assembly Drawing – as required – EO release for qual
- 16. ☐ Complete, ☐ N/A: PLD Design –PLD Source code, EO released / clear case
- 17. ☐ Complete, ☐ N/A: PLD FCI – EO Release
- 18. ☐ Complete, ☐ N/A: SOF Environmental qual test report, Support SDRL
- 19. ☐ Complete, ☐ N/A: Code review and tracing checklist, Clear case
- 20. ☐ Complete, ☐ N/A: Functional PLD and post route simulation results, captured in project file
- 21. ☐ Complete, ☐ N/A: PLD Elemental Analysis Report
- 22. ☐ Complete, ☐ N/A: Updated FRD,TB & Test Cases developed, update through cert phase - clear case
- 23. ☐ Complete, ☐ N/A: Updated Motor ATP (EO)
- 24. ☐ Complete, ☐ N/A: Updated Motor documentation (EO)
- 25. ☐ Complete, ☐ N/A: Production Readiness Review complete
- 26. ☐ Complete, ☐ N/A: Update 2D & 3D HV Clearance Reports – (E Release)
- 27. ☐ Complete, ☐ N/A: Update High Voltage / Altitude Test Reports (E Release)
- 28. ☐ Complete, ☐ N/A: Design checklists completed



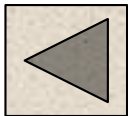
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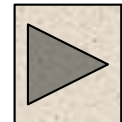


Phase 8 – Certification Work Packages

**Return to
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Certification Phase – Design Turn [DDVT] WP42

Inputs

Problem Reports

V+V actions / issues
Blue / Red label problem list

Qualification Data

Environmental test issues
EMI test issues

DFX Inputs

Manufacturability DFX inputs
DTC updates

Requirements

CCA design requirements updates

Tasks / ETC

Requirements

Update requirements / block diagrams – as required (40)
Update compliance matrix / HVR (40)

Design Changes

Evaluate design and manufacturability DFX inputs (40)
Evaluate Qual changes and incorporate (40)
Update Schematic / BOM (40)
Update Analysis (performance / Timing / Simulation) (40)
Update part placement and trace routing instructions (40)
Update design documentation / description (40)
Update CCA Test Procedure, as necessary (40)

PWB Updates

Review part placement changes (40)
Review trace routing changes (40)

Problem Reports

Close out all PRR actions (40)

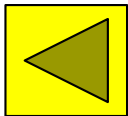
Production

Support production Hardware Build / readiness review (40)

Deliverables

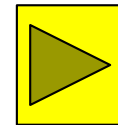
1. Problem reports closed or deferred - clear quest
2. HW accomplishments summary (EO)
3. Successful SOI #4 review audit report in clear case
4. Updated CCA Drawing Package, EO release
 - a) Schematic
 - b) BOM
 - c) Assembly Drawing
5. Updated CCA Test Procedure
6. Updated Analysis, Project Memo

Return to
summary page



Resources (hrs)
- ADVT (520)

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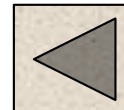


Phase 8 Exit Criteria

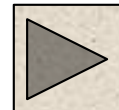
Phase 8 – Certification

1. ☐ Complete, ☐ N/A: Problem reports closed or deferred – clear quest
2. ☐ Complete, ☐ N/A: Successful transition of design to production evidence that PRR Checklist is complete and actions are closed (Project Memo)
3. ☐ Complete, ☐ N/A: HW accomplishments summary (EO)
4. ☐ Complete, ☐ N/A: Successful SOI #4 review audit report in clear case
5. ☐ Complete, ☐ N/A: Updated CCA Drawing Package, EO release
 - a. ☐ Complete, ☐ N/A: Schematic
 - b. ☐ Complete, ☐ N/A: BOM
 - c. ☐ Complete, ☐ N/A: Assembly Drawing
6. ☐ Complete, ☐ N/A: Updated CCA Test Procedure
7. ☐ Complete, ☐ N/A: Updated Analysis, Project Memo
8. ☐ Complete, ☐ N/A: Updated Drawings & Models, EO release
 - a. ☐ Complete, ☐ N/A: BOM
 - b. ☐ Complete, ☐ N/A: Assembly Drawing
 - c. ☐ Complete, ☐ N/A: Chassis
 - d. ☒ Complete, ☐ N/A: Mechanical Subassemblies
9. ☐ Complete, ☐ N/A: Updated Analysis, Project Memo
10. ☐ Complete, ☐ N/A: Resolved Problem reports
11. ☐ Complete, ☐ N/A: Updated ATP Motor/Actuator, as needed (Actuator support only)
12. ☐ Complete, ☐ N/A: Motor PRR Complete
13. ☐ Complete, ☐ N/A: Updated Motor Req'ts Doc
14. ☐ Complete, ☐ N/A: Updated Motor documentation (EO)
15. ☐ Complete, ☐ N/A: Update 2D & 3D HV Clearance Reports - (E Release)
16. ☐ Complete, ☐ N/A: Update High Voltage / Altitude Test Reports (E Release)
17. ☐ Complete, ☐ N/A: Design review checklists

**Return to
summary page**

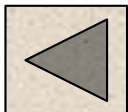


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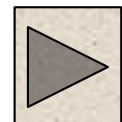


Product Maturation/EIS and Sustainment Work Packages

**Return to
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**Return to
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Design Engineering – Product Maturation/EIS (FPY > 92%) WP49

Inputs

Manufacturing Data

FPY (supply chain, CCA, Box)
Product cost data
NC history
RURs
Parametric ATP Data
Supplier quality rating
Supply chain sourcing strategies

Program/Design Data

Customer demands (design change, new features, etc)
Obsolescence Status, Errata
Fielded MTBUR, DMC

Tasks / ETC

Lead Tasks

Conduct EIS Review (entry event when FPY > 92%)
Program Reviews (Moog with Moog customers)
Lead RCCAs as required.
Develop solutions to design problems
Actively work to reduce NCs and improve FPY
Review ATP Limits with respect to FPY, NCs and parametric data and make changes as appropriate
Lead Cost/Product/Process improvement initiatives as required
Lead Delta Qualification/Certification, QBS, etc activities as required
Create and Maintain problem reports

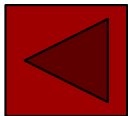
Support Tasks

CRB Support
Drawing, BOM, ATP, HASS, etc updates as required
Review supplier performance data as required
Support Reliability Testing activities (i.e. ongoing Proof of HASS, etc)
Support Supply Chain transitions as required
Review Parametric test data for shifts and out of family trends

Deliverables

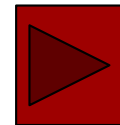
1. Refresh Strategy
2. Support Weekly Manufacturing-Design meetings
3. Updated drawings, BOMs, ATP, HASS, ATP Limits, etc as required
4. Delta Qual documents as required

Return to
summary page



Resources (hrs)
- Project/IDVT (100% LOE)

Return to
swimlane



Design Engineering – Sustainment (FPY > 99%) WP51

Inputs

Manufacturing Data

FPY (supply chain, CCA, Box)
Product cost data
NC history
RURs
Parametric ATP Data
Supplier quality rating
Supply chain sourcing strategies

Program/Design Data

Customer demands (design change, new features, etc)
Obsolescence Status, Errata
Fielded MTBUR, DMC

Tasks / ETC

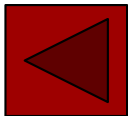
Support Tasks

CRB Support
Program Reviews (Moog with Moog customers)
Support RCCAs as required
Develop Refresh Strategy working with Program team, customer and manufacturing engineering
Cost/Product/Process improvement initiatives as required
Drawing, BOM, ATP, HASS, etc updates as required
Delta Qualification/Certification, QBS, etc activities as required
Support Reliability Testing activities (i.e. ongoing Proof of HASS, etc)
Support Supply Chain transitions as required
Review Parametric test data for shifts and out of family trends
Review ATP Limits with respect to FPY, NCs and parametric data and make changes as appropriate
Create and Maintain problem reports

Deliverables

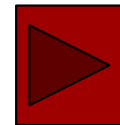
1. Refresh Strategy
2. Support Weekly Manufacturing-Design meetings
3. Updated drawings, BOMs, ATP, HASS, ATP Limits, etc as required
4. Delta Qual documents as required

Return to
summary page



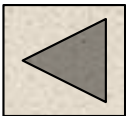
Resources (hrs)
- Project/IDVT (25% LOE)

Return to
swimlane



Phase 1 – MFG Work Packages

**Return to
summary page**



**Return to
swimlane**



Requirements Definition - Mfg Project Plan WP4

Inputs

Requirements

Spec/SOW
Box HRD
Proposal Baseline
DTC Targets

Schedule

Updated quantities and milestones

Plans

Quality flow down
Proposal EMCP0
Cert/Project Plan
Preliminary product structure

Tasks / ETC

Project Preparation

Review Proposal Baseline including budgets (8)
Review product relative to platforms for synergy (4)
Review plan for magnetic sourcing (4)
Review plan for cable assemblies sourcing (4)
Review plan for mechanicals including box (8)

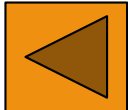
Design Requirements & Standards

Capabilities gap analysis
(capacity, equipment, processes, materials, etc) (8)
Review DTC targets versus plan/actuals (8)
Defined prototype and production build locations
Update EMCP1 (32)

Deliverables

1. DTC feedback to project team
2. EMCP1(MFG plan)

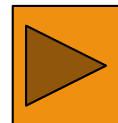
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Resources (hrs)

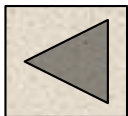
-Operations Lead (28)
-Prod/Proc Engineering (32)
-Supply Chain (16)
-76 hours total

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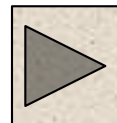


Phase 3 – MFG Work Packages

**Return to
summary page**



**Return to
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Preliminary Design – Prelim. Mfg process definition WP12

Inputs

Tasks / ETC

Deliverables

Requirements

Preliminary CCA Design Info
Updated quantities and milestones

Updated Box HRD

Plans

EMCP1
Revised project plan/scope changes

DFX

Revised DTC Targets

Requirement Reviews

Review preliminary block diagrams /allocations (24)

Review preliminary BOM and schematics(32)

Review preliminary Box design (24)

Plans

Updated EMCP2 (32)

Review risk management plan (16)

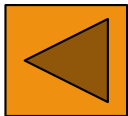
Review DTC targets versus plan/actuals (16)

DFX

Conduct DfX (M,A,T) reviews (40)

1. DfX (M,A,T) at Box level summary
2. DfX (M,A,T) at CCA level summary
3. Process flow diagram
4. DTC feedback to project team
5. EMCP2

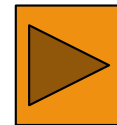
Return to
summary page



Resources (hrs)

-Operations Lead (36)
-Prod/Proc Engineering (128)
-Supply Chain (20)
-184 hours total

Return to
swimlane



Preliminary Design – Prototype/Risk Mitigation Build

Inputs

Tasks / ETC

Deliverables

Requirements

Preliminary CCA Design Info
CCA Risk Build data as required
Updated quantities and milestones
PDR materials

Plans

EMCP2
Revised project plan/scope changes

DFX

Revised DTC targets

Requirement Reviews

Review preliminary design box and CCA (80)

Plans

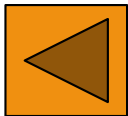
Updated and released EMCP3 (24)
Refine AWWs, TWs if required to support product and process engineering per EMCP (180)

DFX

Review DTC targets versus plan/actuals (16)
Conduct DFX (M,A,T) reviews (80)

1. DFX (M,A,T) at Box level summary
2. DFX (M,A,T) at CCA level summary
3. AWWs and TWs if required
4. Prototype/risk mitigation CCAs, as required
5. Product/Process/Ops PDR materials
6. DTC feedback to project team
7. EMCP3

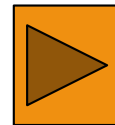
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Resources (hrs)

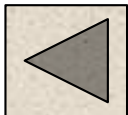
-Operations Lead (24)
-Prod/Proc Engineering (340)
-Supply Chain (16)
-380 hours total

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swimlane

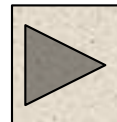


Phase 4 – MFG Work Packages

**Return to
summary page**



**Return to
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Detailed Design - Mfg Process definition WP20

Inputs

Project

Revised project plan
/ scope changes

Plans

EMCP3
Latest AW, TW

Requirements

CCA TRDs
Detailed Design Package
Revised DTC Targets
Special test Reqs (HASS, etc)

Tasks / ETC

Design Support / Reviews

Review detailed drawings box and CCA (120)
Review DTC targets versus plan/actuals (32)
Review TRD (Test Requirement Docs) (32)

Drawings

Update EMCP4 (24)
Refine AW with CEM Process Engineering (160)
Refine TW with CEM Product Engineering (160)

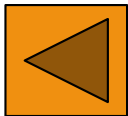
Production

Visit CCA CEM and audit per strategy (300)

Deliverables

- 1.MFG - DFMAT – Peer review with MFG project memo / action resolution
- 2.MFG - EMCP4 (MFG plan update)
- 3.CDR review package – as required

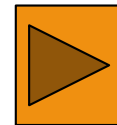
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Resources (hrs)

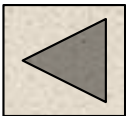
-Operations Lead (40)
-Prod/Proc Engineering (748)
-Supply Chain (40)
-828 hours total

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swimlane

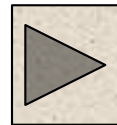


Phase 5 – MFG Work Packages

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Item Build & Test – Dev HW Build CCA/Item WP28

Inputs

Design Data/Requirements

CCA Dev Test Procedure
Released PLD code
Box ATP test requirements
Box ATP limits justification
Box ATP

Plans

EMCP4
Revised project plan/scope changes
Latest AW, TW
Revised DTC Targets

Hardware/other

POB hardware, tooling
CCA Dev Test Fixtures

Tasks / ETC

Build

Liaison with CEM (120)
Update box and CCA AWs & TWs if required (200)
Conduct POB and report (280)

Documents

Update EMCP5 (8)

Test

Support box and CCA Test Procedures as required (200)
Support Des Engineering testing (24)

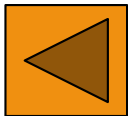
Reviews / Reports

Validate DTC actuals (40)
Review DTC targets versus plan/actuals (24)
Support MRB (120)

Deliverables

1. DFx (M,A,T) at Box level summary
2. DFx (M,A,T) at CCA level summary
3. Hardware CCA (turn0), QTY based on project need
4. Hardware box (turn0), Qty based on project need
5. Updated AW, TW if required
6. Proof of build report – Project memo
7. DTC feedback to project team - Project memo
8. EMCP5

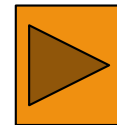
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Resources (hrs)

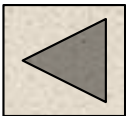
-Operations Lead (80)
-Prod/Proc Engineering (856)
-Supply Chain (80)
-1016 hours total

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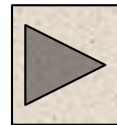


Phase 6 – MFG Work Packages

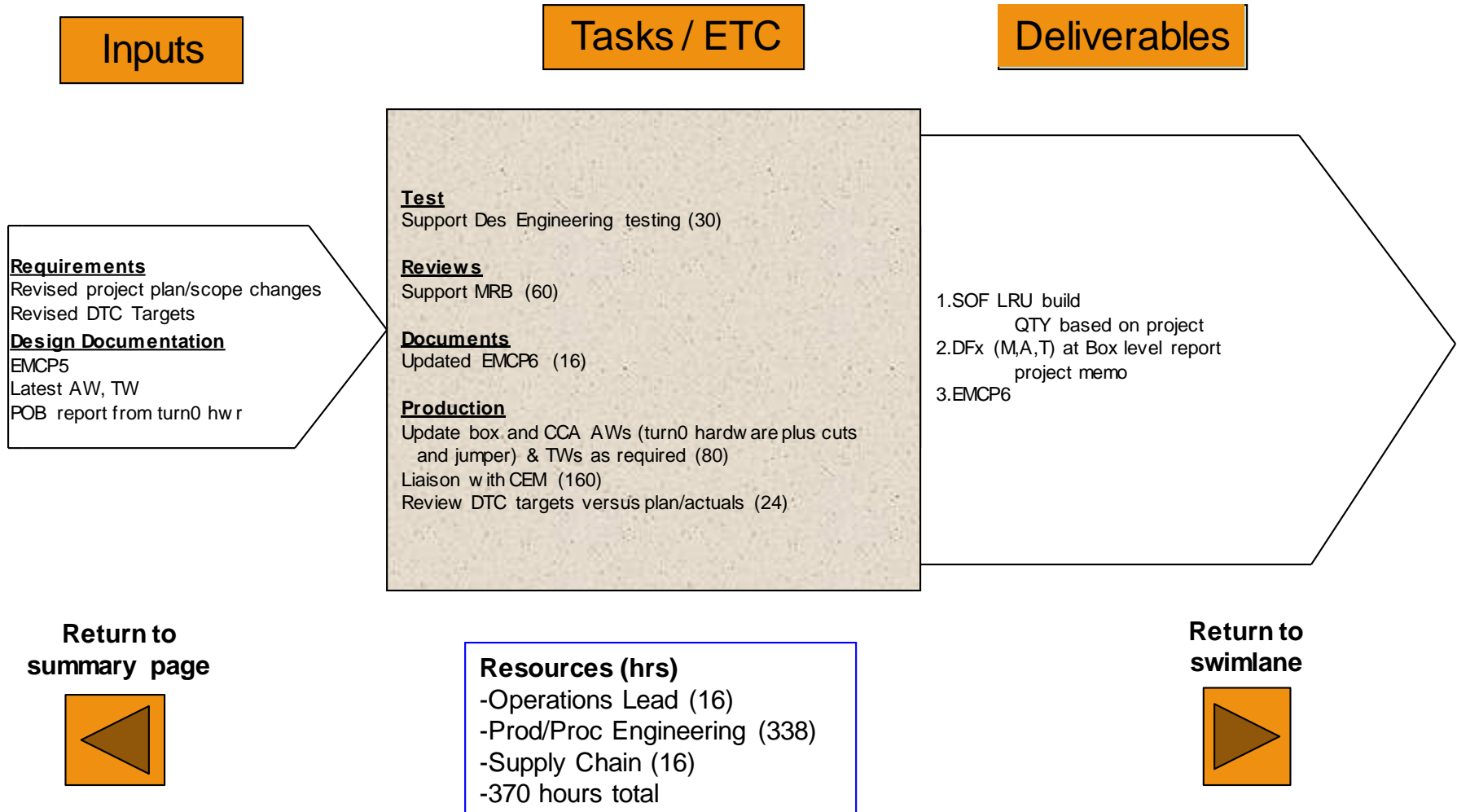
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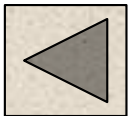


System Integration and SOF – SOF Build CCA/Item WP36

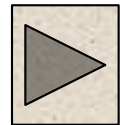


Phase 7 – MFG Work Packages

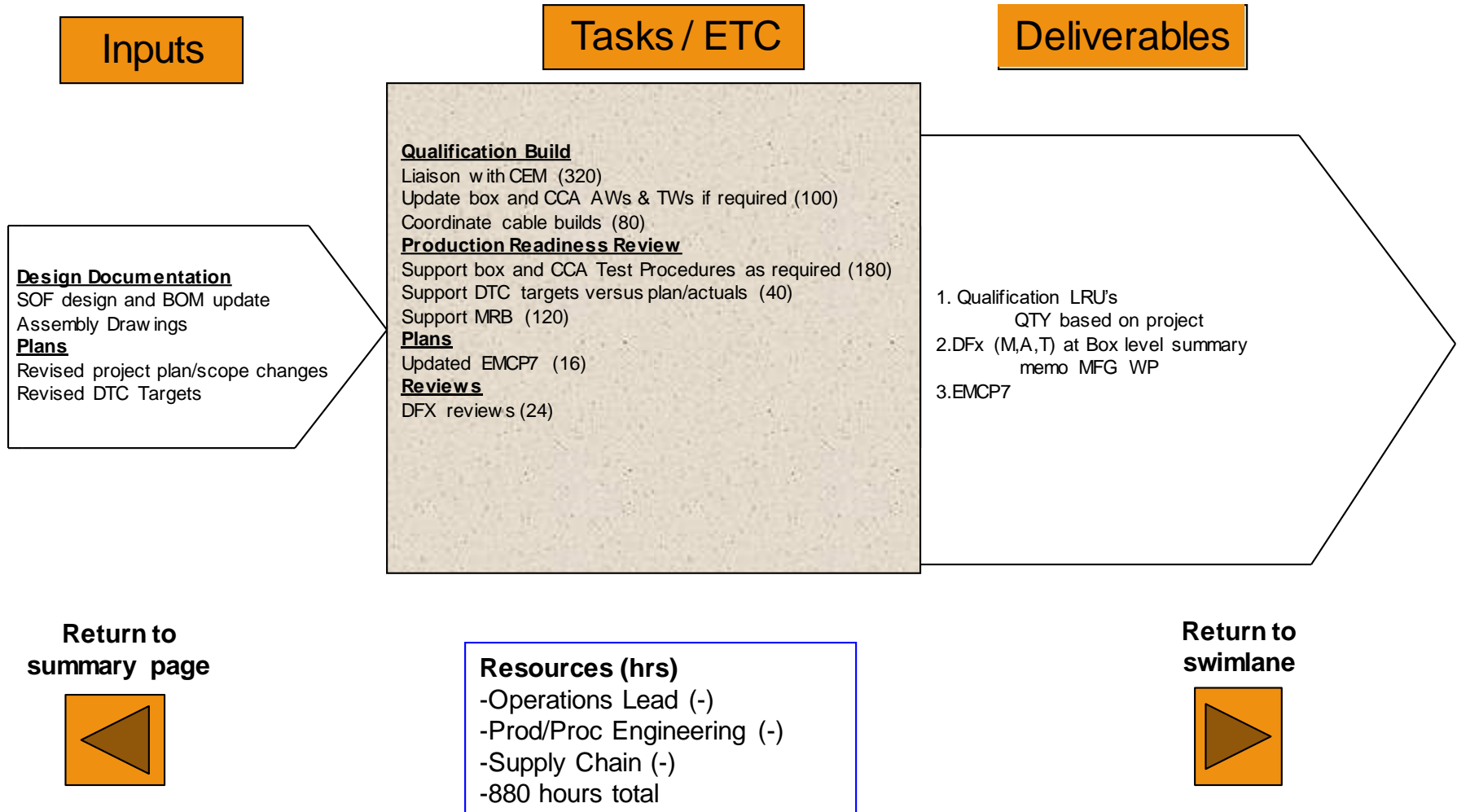
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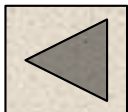


Qualification Phase – Production Readiness Qual Builds WP40

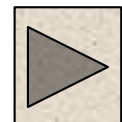


Phase 8 – MFG Work Packages

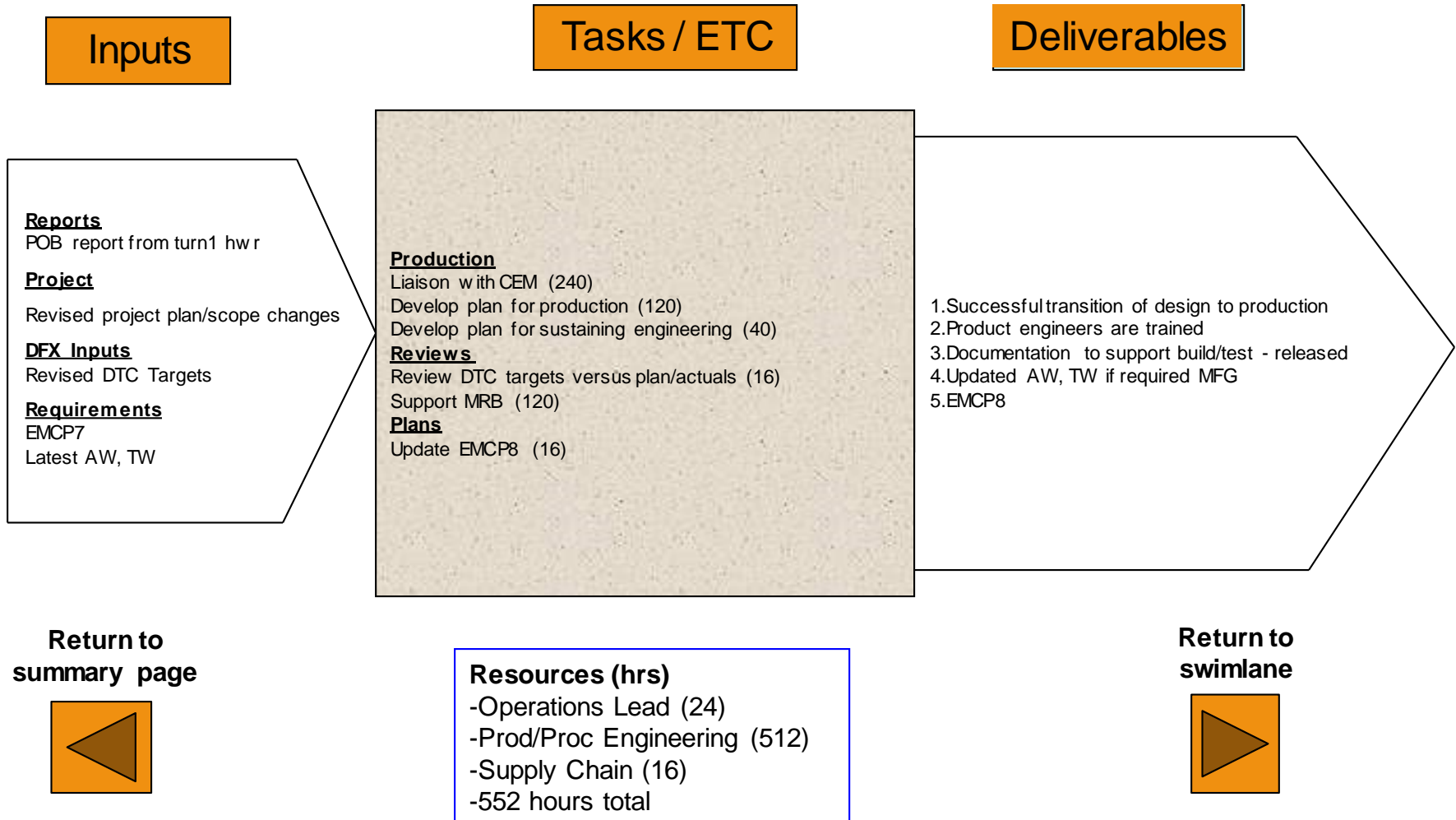
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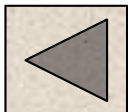


Certification Phase – Production Hardware Build WP48

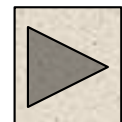


Product Maturation/EIS and Sustainment Work Packages

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Manufacturing Engineering – Product Maturation/EIS (FPY > 92%) WP50

Inputs

Tasks / ETC

Deliverables

Manufacturing Data

FPY (supply chain, CCA, Box)

Product cost data

NC history

RURs

Parametric ATP Data

Supplier quality rating

Supply chain sourcing strategies

Program/Design Data

Customer demands (design change, new features, etc)

Obsolescence Status, Errata

Fielded MTBUR, DMC

Support Tasks

Develop Plan for Every Part (P4EP)

CRB support

Supplier performance review meetings

Support RCCAs as required

Create and Maintain problem reports

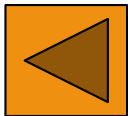
Process Data

Process parametric data from CCA and Box ATP

Lead test equipment maintenance and upgrade activities

1. Generate Incident Database
2. Generate parametric data summary
3. Lead weekly Manufacturing-Design meeting 'Product Yield Top Concerns'
4. Conduct Monthly Manufacturing Review meeting with LRU team (FPY, NC, on Hold, cost, etc)
5. Update TW, AW as required

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Resources (hrs)

- Product/Proc Eng (50%/25% LOE)
- Supply Chain (25% LOE)
- QE (5% LOE)

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Manufacturing Engineering – Sustainment (FPY > 99% WP52)

Inputs

Tasks / ETC

Deliverables

Manufacturing Data

FPY (supply chain, CCA, Box)

Product cost data

NC history

RURs

Parametric ATP Data

Supplier quality rating

Supply chain sourcing strategies

Program/Design Data

Customer demands (design change, new features, etc)

Obsolescence Status, Errata

Fielded MTBUR, DMC

Lead Tasks

Conduct Product Maturation Entry Review (entry event when FPY > 99%)

Lead RCCAs as required

Create and Maintain problem reports

Support Tasks

CRB support

Supplier performance review meetings

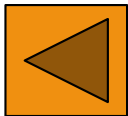
Process Data

Process parametric data from CCA and Box ATP

Lead test equipment maintenance and upgrade activities

1. Maintain Incident Database
2. Maintain parametric data summary
3. Lead weekly Manufacturing-Design meeting 'Product Yield Top Concerns'
4. Conduct Monthly Manufacturing Review meeting with LRU team (FPY, NC, on Hold, cost, etc)
5. Update TW, AW as required

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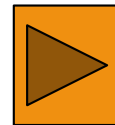
Resources (hrs)

-Product/Proc Eng (25%/10% LOE)

-Supply Chain (10% LOE)

-QE (5% LOE)

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Acronyms

A

ADVT	Analog Design Verification and Test
ATP	Acceptance Test Procedure
ALT	Altitude
AW	Assembly Worksheet
ABOM	Advanced Bill of Material
A&T	Assembly & Test

B

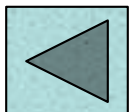
BOM	Bill Of Materials
BLDC	Brushless Direct Current

C

CCA	Circuit Card Assembly
CDR	Critical Design Review
CR	Change Request
CM	Configuration Management
CERT	Certification
CEM	Contract Electronics Manufacturer

D

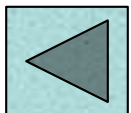
DDVT	Digital Design Verification and Test
DFx (M,A,T)	Design for x where x can be Manufacturing, Cost, Assembly and Test, etc
DTC	Design To Cost
DFMAT	Design for Manufacturability, Assembly and Test
DUT	Device Under Test
DEV	Development
DMC	Direct Maintenance Cost



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Acronyms (continued)

E	
EE	Electrical Engineering
EMPT	Electronics Manufacturing Process and Test
EDP	Electronics Design Plan (Special Instructions used for PWB Layout definition)
EO	Engineering Order: form and procedure for implementing design changes
EMC	Electromagnetic Compliance (Compatibility)
EMI	Electromagnetic Interference
EM	Electro-Mechanical
ETC	Estimate To Complete
EVMS	Earned Value Management System
EMCP	Electronics Manufacture Control Plan
F	
FCI	Firmware Configuration Index
FRD	Firmware Requirements Document
FW V&V	Firmware Verification and Validation
FEs	Functional Elements
FMEA	Failure Mode Effects Analysis
FDD	Firmware Design Drawing
FW	Firmware



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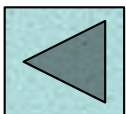
Acronyms (continued)

H

HALT	Highly Accelerated Life Test
HAS	Hardware Accomplishment Summary
HASS	Highly Accelerated Stress Screens
HCMP	Hardware Configuration Management Plan
HDP	Hardware Development Plan
HDD	Hardware Description Document
HEPG	Hardware Engineering Process Group
HVP	Hardware Verification Plan
HRD	Hardware Requirements Document
HW	Hardware
HV	High Voltage
HVR	Hardware Verification Report
HVCP	Hardware Verification Cases and Procedures
HVS	Hardware Verification Standards
HVTCP	Hardware Verification Test Cases and Procedures
HVTP	Hardware Verification Test Procedures
HCMP	Hardware Configuration Management Plan
HPAP	Hardware Process Assurance Plan
HRS	Hardware Requirements Specification

I

ICD	Interface Control Diagram
IDVT	Item Design Verification Test
IP	Intellectual Property
IPT	Integrated Product Teams
IR&D	Internal Research and Development
IO	Input /Output
IMS	Integrated Master Schedule



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Acronyms (continued)

K

Kt/Ke	Torque constant (Kt)/Voltage constant (Ke)
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L

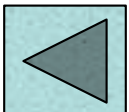
LRU	Line Replaceable Unit
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M

MDVT	Motor Design Verification and Test
MECH	Mechanical
MOC	Means of Compliance
MBS	Moog Business System
MRB	Material Review Board
MFG	Manufacturing
ME	Mechanical Engineering
MTBUR	Mean Time Between Unscheduled Removal

P

PHAC	Plan for Hardware Aspects of Certification
PLD	Programmable Logic Device
PRB	Program Review Board
PACT	Packaging Design Verification and Test
PDVT	Power Design Verification and Test
PDR	Preliminary Design Review
PRR	Production Readiness Review
PN	Part Number
PWB	Printed Wire Board
PPL	Preferred Parts List
PR	Problem Report
POB	Proof of Build
PROD	Production
PROC	Procedure



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Acronyms (continued)

Q

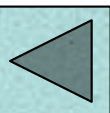
QA	Quality Assurance
QUAL	Qualification
QTP	Qualification Test Procedure
QTY	Quality

R

RQMT	Requirement
REV	Revision
Rtt/Ltt	Terminal to Terminal Resistance and Inductance

S

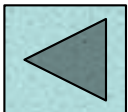
SOF	Safety Of Flight
SOI	State of Involvement
SDRL	Subcontractor Data Requirement List
SRR	System Requirements Review
SW	Software
STE	Standard Test Equipment
SYS	System
SME	Subject Matter Expert
SOW	Statement Of Work
SSMP	System Safety Management Plan
SPEC	Specification



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Acronyms (continued)

T	
TRD	Test Requirements Document
TRR	Test Readiness Review
TB	Test Bench
TEMP	Temperature
TWs	Test Worksheet
TE	Test Equipment
V	
V&V	Verification and Validation
VHDL	Very High-level Design Language
VIB	Vibration
W	
WP	Work Package
WO	Work Order
WBS	Work Breakdown Structure



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