Relatório Multiplicadores

INE5406-05235A

Equipe:

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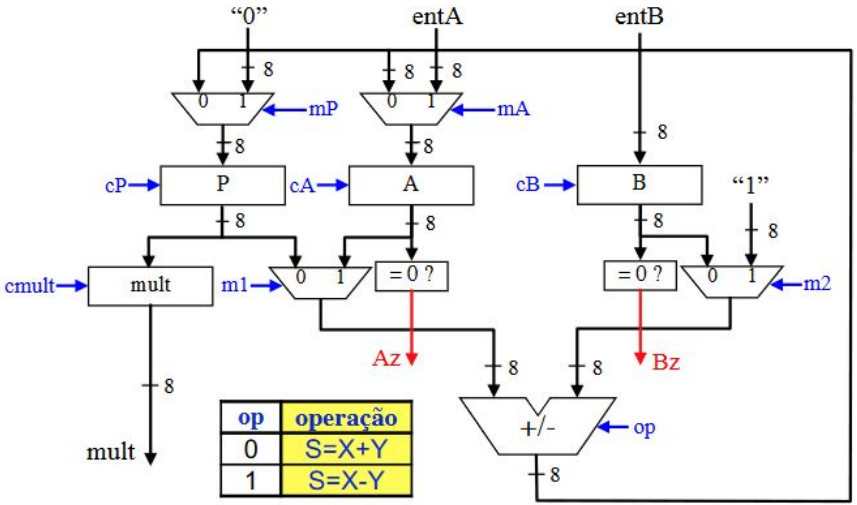
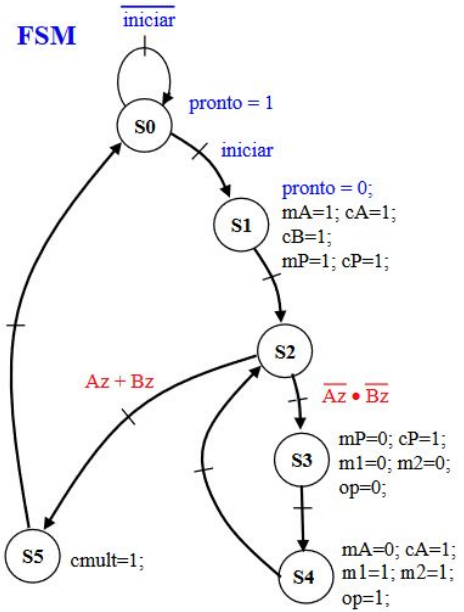
- Julio Gonçalves Ramos - 19203165

Multiplicador do Exemplo 4 do slide “Aula 5-T”

- Bloco Operativo



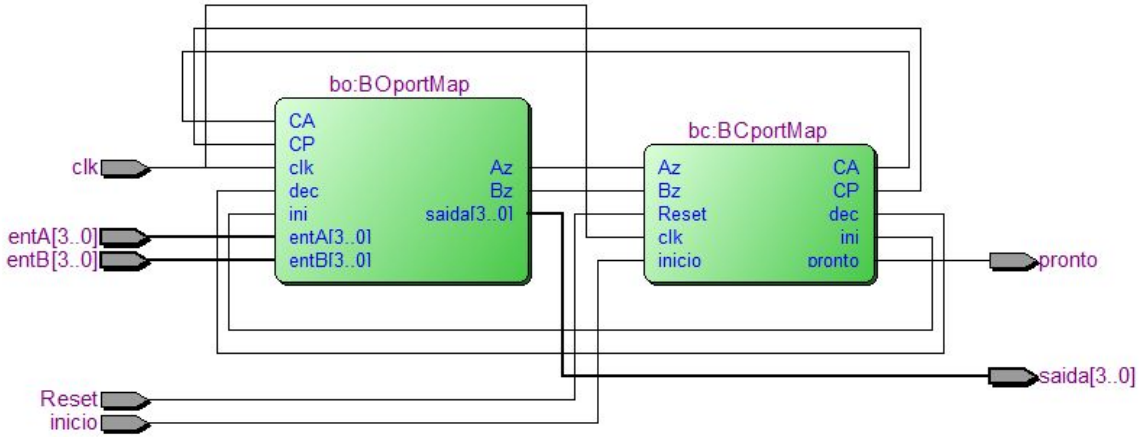
- FSM



(Retirados dos slides “Aula 5-T”)

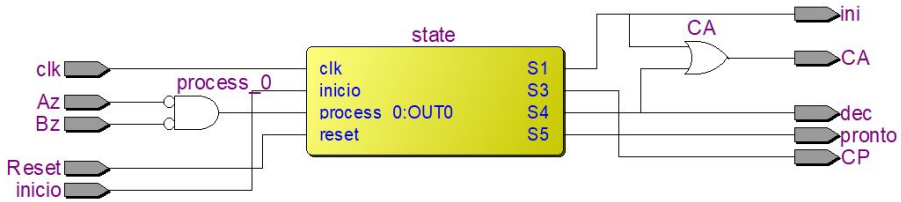
Multiplicador do Exemplo 4 do slide “Aula 5-T”

- Netlist
  - Versão Completa

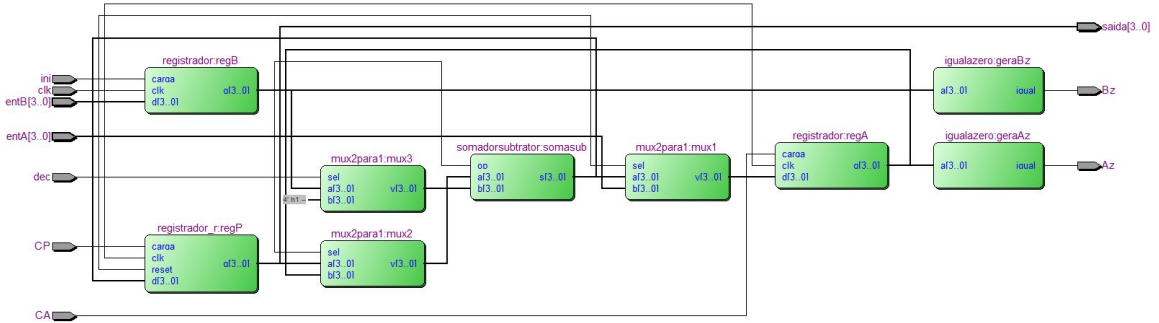


Multiplicador do Exemplo 4 do slide “Aula 5-T”

- Bloco de Controle

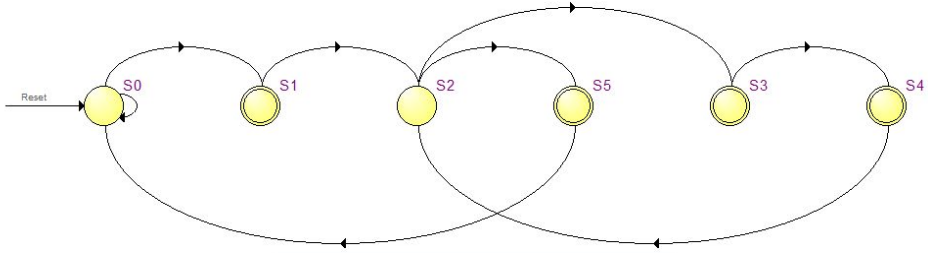


- Bloco Operativo



Multiplicador do Exemplo 4 do slide “Aula 5-T”

- Máquina de Estados do Bloco de Controle



State Table

	Source State	Destination State	Condition
1	S0	S0	(!inicio)
2	S0	S1	(inicio)
3	S1	S2	
4	S2	S5	(!process_0)
5	S2	S3	(process_0)
6	S3	S4	
7	S4	S2	
8	S5	S0	

Transitions | Encoding

Multiplicador do Exemplo 4 do slide “Aula 5-T”

- Simulação de ondas - ModelSim

Entrada A = 0011 (03) | Entrada B = 0100 (04) | Saida = 1100 (12)

Multiplicador do Exemplo 4 do slide “Aula 5-T”

- Análise Comparativa - 4 Bits vs 8 Bits
  - Área

Total logic elements	30 / 4,608 (< 1 %)
Total combinational functions	24 / 4,608 (< 1 %)
Dedicated logic registers	18 / 4,608 (< 1 %)
Total registers	18
Total pins	16 / 158 (10 %)

4 Bits

Total logic elements	48 / 4,608 (1 %)
Total combinational functions	43 / 4,608 (< 1 %)
Dedicated logic registers	30 / 4,608 (< 1 %)
Total registers	30
Total pins	28 / 158 (18 %)

8 Bits

Multiplicador do Exemplo 4 do slide “Aula 5-T”

- Atraso

Minimum Clock to Output Times

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	saida[*]	clk	6.062	6.062	Rise	clk
1	saida[3]	clk	6.364	6.364	Rise	clk
2	saida[2]	clk	6.289	6.289	Rise	clk
3	saida[1]	clk	6.190	6.190	Rise	clk
4	saida[0]	clk	6.062	6.062	Rise	clk
2	pronto	clk	6.054	6.054	Rise	clk

4 Bits

Minimum Clock to Output Times

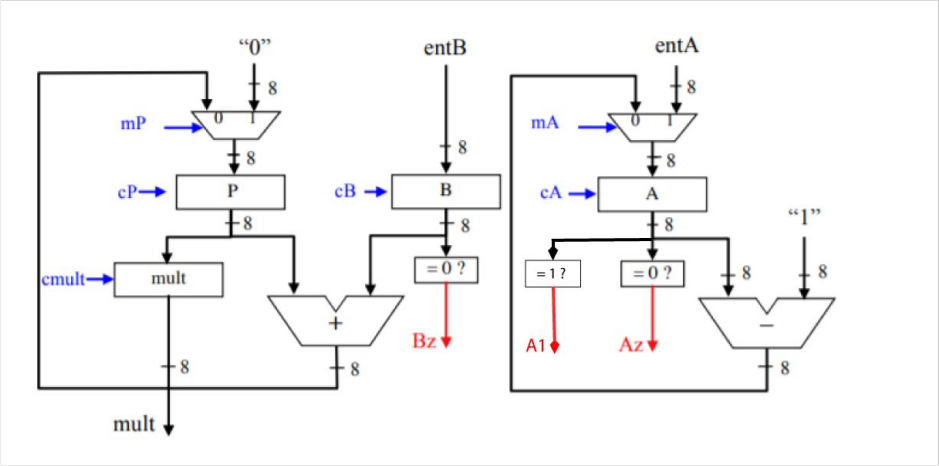
	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	saida[*]	clk	6.186	6.186	Rise	clk
1	saida[6]	clk	6.515	6.515	Rise	clk
2	saida[3]	clk	6.385	6.385	Rise	clk
3	saida[0]	clk	6.377	6.377	Rise	clk
4	saida[5]	clk	6.306	6.306	Rise	clk
5	saida[1]	clk	6.253	6.253	Rise	clk
6	saida[4]	clk	6.235	6.235	Rise	clk
7	saida[7]	clk	6.202	6.202	Rise	clk
8	saida[2]	clk	6.186	6.186	Rise	clk
2	pronto	clk	6.163	6.163	Rise	clk

8 Bits

Multiplicador do Exemplo 5* do slide “Aula 5-T”

* modelo adaptado para Mealy

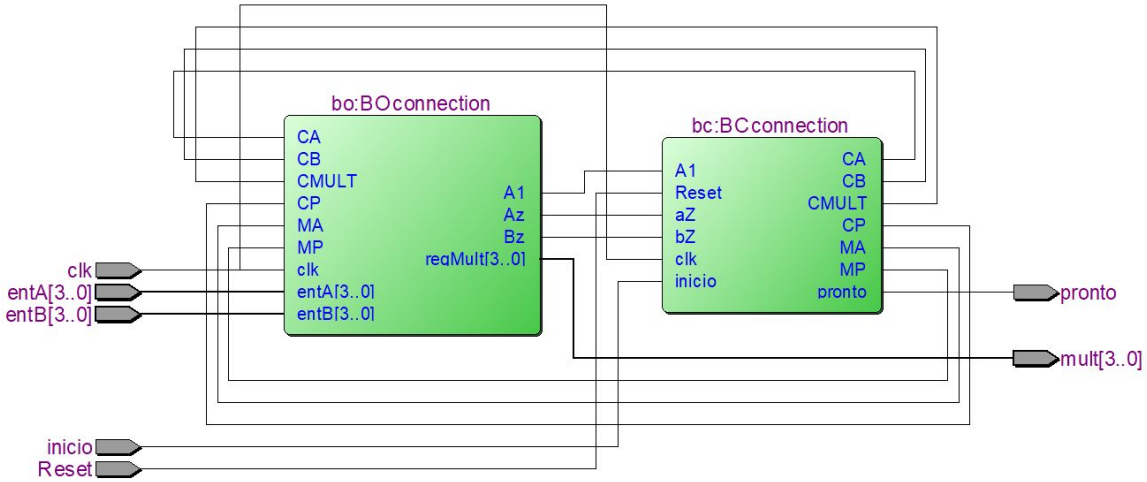
- Bloco Operativo



Multiplicador do Exemplo 5* do slide “Aula 5-T”

* modelo adaptado para Mealy

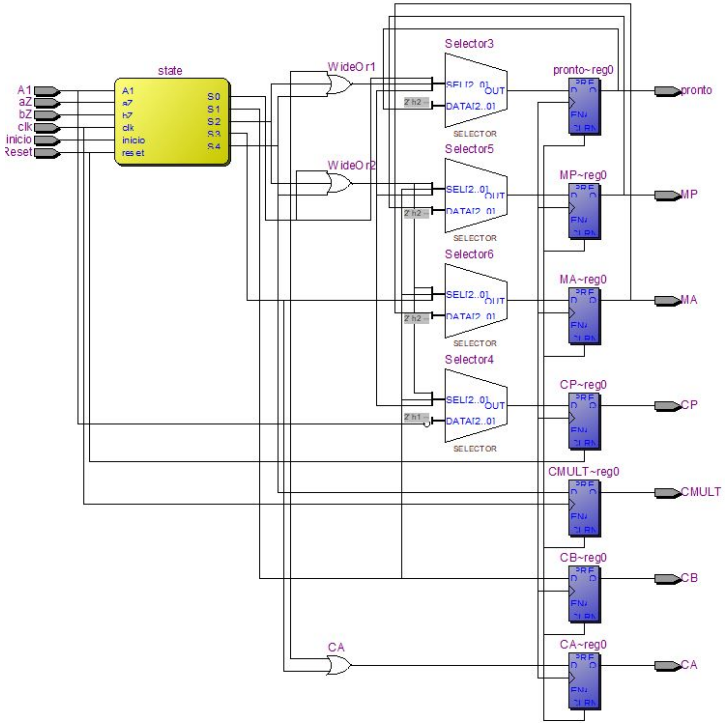
- Netlist
  - Versão Completa



Multiplicador do Exemplo 5* do slide “Aula 5-T”

* modelo adaptado para Mealy

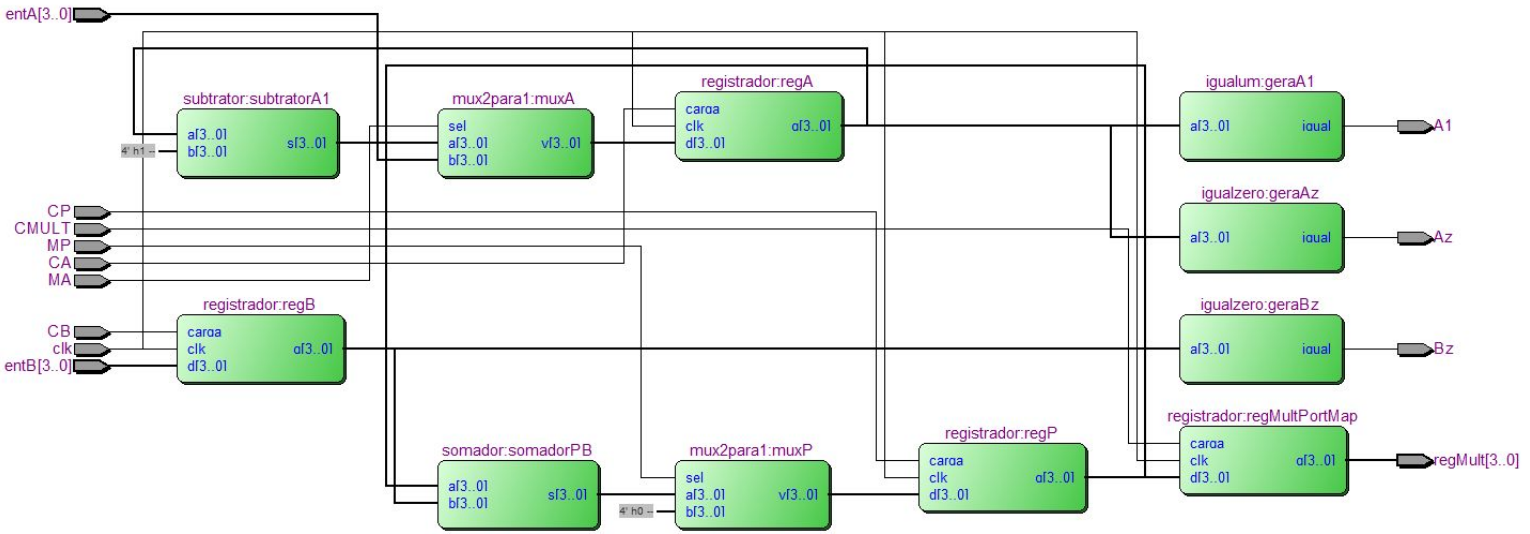
- Bloco de Controle



Multiplicador do Exemplo 5* do slide “Aula 5-T”

* modelo adaptado para Mealy

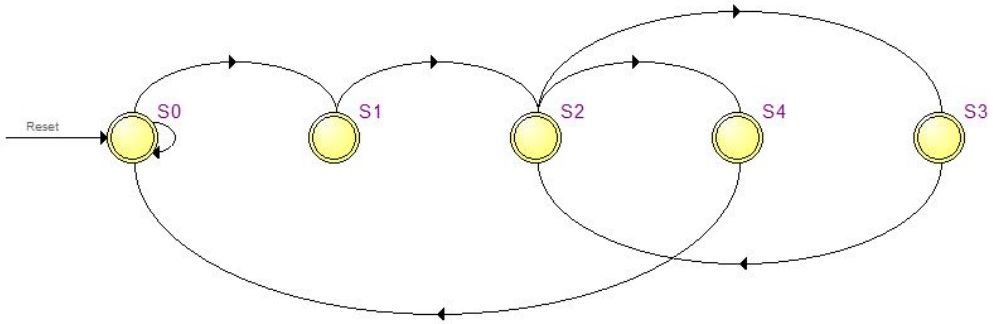
- Bloco Operativo



Multiplicador do Exemplo 5* do slide “Aula 5-T”

* modelo adaptado para Mealy

- Máquina de Estados do Bloco de Controle



State Table

	Source State	Destination State	Condition
1	S0	S1	(inicio)
2	S0	S0	(!inicio)
3	S1	S2	
4	S2	S3	(!aZ).(!bZ)
5	S2	S4	(!aZ).(bZ) + (aZ)
6	S3	S2	

Transitions | Encoding

Multiplicador do Exemplo 5* do slide “Aula 5-T”

* modelo adaptado para Mealy

- Simulação de ondas - ModelSim

Entrada A = 0011 (03) | Entrada B = 0100 (04) | Saida = 1100 (12)

Multiplicador do Exemplo 5* do slide “Aula 5-T”

* modelo adaptado para Mealy

- Análise Comparativa - 4 Bits vs 8 Bits
  - Área

Total logic elements	30 / 4,608 (< 1 %)
Total combinational functions	20 / 4,608 (< 1 %)
Dedicated logic registers	26 / 4,608 (< 1 %)
Total registers	26
Total pins	16 / 158 (10 %)

4 Bits

Total logic elements	46 / 4,608 (< 1 %)
Total combinational functions	29 / 4,608 (< 1 %)
Dedicated logic registers	42 / 4,608 (< 1 %)
Total registers	42
Total pins	28 / 158 (18 %)

8 Bits

Multiplicador do Exemplo 5* do slide “Aula 5-T”

* modelo adaptado para Mealy

- Atraso

Minimum Clock to Output Times

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	pronto	clk	6.036	6.036	Rise	clk
2	mult[*]	clk	6.005	6.005	Rise	clk
1	mult[2]	clk	6.014	6.014	Rise	clk
2	mult[1]	clk	6.006	6.006	Rise	clk
3	mult[3]	clk	6.006	6.006	Rise	clk
4	mult[0]	clk	6.005	6.005	Rise	clk

4 Bits

Minimum Clock to Output Times

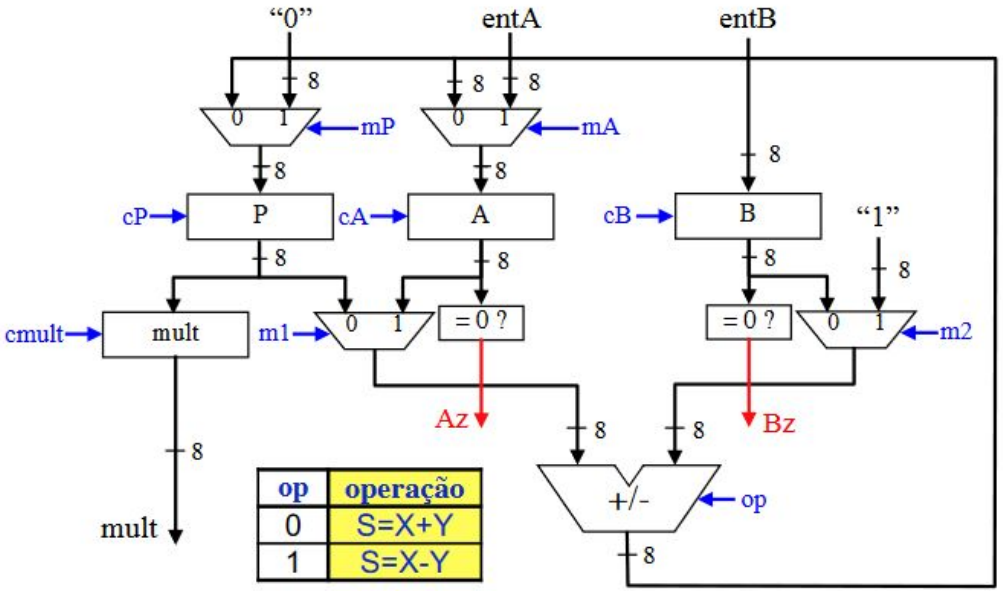
	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	pronto	clk	5.957	5.957	Rise	clk
2	mult[*]	clk	5.678	5.678	Rise	clk
1	mult[2]	clk	6.049	6.049	Rise	clk
2	mult[6]	clk	5.994	5.994	Rise	clk
3	mult[4]	clk	5.992	5.992	Rise	clk
4	mult[1]	clk	5.981	5.981	Rise	clk
5	mult[3]	clk	5.960	5.960	Rise	clk
6	mult[7]	clk	5.855	5.855	Rise	clk
7	mult[5]	clk	5.718	5.718	Rise	clk
8	mult[0]	clk	5.678	5.678	Rise	clk

8 Bits

Multiplicador do Exemplo 4* do slide “Aula 5-T”

* modelo adaptado para Mealy

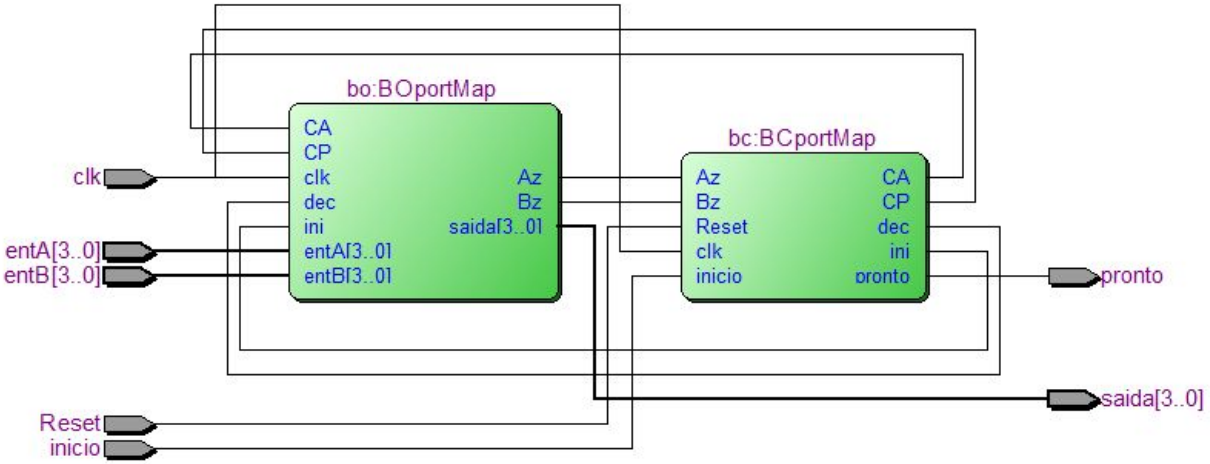
- Bloco Operativo



Multiplicador do Exemplo 4* do slide “Aula 5-T”

* modelo adaptado para Mealy

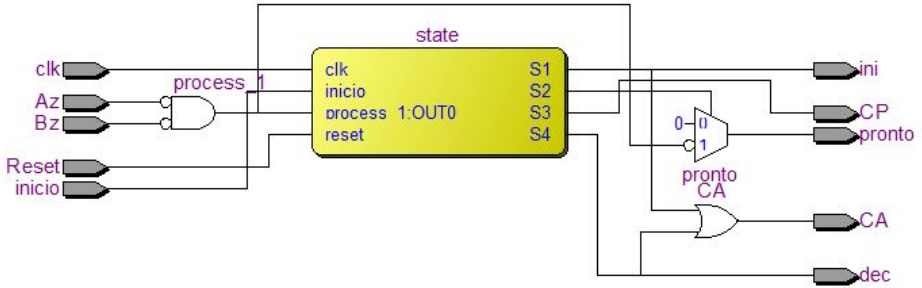
- Netlist
  - Versão Completa



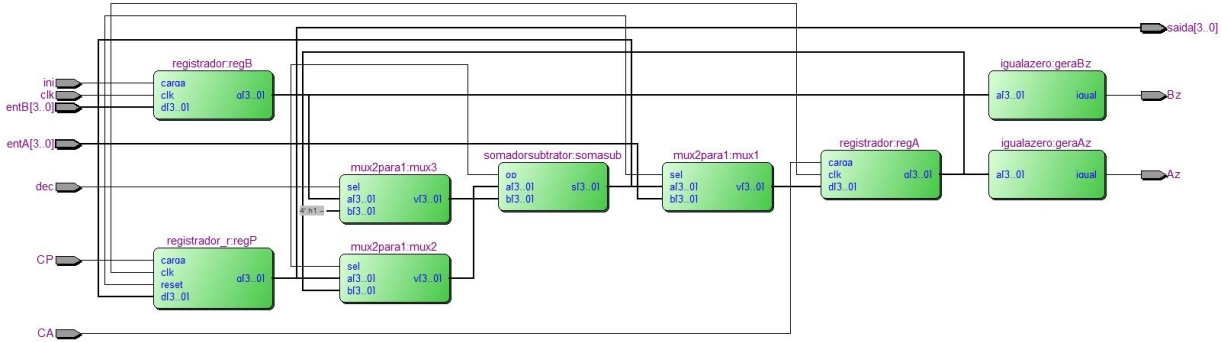
Multiplicador do Exemplo 4* do slide “Aula 5-T”

* modelo adaptado para Mealy

- Bloco de Controle



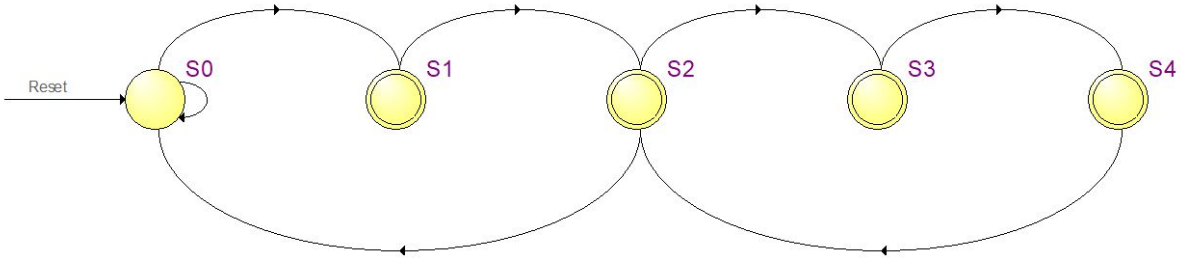
- Bloco Operativo



Multiplicador do Exemplo 4* do slide “Aula 5-T”

* modelo adaptado para Mealy

- Máquina de Estados do Bloco de Controle

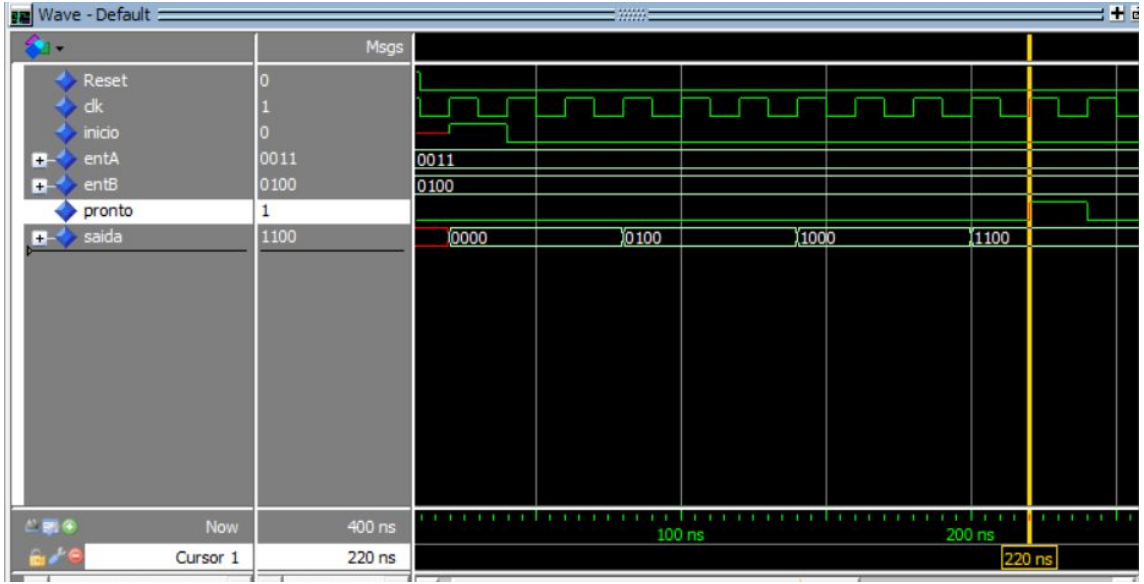


	Source State	Destination State	Condition
1	S0	S0	(!inicio)
2	S0	S1	(inicio)
3	S1	S2	
4	S2	S0	(!process_1)
5	S2	S3	(process_1)
6	S3	S4	
7	S4	S2	

Multiplicador do Exemplo 4* do slide “Aula 5-T”

* modelo adaptado para Mealy

- Simulação de ondas - ModelSim



Entrada A = 0011 (03) | Entrada B = 0100 (04) | Saída = 1100 (12)

Multiplicador do Exemplo 4* do slide “Aula 5-T”

* modelo adaptado para Mealy

- Análise Comparativa - 4 Bits vs 8 Bits
  - Área

Total logic elements	30 / 4,608 (< 1 %)
Total combinational functions	24 / 4,608 (< 1 %)
Dedicated logic registers	17 / 4,608 (< 1 %)
Total registers	17
Total pins	16 / 158 (10 %)

4 Bits

Total logic elements	45 / 4,608 (< 1 %)
Total combinational functions	43 / 4,608 (< 1 %)
Dedicated logic registers	29 / 4,608 (< 1 %)
Total registers	29
Total pins	28 / 158 (18 %)

8 Bits

Multiplicador do Exemplo 4* do slide “Aula 5-T”

* modelo adaptado para Mealy

- Atraso

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	pronto	clk	6.822	6.822	Rise	clk
2	saida[*]	clk	6.093	6.093	Rise	clk
1	saida[0]	clk	6.324	6.324	Rise	clk
2	saida[2]	clk	6.320	6.320	Rise	clk
3	saida[3]	clk	6.094	6.094	Rise	clk
4	saida[1]	clk	6.093	6.093	Rise	clk

4 Bits

Minimum Clock to Output Times

	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	pronto	clk	7.103	7.103	Rise	clk
2	saida[*]	clk	5.946	5.946	Rise	clk
1	saida[2]	clk	6.479	6.479	Rise	clk
2	saida[5]	clk	6.307	6.307	Rise	clk
3	saida[1]	clk	6.246	6.246	Rise	clk
4	saida[0]	clk	6.200	6.200	Rise	clk
5	saida[3]	clk	6.052	6.052	Rise	clk
6	saida[6]	clk	6.012	6.012	Rise	clk
7	saida[4]	clk	6.009	6.009	Rise	clk
8	saida[7]	clk	5.946	5.946	Rise	clk

8 Bits

Conclusão

- Circuitos mais rápidos geralmente tem maior área;
- Ter menos estados garante um menor tempo de execução;
    - Sendo assim, máquinas de Mealy geralmente são mais eficientes, já que geram menos estados.
- menos elementos/ melhor arranjo