RISC-V Architecture for Motion Planning Algorithms in Autonomous Drone Applications

A senior design project submitted in partial fulfillment of the requirements for the degree of Bachelor of Science at Harvard University

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Abstract

This thesis aims to design RISC-V computer architecture that supports the fast execution of motion planning algorithms for drone applications. First, the computation of sampling-based motion planning algorithms commonly used in autonomous drones (such as Rapidly-exploring Random Tree (RRT), Rapidly-exploring Random Tree Star (RRT*), Probabalistic Road Map (PRM)) will be profiled on an unmodified RISC-V processor. From this profiling, common bottlenecks and hotspots in execution will be identified. Based on these results, this project will extend the RISC-V Instruction Set Architecture (ISA) and design a modified processor to support the extensions.

Contents

List of Acronyms

ISA Instruction Set Architecture

PRM Probabalistic Road Map

RRT Rapidly-exploring Random Tree

RRT* Rapidly-exploring Random Tree Star

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Chapter 1

Introduction

This is a pretend citation[1]

Bibliography

[1] S. Murray, W. Floyd-Jones, Y. Qi, D. Sorin, G. Konidaris, and D. Robotics, "Robot Motion Planning on a Chip," tech. rep.

Appendices

Appendix A

Appendix 1