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CP1: Progress Report

Functionalities

This checkpoint, we implemented our datapath design for a basic pipelined processor. We also implemented the control_rom module that is used to send control signals through the pipeline. The pipeline handles all of the RV32I instructions (except for the noted exceptions). The pipeline currently does not handle hazards and uses a dual-port “magic” memory instead of split caches.

Contributions

Anthony worked on the control ROM using the MP2 controller as a baseline for what control signals to send during an opcode. Hemang updated and refined the ROM to add additional signals for the pipeline. He also implemented the stage “barriers” (if_id, id_exe, etc.) and added registers to hold values needed for the current instruction. Each member worked on the implementation and debugging of the datapath

Testing Strategies

To verify the design, we looked at the values coming through each stage are the expected values. For example, we made sure that values for the *current* instruction were correct and expected. We realized that some of the values the current instruction needed were being changed so we decided to have registers that hold values of the control signal at each “barrier” stage. To verify the entire pipeline, we used the provided testcode and ensured that the expected values were correct.