RISC-V Pipelined Processor

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Advanced Features

1. Basic Hardware Prefetching
2. Pipelined L1 Caches
3. Tournament Branch Predictor

Performance Analysis

- Prefetching performed worst.
- 5ms vs 7ms execution time.
- Resulted in larger miss penalty.
- Fetch line i+1 when line i is accessed.
- Offset = (line_i_starting_address + 32).

What We Could Have Done Differently

- Fully verify designs.
- Utilize debugging tools.
- Start early (the classic…).
- Integrating the MP3 Cache

Thank you