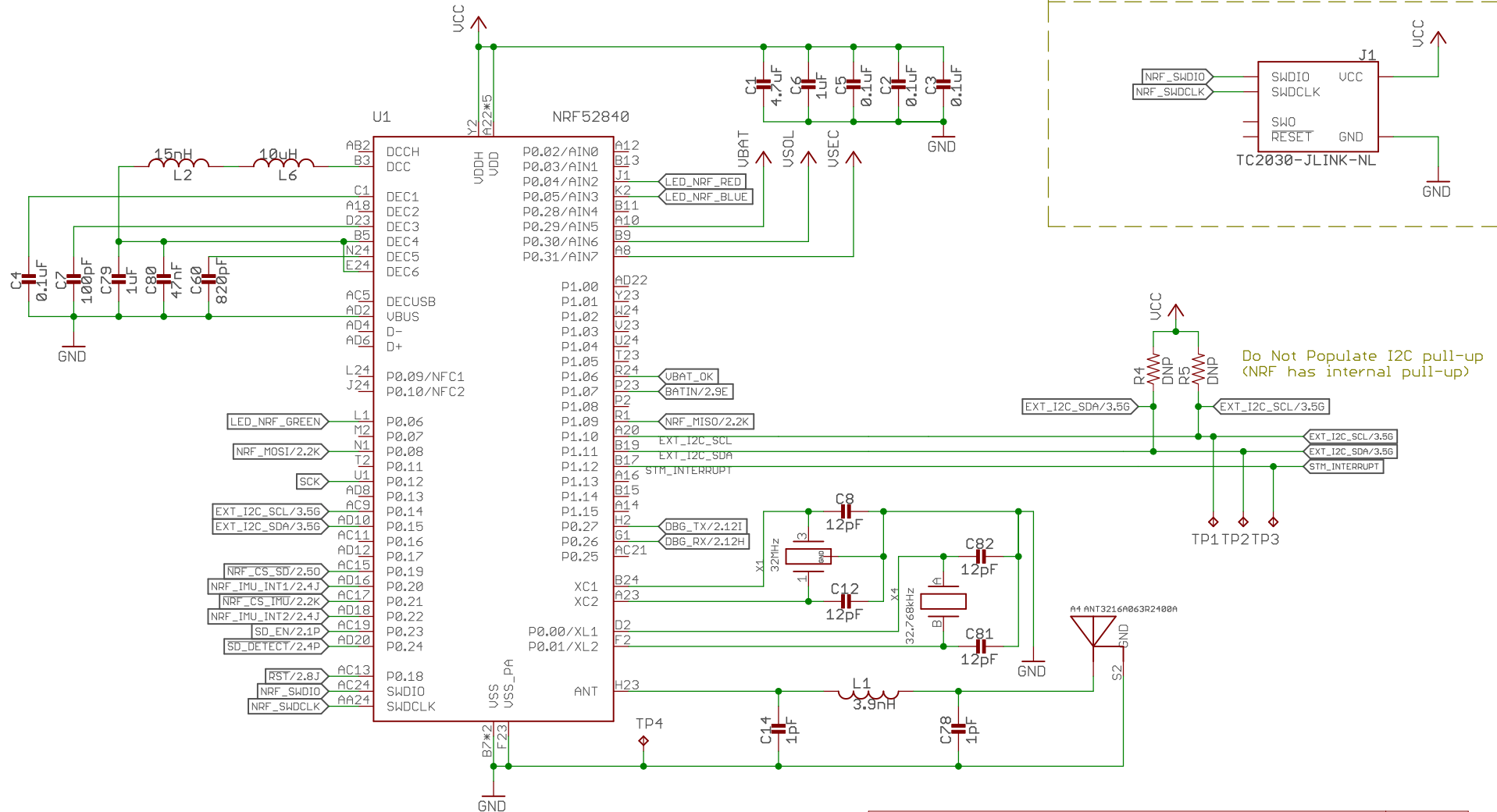


nRF52840 BLE



Power Supply and Charging

The schematic diagram illustrates the power supply and charging circuit for the DW1000 module. It features two USB connectors, J1 and J3, both providing +5V, D-, D+, ID, and GND pins. The circuit includes a USB-to-UART bridge IC (U1, FT232RL), a USB-to-serial IC (U2, MCP73831), and a linear voltage regulator (U4, MAX8887EZK33+T). The power supply is regulated to 3.3V. The charging circuit is implemented using a diode (D1, GREEN) and a resistor (R2, 1k). The output of the regulator is connected to the VCC pin of the DW1000 module. The circuit also includes several passive components: capacitors C13 (1uF), C14 (4.7uF), C15 (10nF), and C16 (4.7uF); resistors R3 (2k 1%), R7 (2.2M), R8 (10M), and R9 (10M); and a battery symbol (BATIN/1.61). A note indicates that the voltage regulator must be a stable LDO for the DW1000.

Must be a stable LDO for the DW1000.

Accelerometer

Antennas

A5 TAIYO-YUDEN-AH086M

A2,TAIYO-YUDEN-AH086M

A2 TAIYO-YUDEN-AH086M

RF 1/3.6A

RF 2/3.6B

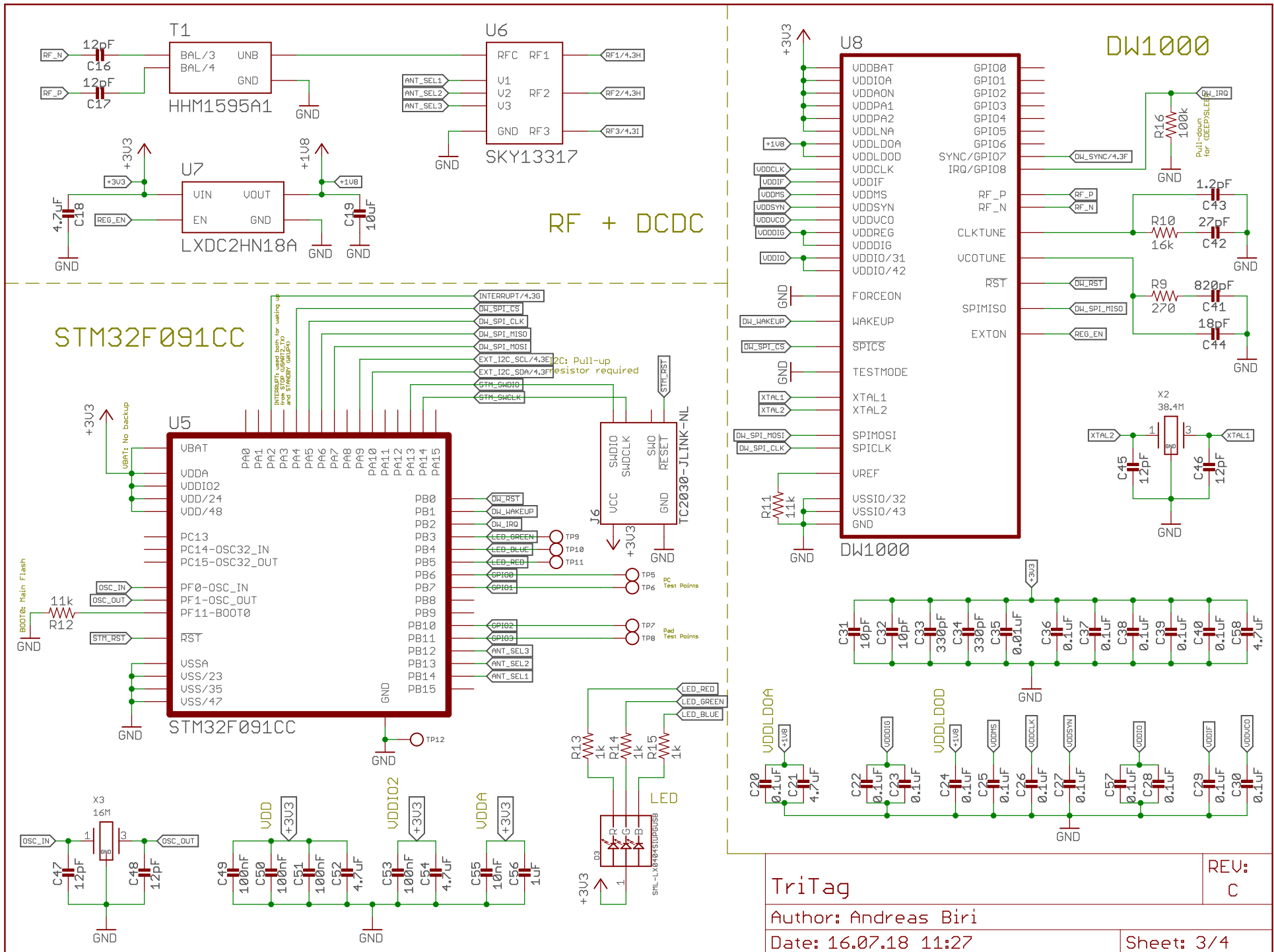
RF 3/3.6C

SD Card Adapter

The schematic diagram illustrates the internal wiring of an SD Card Adapter. Key components and connections include:

- U12 (SIP32510):** A multi-pin IC with pins labeled ULOAD, USUPP, EN, and GND. It is connected to a 5*2 pin header.
- Resistors:**
 - R19 (100k) connects the EN pin to the SD_EN/1.3M header.
 - R20 (100k), R21 (10k), R22 (10k), and R23 (10k) are pull-up resistors for the NR*_MISO/1.6J, NR*_CS_SD/1.3L, NR*_MOSI/1.3J, and NR*_SCK headers, respectively.
- Capacitor:** C77 (4.7uF) is connected between the USUPP pin and GND.
- Signal Lines:**
 - DATA0/MISO is connected to pin 4.
 - DATA1/RSV is connected to pin 7.
 - DATA2/NC is connected to pin 10.
 - DATA3-CD/CS_N is connected to pin 1.
 - CMD/MOSI is connected to pin 6.
 - CLK is connected to pin 5.
 - GND is connected to pin 8.
- Other Connections:**
 - SD_DETECT/1.3M is connected to the bottom of the 4.7uF capacitor.
 - CARD_INSERTED is connected to the bottom of the 4.7uF capacitor and the CLK pin.

The board is identified as CON_MICRO_SDDM3AT-SF-PEJM5.



EXTERNAL SIGNALS

The following signals must be integrated into all designs using the design block:

— EXT_I2C_SCL/3.5G
— EXT_I2C_SDA/3.5G

Note: Additional I2C pull-up resistors required

— DW_SYNC/3.11C
— INTERRUPT/3.5F

— RF1/3.6A
— RF2/3.6B
— RF3/3.6C

TriTag		REV: C
Author: Andreas Biri		
Date: 16.07.18 11:27		Sheet: 4/4