

nRF52840 BLE

PCB layout for nRF52840 BLE module. The diagram shows the nRF52840 chip (U7) connected to various components including LEDs (LED\_NRF\_BLUE, LED\_NRF\_RED, LED\_NRF\_GREEN), a debugger (TC2030-JLINK-NL), and an antenna (A1 ANT3216A063R2408A). The layout includes power supply connections (+3V3, GND), decoupling capacitors (C61, C55, C33, C30, C31), and various other components like resistors (R4, R5, R6), inductors (L2, L6), and connectors (J1, J4). The nRF52840 pinout is detailed on the right side of the chip, showing connections for pins A12 through A24, B1 through B11, and C1 through C6.

Key components and connections:

- Power:** +3V3 supply connected to VDD and UDD pins. Ground connections at multiple points.
- LEDs:** LED\_NRF\_BLUE (A12), LED\_NRF\_RED (B11), LED\_NRF\_GREEN (B13).
- Debugger:** TC2030-JLINK-NL connected to SWDIO, SWDCLK, SWO, RESET, and GND.
- Antenna:** A1 ANT3216A063R2408A connected to H23 and F23.
- Decoupling:** Capacitors C61, C55, C33, C30, C31 for power supply decoupling.
- Timing:** Various capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100) and inductors (L1, L2, L3, L4, L5, L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, L21, L22, L23, L24, L25, L26, L27, L28, L29, L30, L31, L32, L33, L34, L35, L36, L37, L38, L39, L40, L41, L42, L43, L44, L45, L46, L47, L48, L49, L50, L51, L52, L53, L54, L55, L56, L57, L58, L59, L60, L61, L62, L63, L64, L65, L66, L67, L68, L69, L70, L71, L72, L73, L74, L75, L76, L77, L78, L79, L80, L81, L82, L83, L84, L85, L86, L87, L88, L89, L90, L91, L92, L93, L94, L95, L96, L97, L98, L99, L100) for timing and signal conditioning.

TriTag

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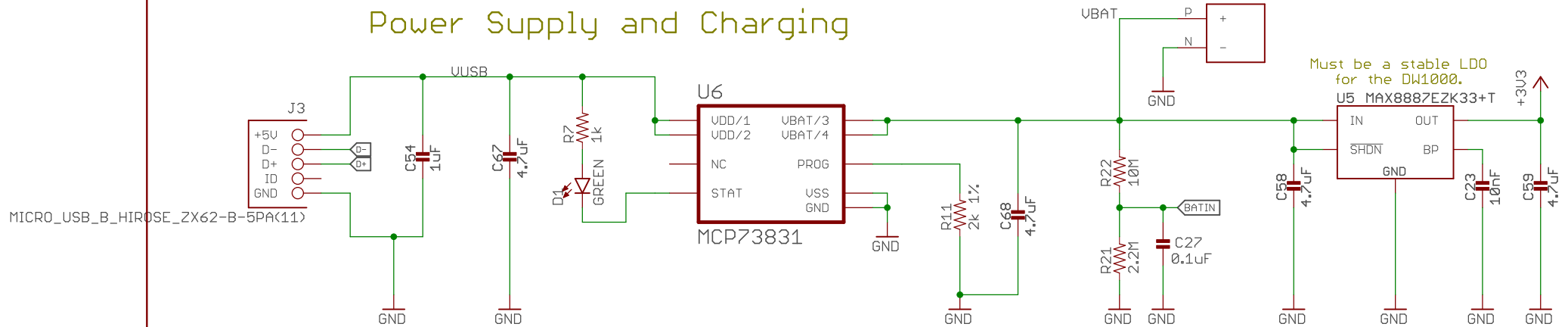
Date: 23.07.18 10:44

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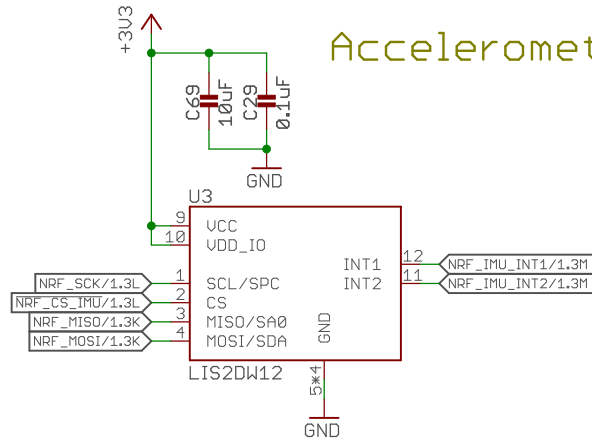
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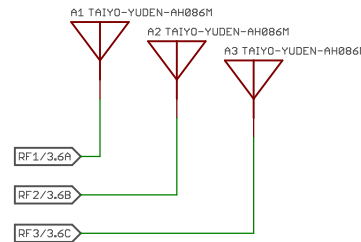
## Power Supply and Charging



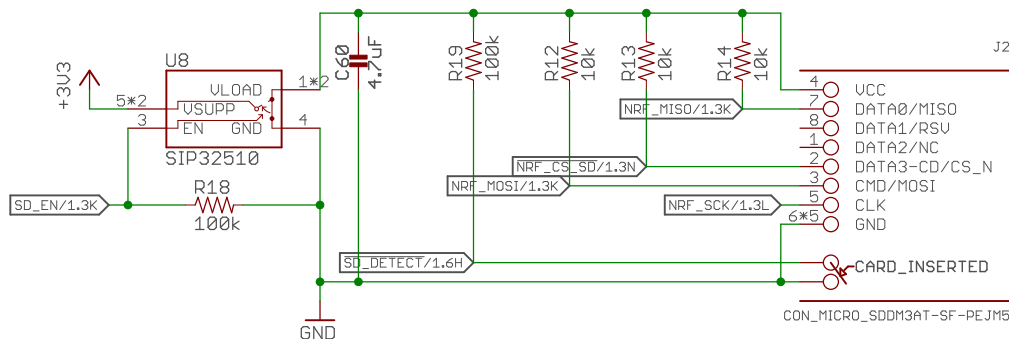
## Accelerometer



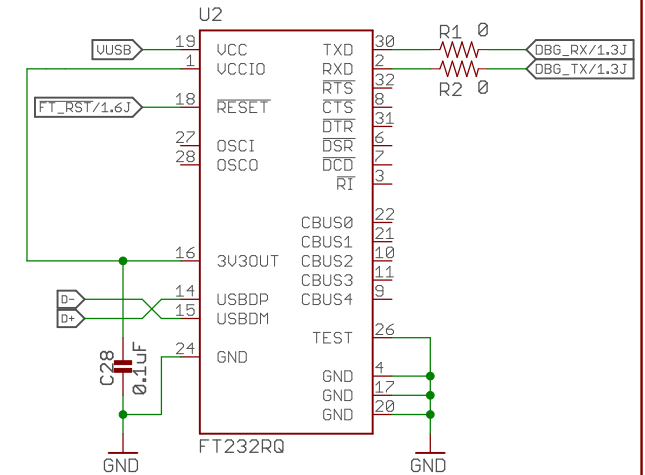
## Antennas



## SD Card Adapter



## USB-Serial



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## EXTERNAL SIGNALS

The following signals must be integrated into all designs.

### Signals

—  EXT\_I2C\_SCL/3.5G

—  EXT\_I2C\_SDA/3.5G

—  DW\_SYNC/3.10C


—  STM\_INTERRUPT/3.5F

Note: Additional I2C pull-up required.

### Antennas

—  RF1/3.6A

—  RF2/3.6B

—  RF3/3.6C

Guarantee 120° offset in-between

RF traces should respect the keep-out zone.  
Furthermore, try to keep them as short as possible.

### Power Supply

—  +3V3/3.10K

Be aware that the DecaWave is v

We suggest using the "MAX887EZ".  
You can find a reference layout

signs using the design block:

resistors required to +3V3

antennas to maximize polarization difference and antenna diversity

apout zones and be surrounded by a via shield.  
short and straight as possible

ery sensitive regarding its power supply.

"K33+T" from Maxim Integrated.  
at [github.com/lab11/polypoint/pcb/tritag](https://github.com/lab11/polypoint/pcb/tritag).

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