

## Lecture 7.1

## Combinational Logic Design II

First part had, decoders, encoders, tri-state Buffers

Part II, we look at other combinational logic components

We Look at

- Multiplexers (MUX)
- De Multiplexers (DeMux)
- Adders, comparators

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## Multiplexer

MUX sizes  
 $2:1, 4:1, 8:1, 16:1 \dots$   
 $2^n:1$        $n = \# \text{ of select lines}$

What is it used for? Used to select one data input from many data inputs || Many to one

What are its inputs? Two Types

- (1) data inputs
- (2) select inputs

2 bits required to select from 4 inputs

To choose data inputs you need select inputs

what are its outputs?

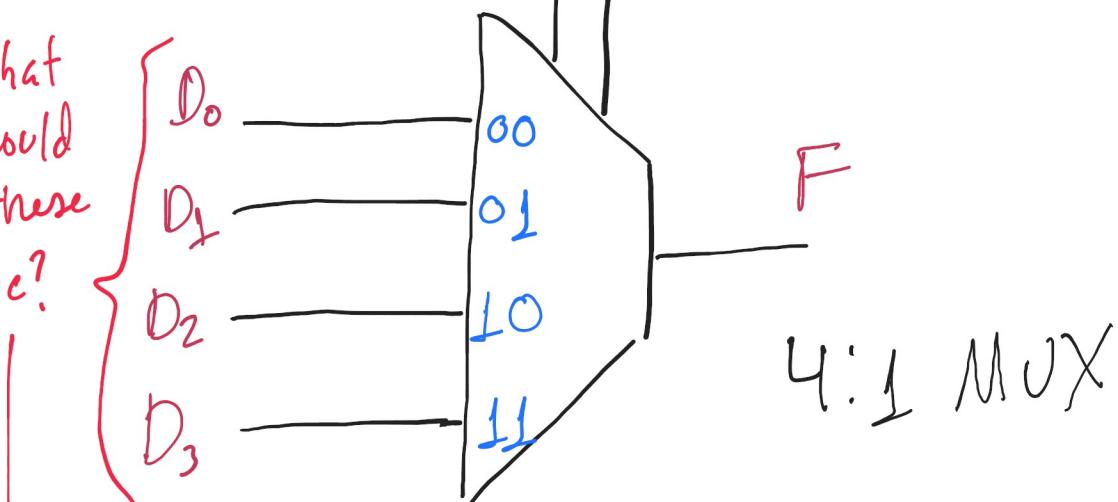
One of the data inputs

Many to one

Symbol?

$S_1 S_0 \rightarrow$  ms select is to the left

what could these be?



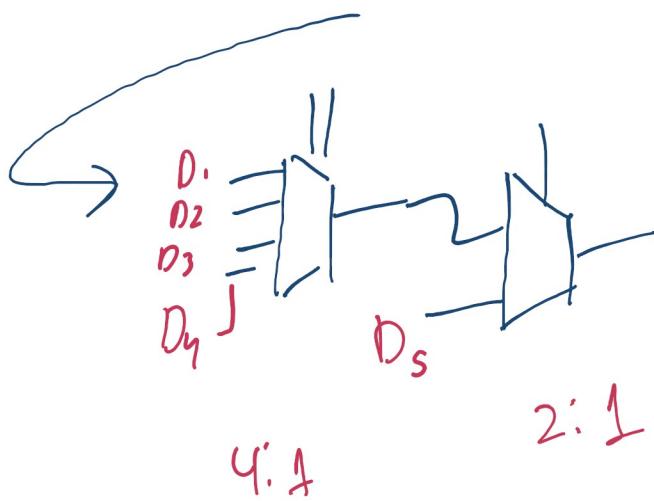
variable, or expressions,  
or Logic 0's or 1's

Ex) How to make 5:1 MUX

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→ use 8:1 MUX

or use 4:1 and 2:1



What statements we can write about the 4:1 symbol?

— specifically, the statements mean this

$$S_1 = 0 \quad S_0 = 0, \quad F = D_0$$

$$S_1 = 0 \quad S_0 = 1, \quad F = D_1$$

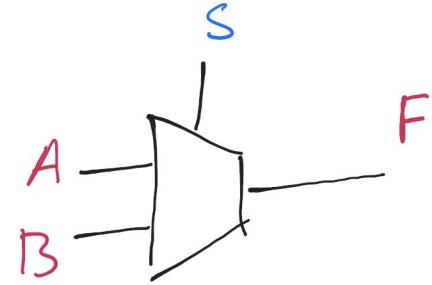
$$S_1 = 1 \quad S_0 = 0, \quad F = D_2$$

$$S_1 = 1 \quad S_0 = 1, \quad F = D_3$$

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## Design a 2:1 MUX

TT, K-map, Logic diagram



Description

$$S = 0, F = A$$

~~$$S = 1, F = B$$~~

S	A	B	F
0	0	0	0 = $\bar{S}\bar{A}\bar{B} = m_0$
0	0	1	0 = $\bar{S}\bar{A}B = m_1$
0	1	0	1 = $\bar{S}A\bar{B} = m_2$
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

So now that we have a truth table, we now have to make the circuit diagram.

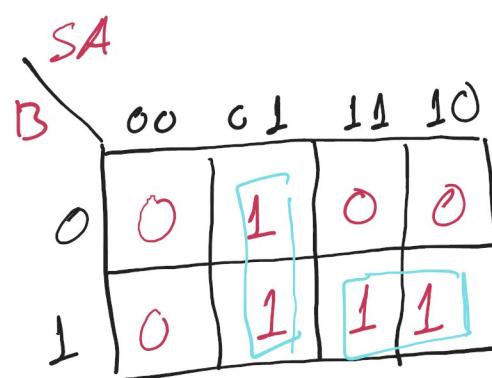
- USE K-Map to make it

we don't want to do it in the canonical manner

$$(F = \sum_m (\underline{\quad}))$$

→ we want the simplest form

→ use K-map to get Simplest SoP



$$F = \bar{S}A + SB$$

if  $S = 0$

$A$  goes thru

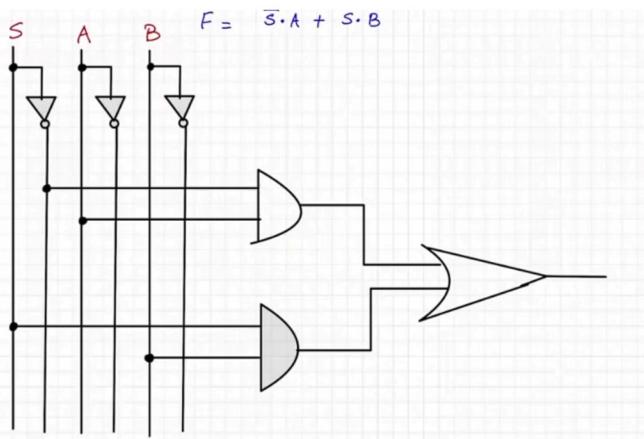
if  $S = 1$   
 $B$  goes thru

$$F = \bar{S}A + SB \text{ makes sense}$$

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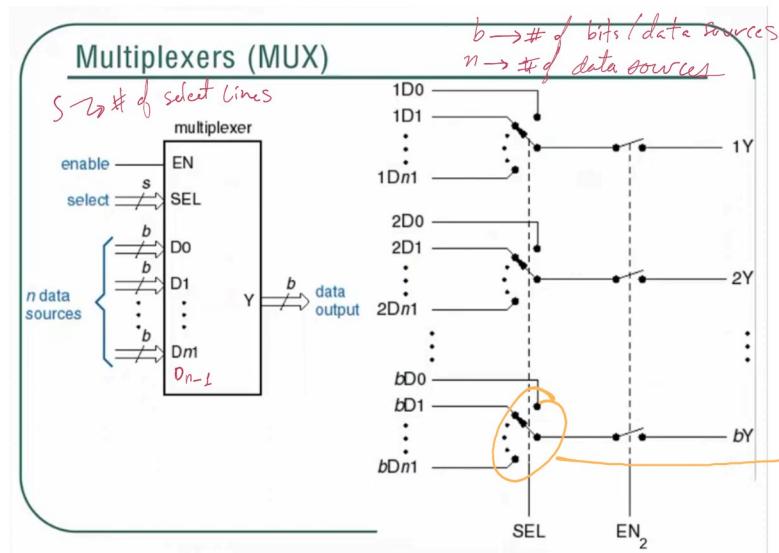
## Logic diagram 2:1 MUX

$$F = \bar{S} \cdot A + S \cdot B$$



This diagram will be inside a 2:L MUX

## Switch Model Multiplexer



Multiplexers can have an enable, select lines, and a bunch of Data inputs

And one Data Output

These are called commutators

NOTES:  $s$  = the number of select lines  
 $n$  = the number of data sources

Earlier we were talking about data sources of 1 bit in size. But data sources can be several bits in size

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$b$  = number of bits in size of each data source

(One data source of size  $b$  bits)

One data source is selected and is selected to be the output  $Y$  of  $b$  bits in size

We now ask ourselves, what's the relationship between  $s$  (number of selects) and  $n$  (number of data sources)?

-For  $n$ , what should  $s$  be?

$$n = 2^s \quad \checkmark$$

$$s = \log_2 n$$

In reality, we can have more select lines than we need.

$$s \geq \log_2 n$$

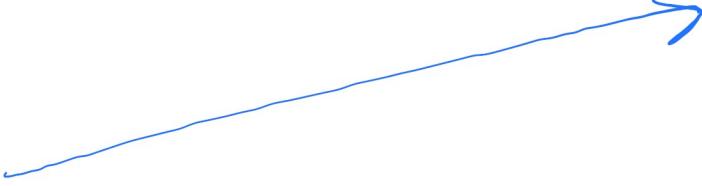
We can see that  $EN_2$  acts as a switch that turns on/off all connections to  $1Y, 2Y, \dots bY$ .

SEL is more involved

SEL is choosing the first bit of the Data source 7  
either  $1D_0, 1D_1, \dots, 1D_{n-1}$  to send to  $1Y$   
1 bit sent (1st bit)

Then  $2D_0, 2D_1, \dots, 2D_{n-1}$  to send to  $2Y$   
1 bit sent (2nd bit)

Eventually  $bD_0, bD_1, \dots, bD_{n-1}$  sent to  $bY$   
1 bit sent (bth bit  
sent, last bit)



$Y$  is of size  $b$

How do I select  $D_0$ ?

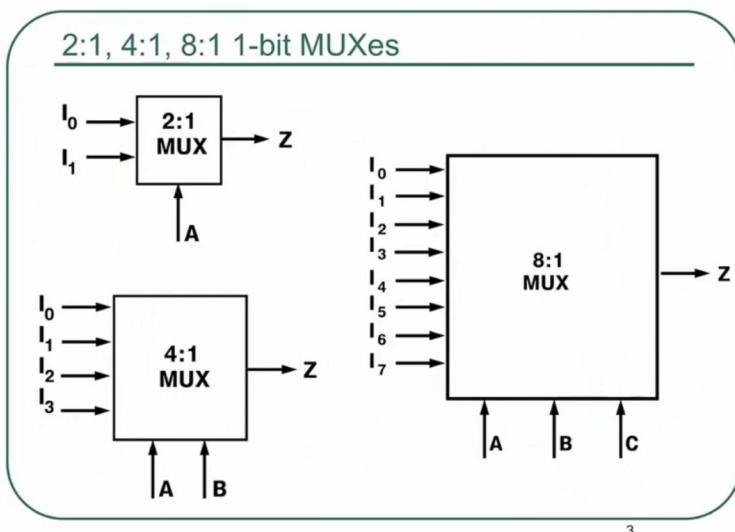
- We select (SEL) the 1st bit of  $D_0$  ( $1D_0$ )  
then select the 2nd bit of  $D_0$  ( $2D_0$ )

And we keep going until we get to the bth bit of  
 $D_0$  ( $1D_{n-1}$ )

$1D_{n-1}$  (to be precise)

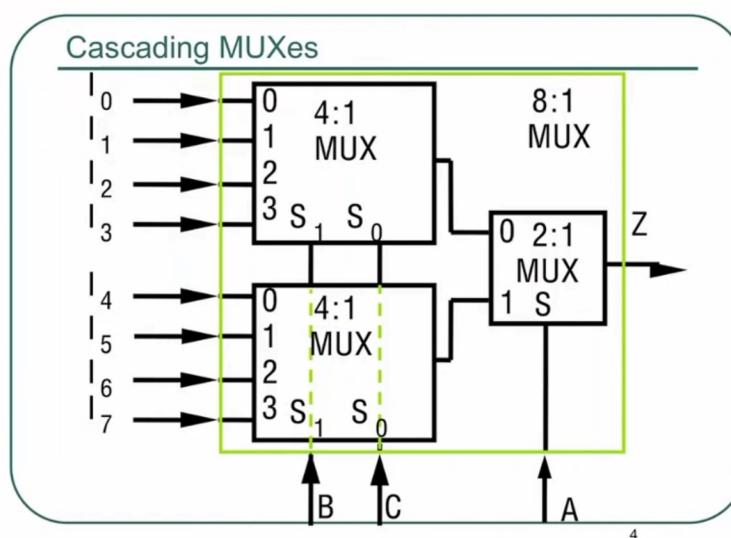
8 we have a total of  $b$  commutators

## sizes of MUX



This should be pretty straight forward

## Cascading MUX (Daisy chain MUXs)



Can we design an 8:1 MUX with 2 4:1 MUXs and 1 2:1 MUX?

Data sources go to top MUX or bottom MUX

$B$  and  $C$  Both control Both MUXs

( $B$  is tied to  $S_1$  of Both MUXs and  $C$  is tied to  $S_0$  of Both MUXs)

B and C select the Data source from both 4:1 MUX  
 and then A slects the final Data source selected from  
 The 4:1 MUXs    → selects via the 2:1 MUX

Therefore we can say

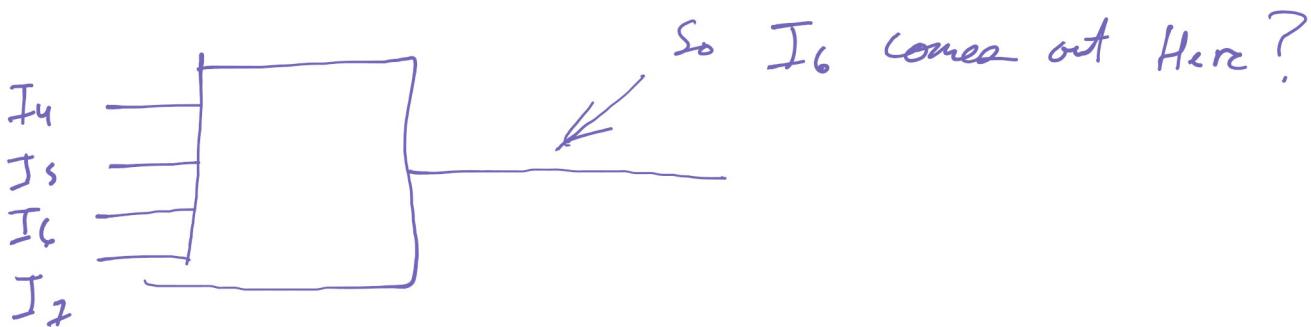
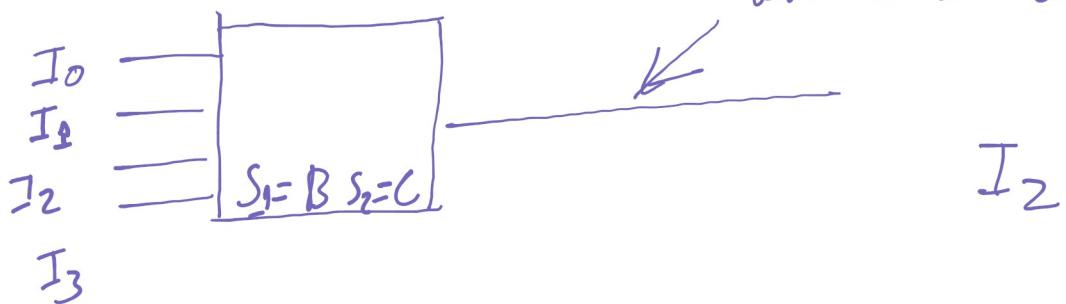
A = Most significant Select

B = 2nd significant Select

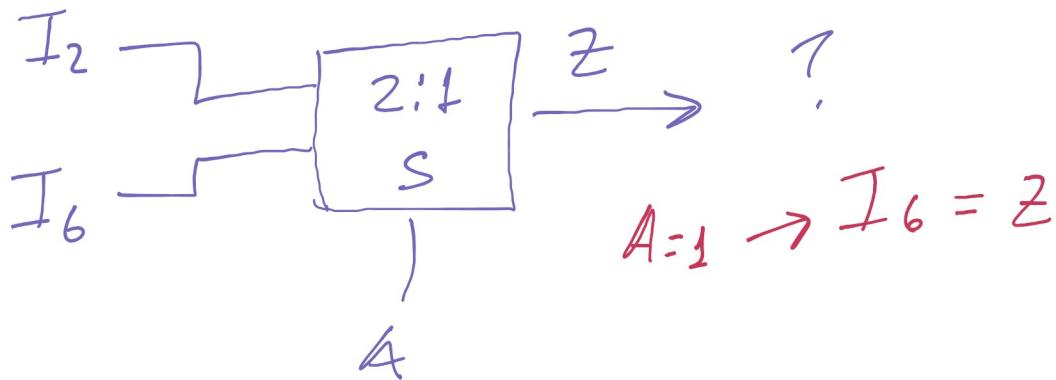
C = Least significant Select

Ex) what is  $I_2$  when  $A=1, B=1, C=0$

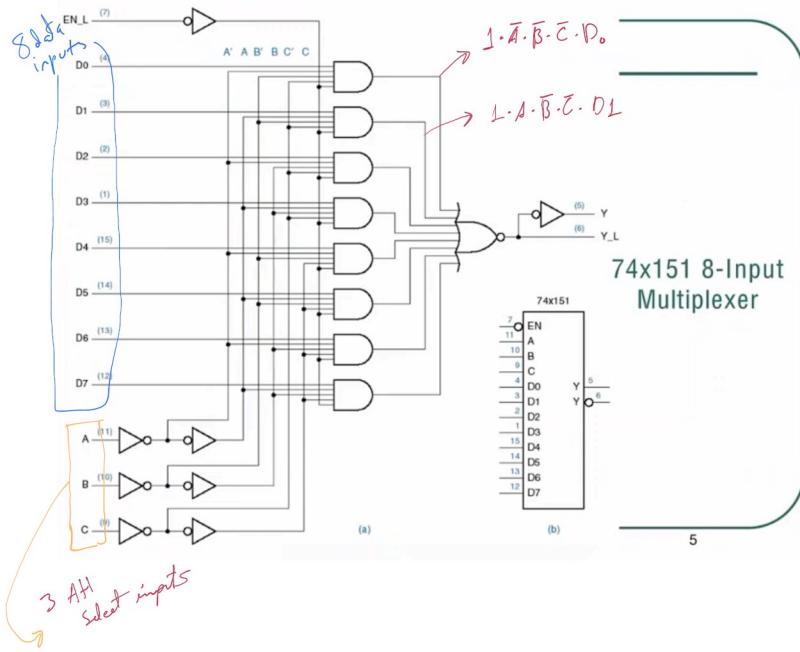
what comes out here?



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## 8 input Multiplexer



To select 1 out of 8 inputs we are going to need 3 selectors

— We have 3 AH select lines

8 Data Sources  
(Data inputs 1 bit each)

— AL Enable

outputs are in True form and complemented form

We follow the circuit diagram to find out the intermediate signals

$$1 \cdot \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D_0$$

$$1 \cdot A \cdot \bar{B} \cdot \bar{C} \cdot D_1$$

We can see that A is our LS bit

To make it clear,

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$$\text{if } A=B=C=0$$

$$Y=D_0 \quad \text{and} \quad Y_L = \overline{D_0}$$

Ex) what's  $Y = ?$  when  $A=1$

$$B=1$$

$$C=0$$

$$Y=D_3$$

$$Y_L = \overline{D_3}$$

## 2 Input, 4 bit MUX

Truth table for a 74x157 2-input, 4-bit multiplexer

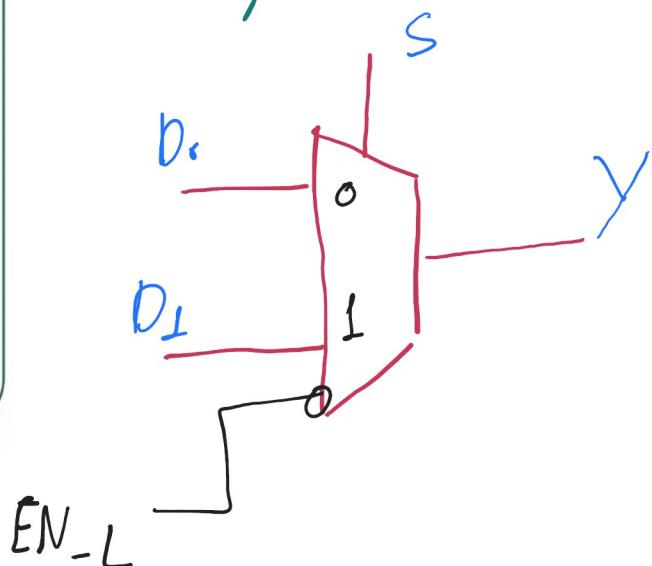
Inputs		Outputs			
EN_L	S	1Y	2Y	3Y	4Y
1	x	0	0	0	0
0	0	1D0	2D0	3D0	4D0
0	1	1D1	2D1	3D1	4D1

Table 6-43

Truth table for a 74x157 2-input, 4-bit multiplexer.

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We have 2 inputs where each input is 4 bits each



S can still be 2 bit length

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From the Truth Table,

$$\text{if } EN-L=0 \Rightarrow S=0$$

each Input  
is a 4 bit  
Input, so  
 $Y$  is a 4 bit  
output

$$\begin{aligned} 1D0 &= 1Y \\ 2D0 &= 2Y \\ 3D0 &= 3Y \\ 4D0 &= 4Y \end{aligned}$$

Here is the Internal circuit Diagram

Where have we seen this before?

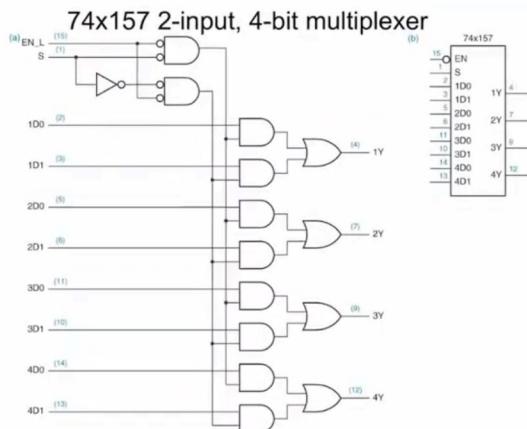
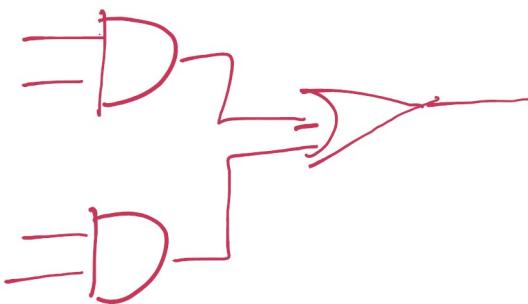


Figure 6-61

The 74x157 2-input, 4-bit multiplexer: (a) logic diagram; (b) traditional logic symbol.

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We have seen this before in the  
2:1 MUX Diagram

We are selecting from 2 to 1. Each of these is a 2 to 1 MUX

4 2:1 MUX

Each 2:1 MUX is selecting the 1st bit or the  
2nd bit or the 3rd bit or the fourth

Here's an example

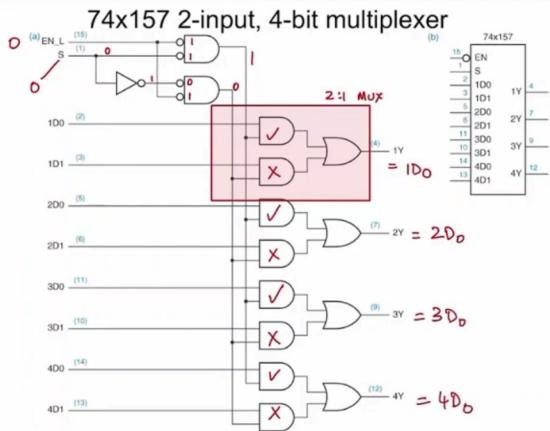


Figure 6-61

The  $74 \times 157$  2-input, 4-bit multiplexer: (a) logic diagram; (b) traditional logic symbol.