Minilab 1a

This is my public github repository: https://github.com/Antily15503/ECE554SP26_Minilab0
I created it by forking our team's github repo, and then adding my report to it.

Waveform image are in the corresponding minilab folder

The IP-based design was more resource-intensive in logic utilization. The pre-built IP was able to leverage the FPGA LUT blocks directly instead of synthesizing all logic from scratch. The tradeoff is around 2x increase in block memory, but this is expected since in IP state storage requires memory blocks.

Minilab 1b

Waveform image and simulation report is in the corresponding minilab folder

1. We basically simulated our design by running scenarios that may arise through operation of the hardware itself. At the end of each scenario, we check the output from the MAC module against expected (which we got from just doing multiplication directly) and displayed our output.

2. We pipelined our MAC

3. An image of using our design is also in the minilab folder. Essentially flipping the switch indicated will show us what value is in the MAC associated with the specified vector (indicated by the other switches)

4. For Signaltap: We used AVM_READ as our trigger with a sample of 1k, image is in the minilab folder.

5. We had a few difficulties across different parts of the minilab. The biggest one was debugging our FIFO, where our signals seemed to be coming in all at the same clock signal, rather than being staggered. Initially we didn't think this was a problem, but it caused errors in getting proper values to be displayed on the FPGA. We found this problem after debugging and analyzing the waveform, which took up a big part of our labtime.