2.4.1 Modeling Simple Circuits

Figure 2.1

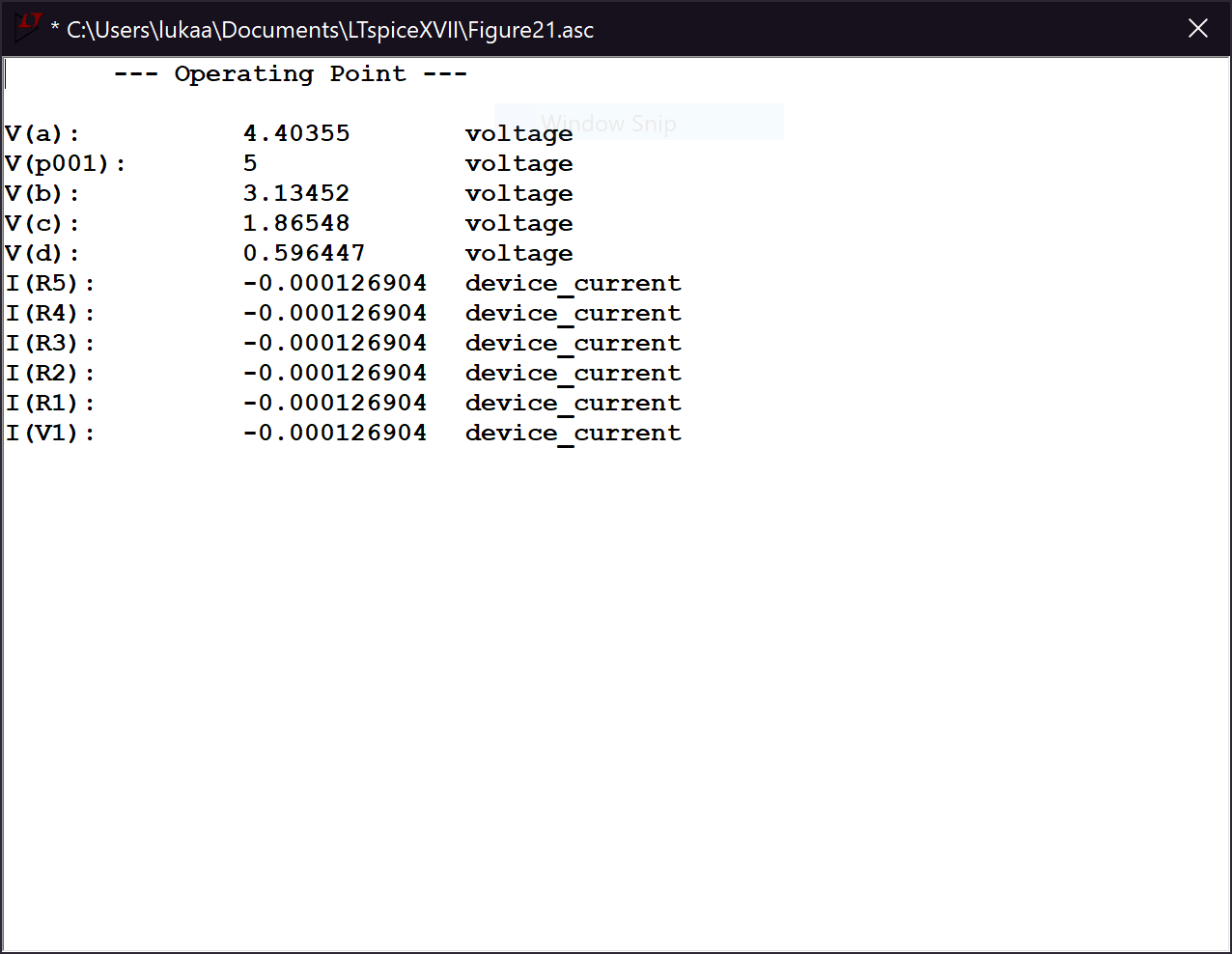
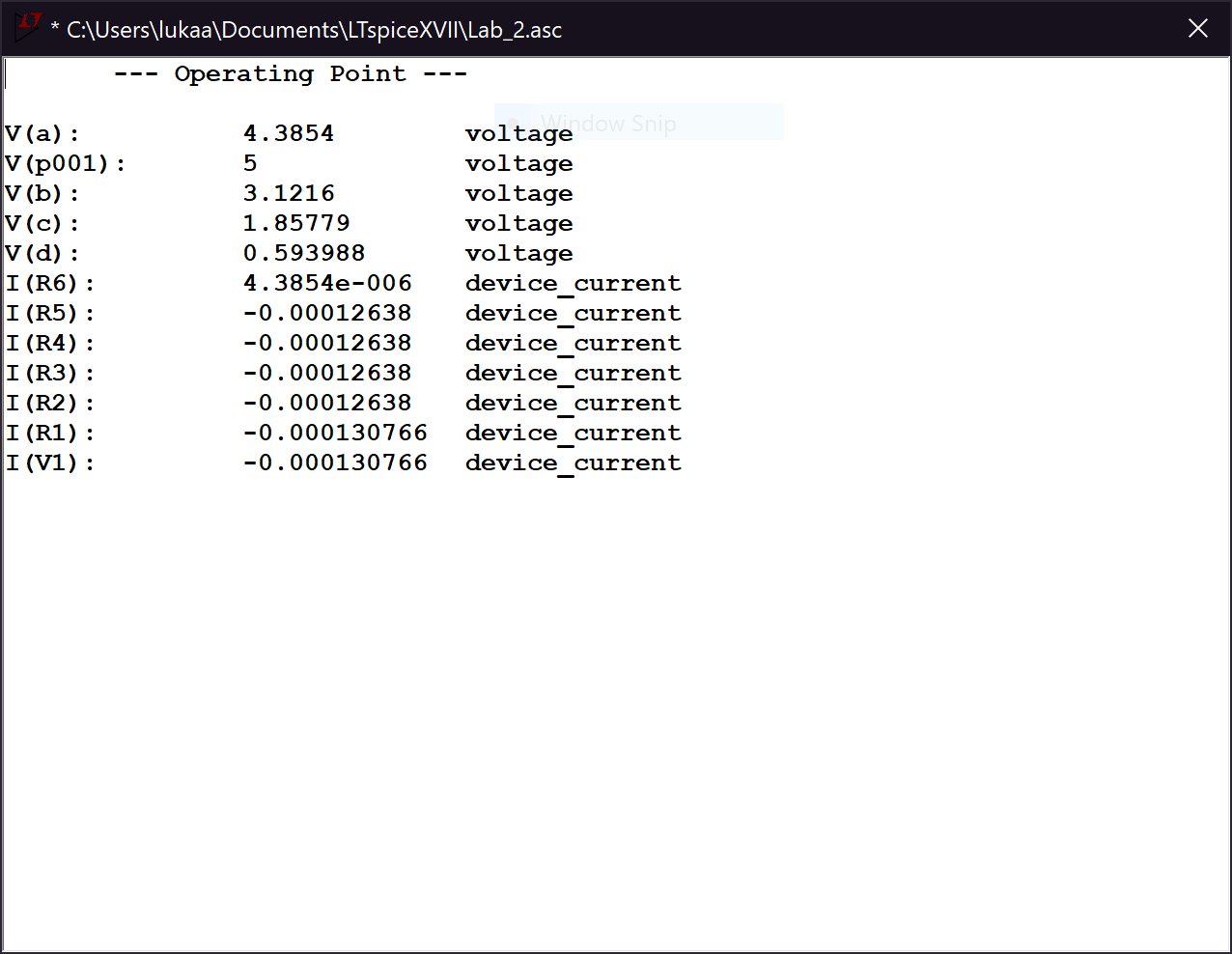
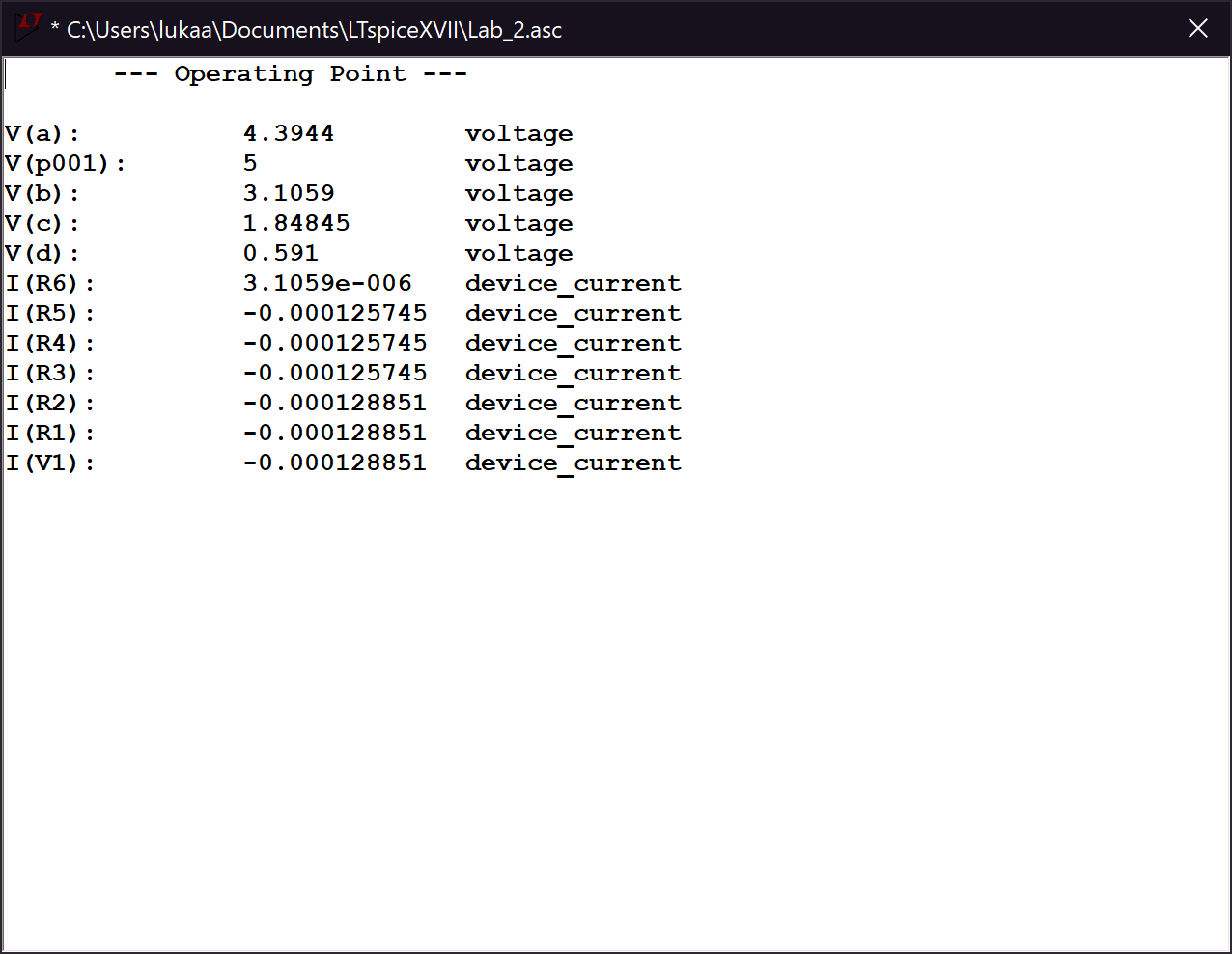


Figure 2.2

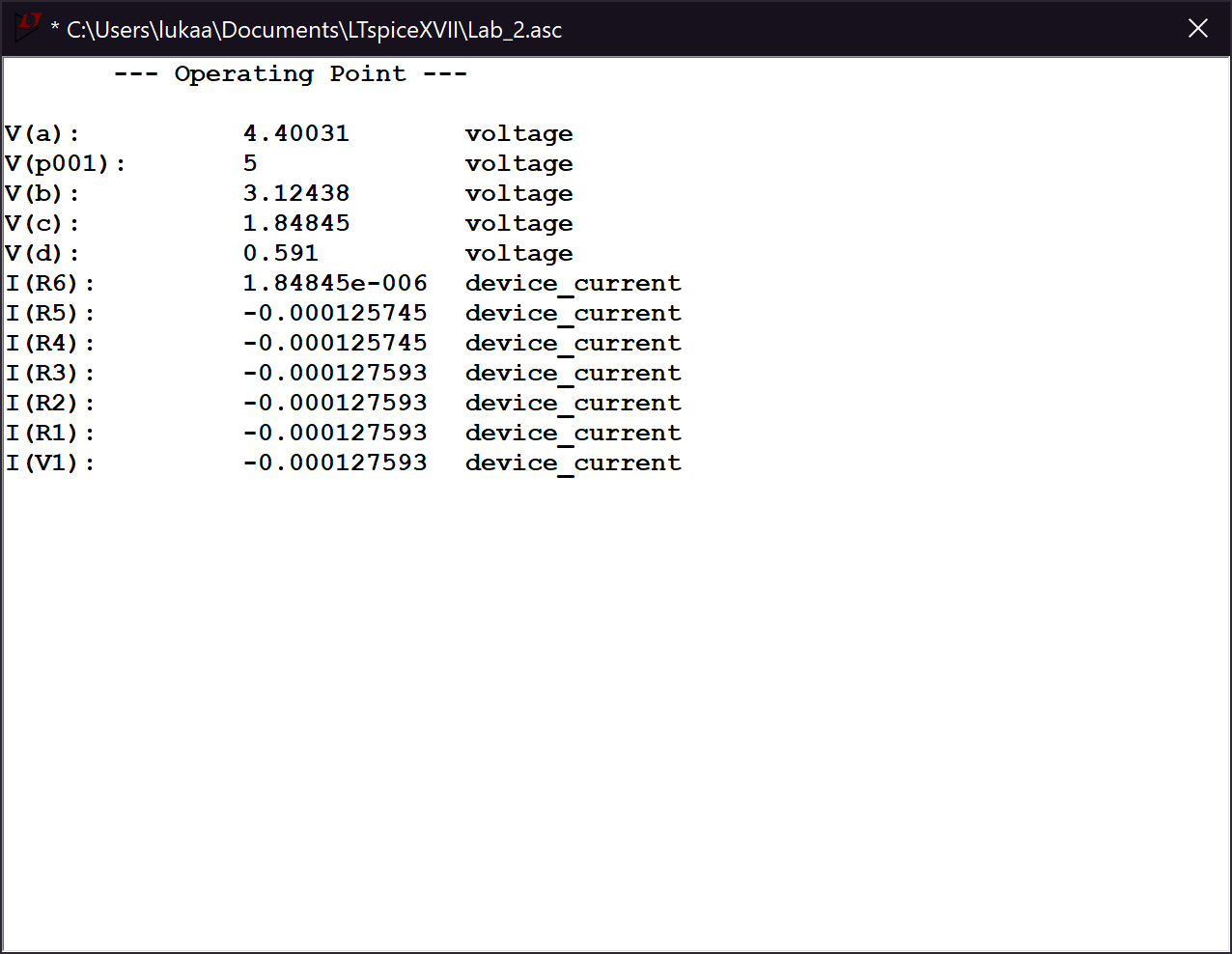
a)



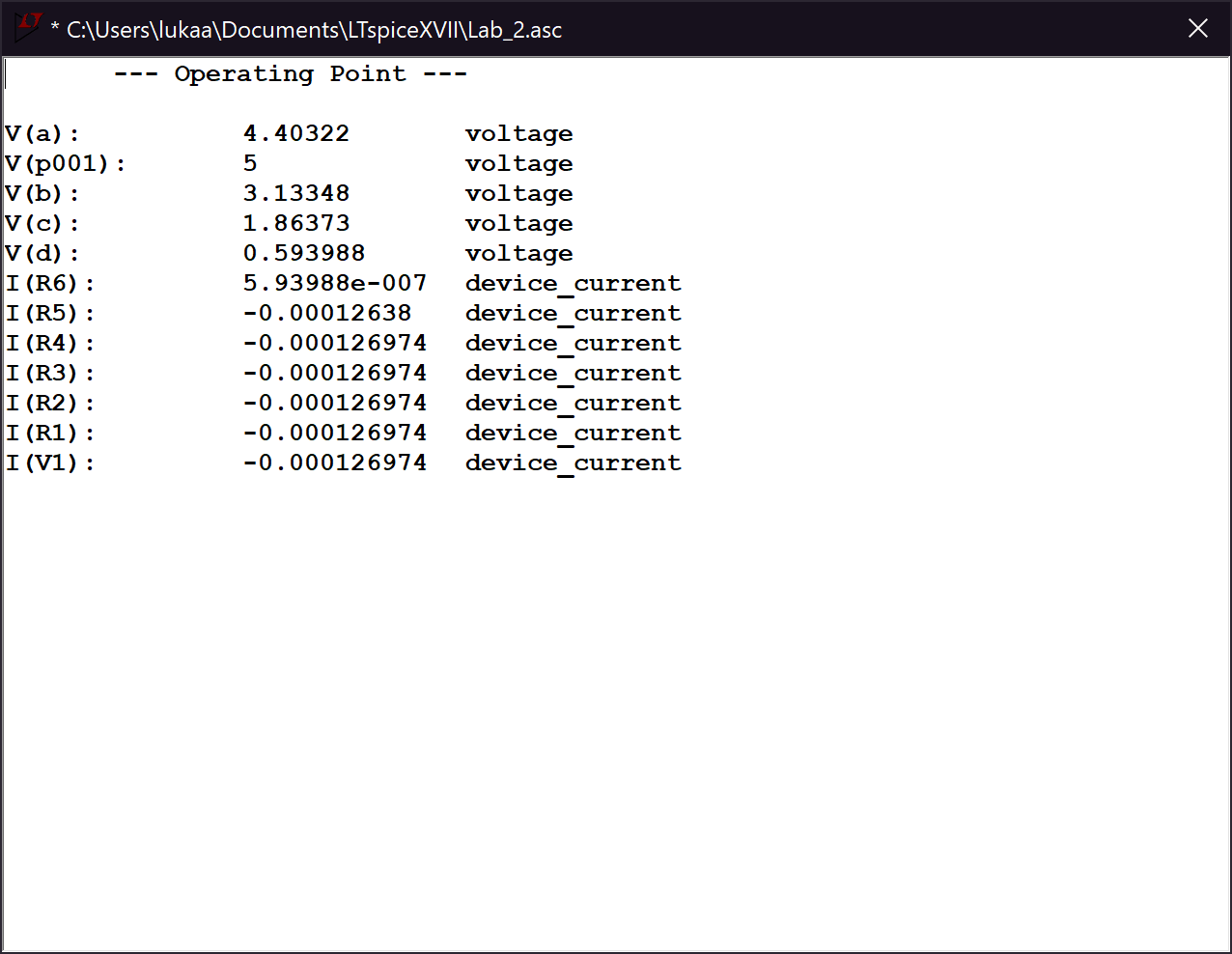
b)



c)

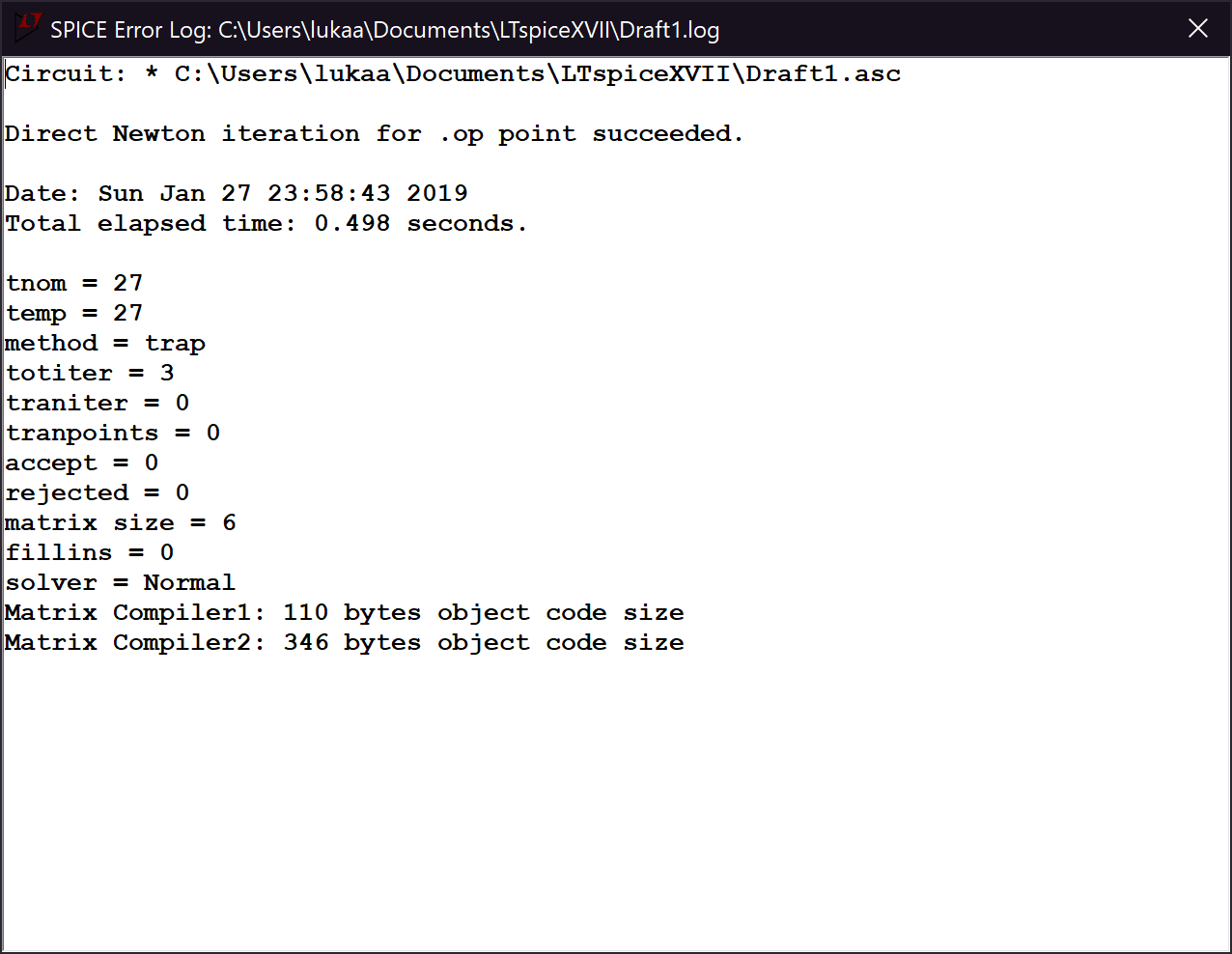


d)

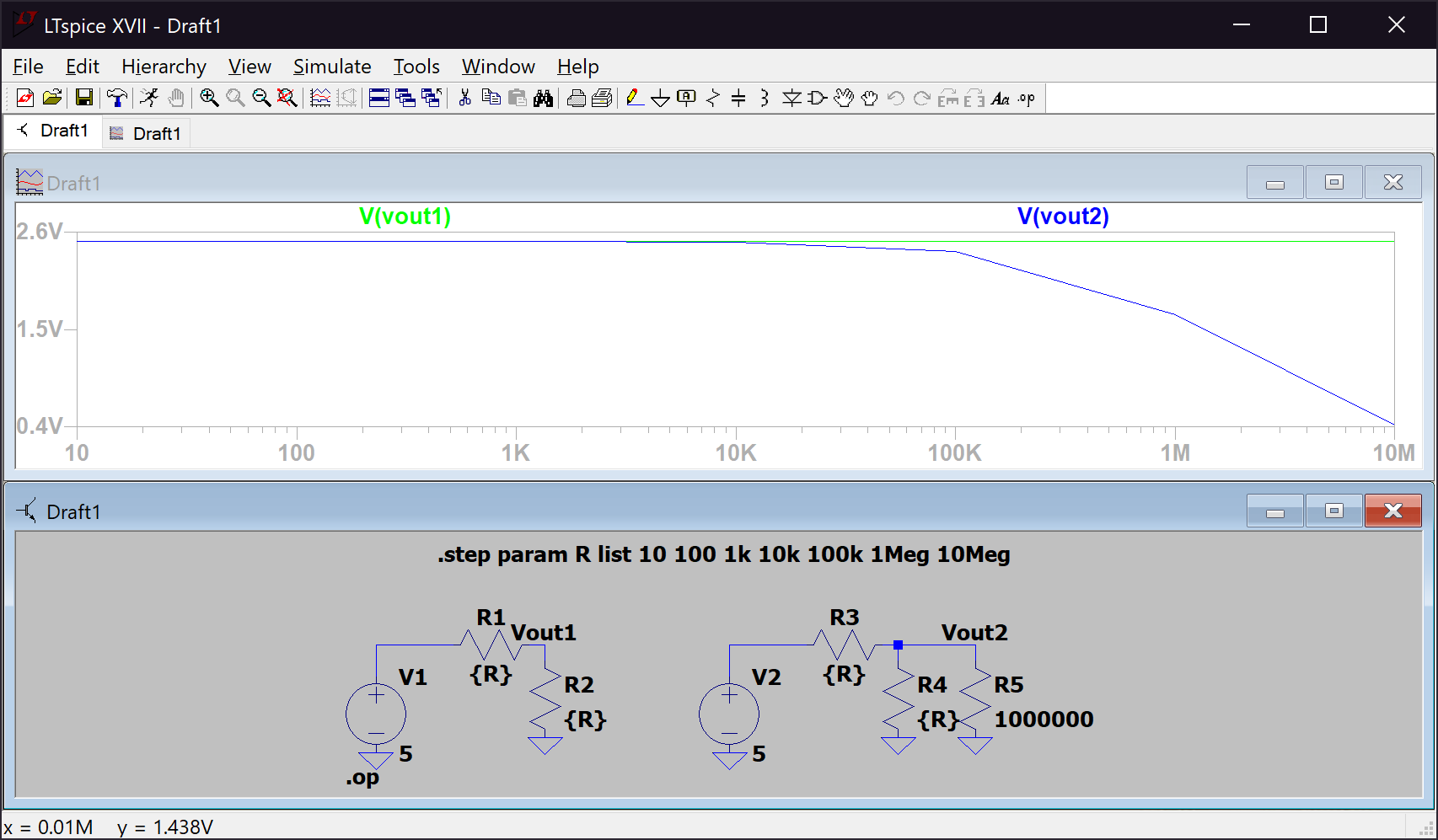


2.4.2 LTspice Variables

Error Log

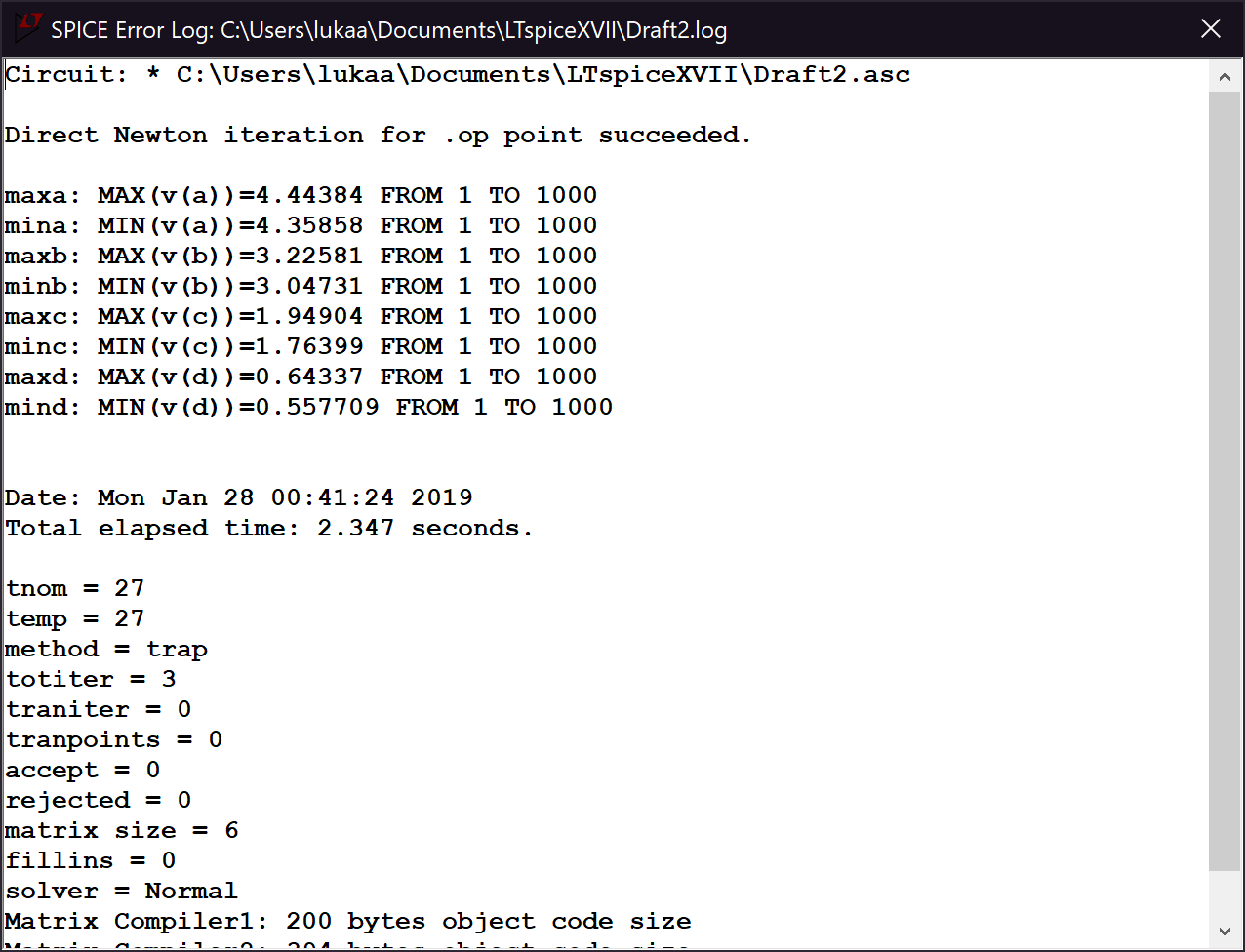


Simulation

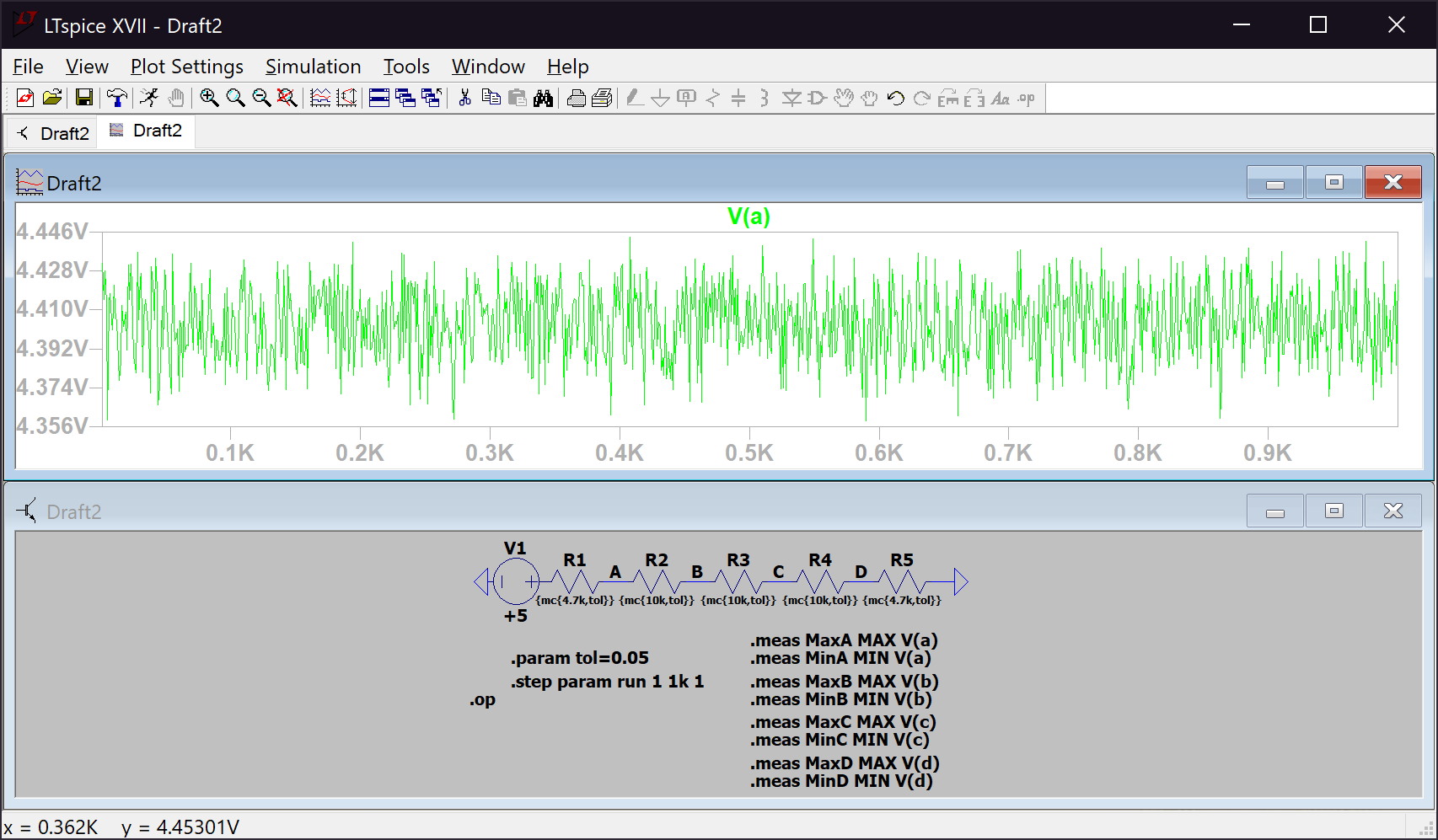


2.4.3 Monte Carlo Simulations

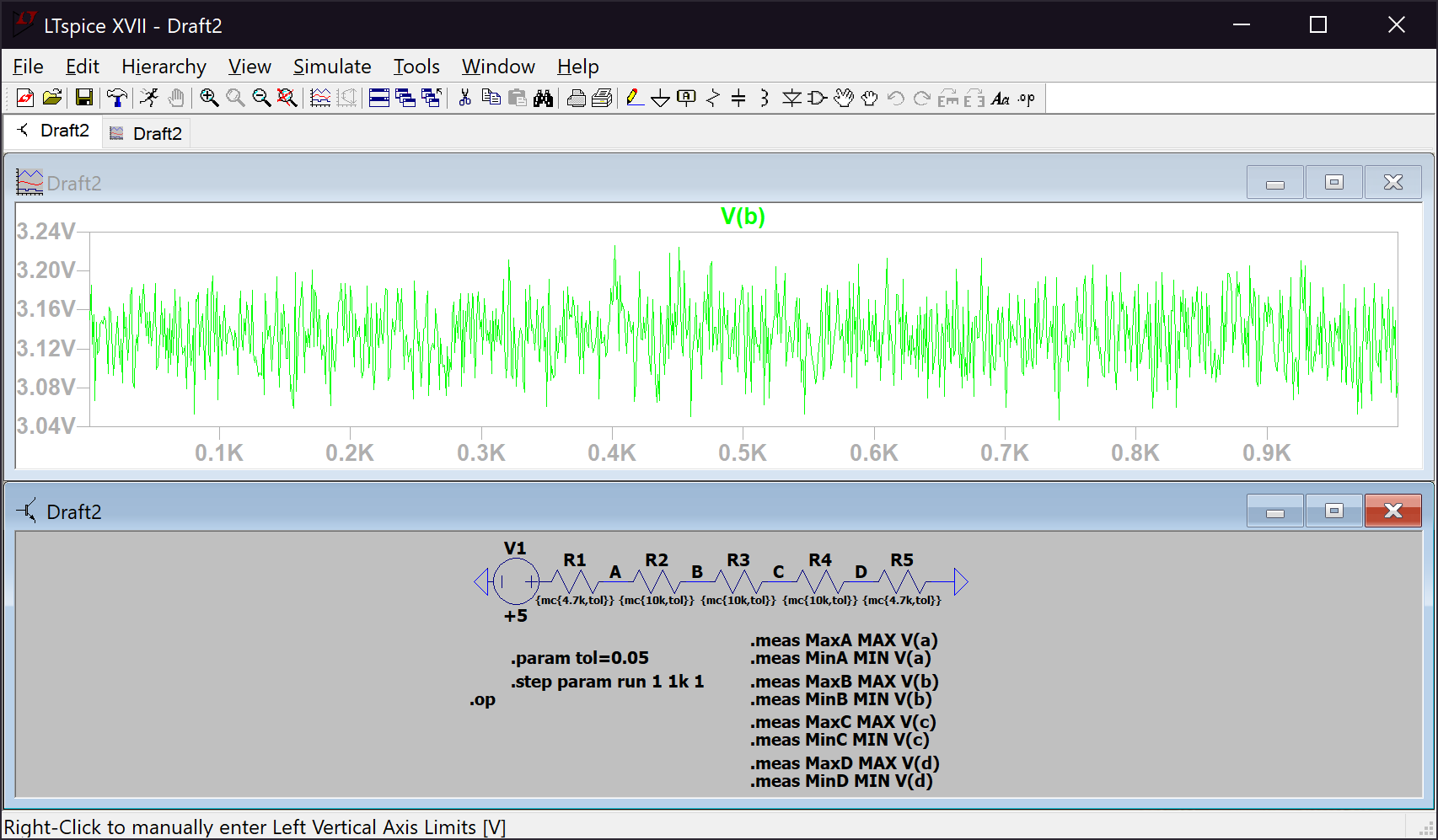
Error Log



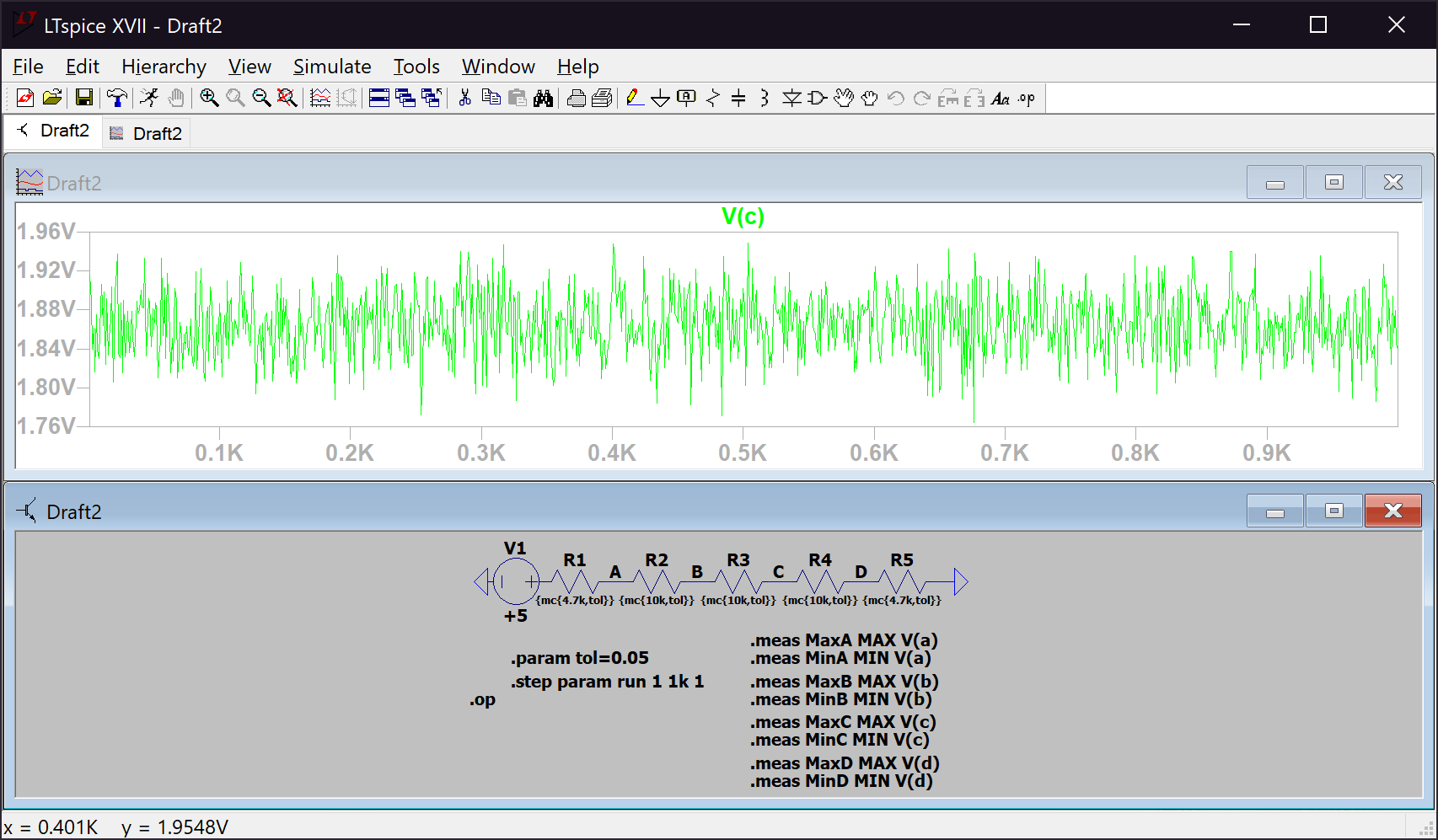
Node A



Node B



Node C



Node D

