389-596

Rockwell

R65C21
PERIPHERAL INTERFACE ADAPTER (PIA)

PRELIMINARY

DESCRIPTION

The R65C21 Peripheral Interface Adapter (PIA) is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the R6500, R6500/* or R65C00 family of microprocessors, the R65C21 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or to "handshake" data between the processor and a peripheral device.

FEATURES

- Low power CMOS N-well silicon gate technology
- Direct replacement for NMOS R6520 or MC6821 PIA
- Two 8-bit bidirectional I/O ports with individual data direction control
- Automatic "Handshake" control of data transfers
- Two interrupts (one for each port) with program control
- 1, 2, 3, and 4 MHz versions
- Commercial and industrial temperature range versions
- 40-pin plastic and ceramic versions
- 5 volt ±5% supply requirements
- Compatible with the R6500, R6500/* and R65C00 family of microprocessors

ORDERING INFORMATION

The R65C21 is available in both a ceramic and a plastic 40-pin package, a commercial or industrial operating temperature range and operating frequencies of 1, 2, 3, or 4 MHz. These versions are coded into the part number as follows:

Part Number:
R65C21___

- Temperature Range (T_L to T_H):
  - Blank = 0°C to +70°C
  - E = −40°C to +85°C
- Frequency Range
  - 1 = 1 MHz
  - 2 = 2 MHz
  - 3 = 3 MHz
  - 4 = 4 MHz
- Package
  - C = Ceramic
  - P = Plastic

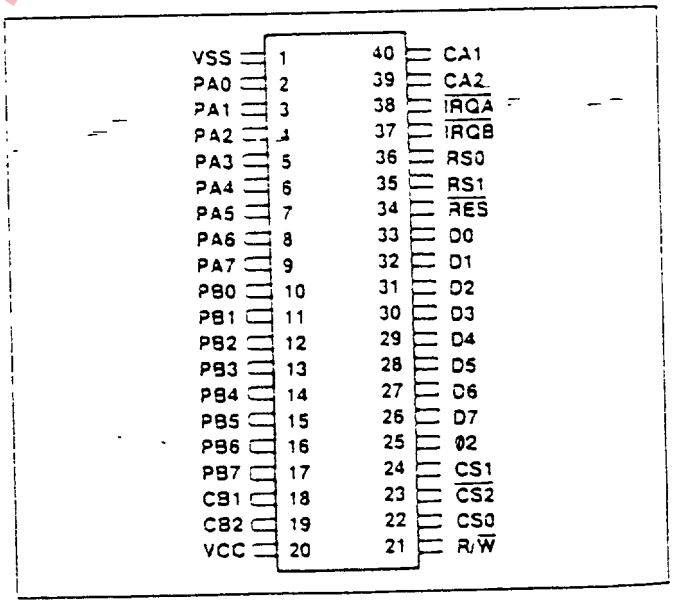


Figure 1. R65C21 Pin Configuration

FUNCTIONAL DESCRIPTION

The R65C21 PIA is organized into two independent sections referred to as the A Side and the B Side. Each section consists of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control (ISCA, ISCB) and the buffers necessary to drive the Peripheral Interface buses. Data Bus Buffers (DBB) interface data from the two sections to the data bus while the Data Input Register (DIR) interfaces data from the DBB to the PIA registers. Chip Select and R/$\overline{W}$ control circuitry interface to the processor bus control lines. Figure 2 is a block diagram of the R65C21 PIA.

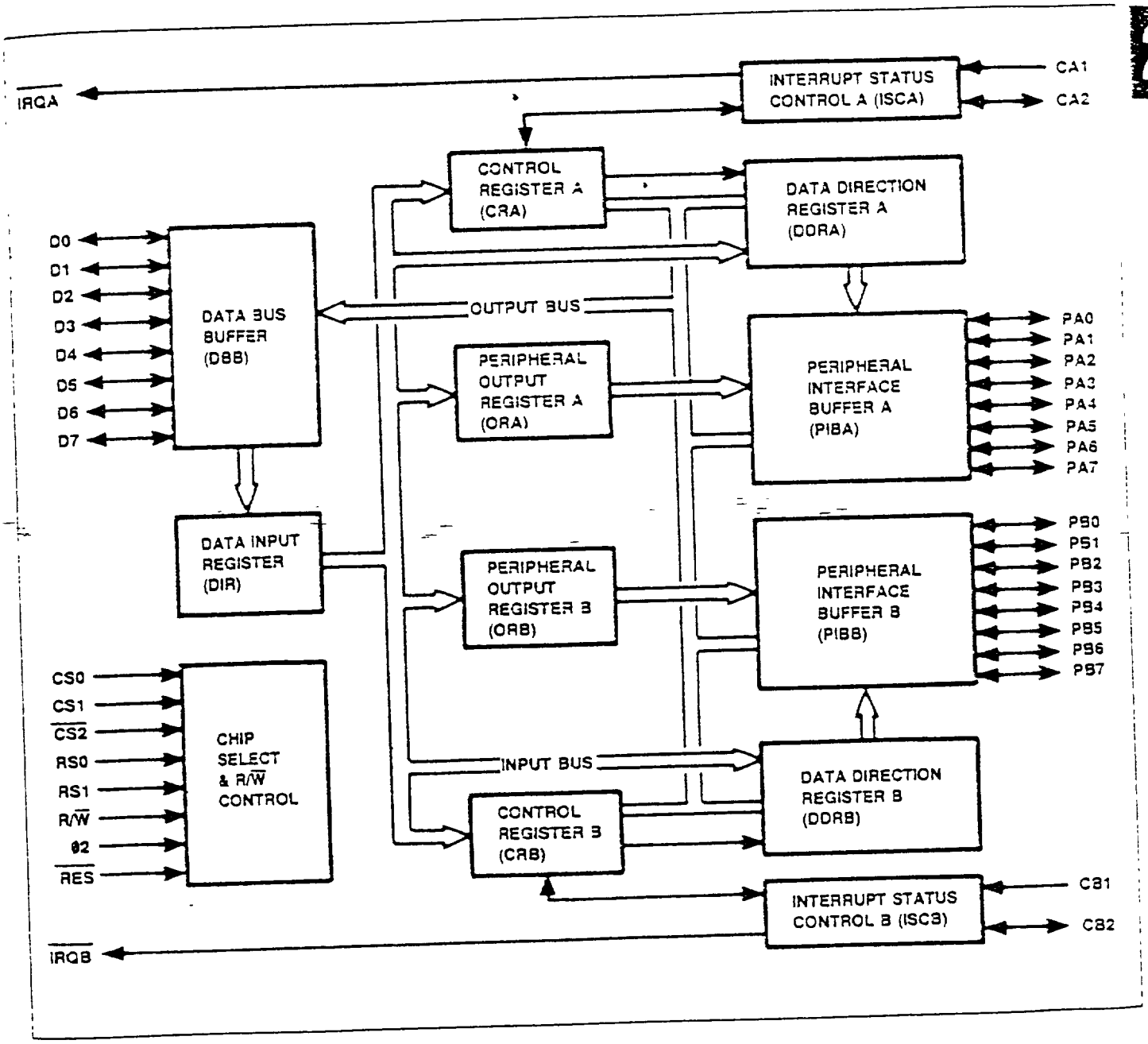


Figure 2. R65C21 PIA Block Diagram

DATA INPUT REGISTER (DIR)

When the microprocessor writes data into the PIA, the data which appears on the data bus during the Ø2 clock pulse is latched into the Data Input Register (DIR). The data is then transferred into one of six internal registers of the PIA after the trailing edge of the Ø2 clock. This assures that the data on the peripheral output lines will make smooth transitions from high to low (or from low to high) and the voltage will remain stable except when it is going to the opposite polarity.

CONTROL REGISTERS (CRA AND CRB)

Table 1 illustrates the bit designation and functions in the two control registers. The control registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) in each control register indicate the status of the Interrupt Input lines (CA1, CA2, CB1, CB2). These Interrupt Status bits (IRQA1, IRQA2 or IRQB1, IRQB2) are normally interrogated by the microprocessor during the $\overline{IRQ}$ interrupt service routine to determine the source of the interrupt.

DATA DIRECTION REGISTERS (DDRA, DDRB)

The Data Direction Registers (DDRA, DDRB) allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Writing a "0" in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a "1" causes it to act as an output.

Bit 2 (DDRA, DDRB) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a "1," a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a "0," a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, RS1) selects the various internal registers as shown in Table 2.

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

PERIPHERAL OUTPUT REGISTERS (ORA, ORB)

The Peripheral Output Registers (ORA, ORB) store the output data from the Data Bus Buffers (DBB) which appears on the Peripheral I/O port. If a line on the Peripheral A Port is programmed as an output by the DDRA, writing a 0 into the corresponding bit in the ORA causes that line to go low (<0.4 V), writing a 1 causes the line to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

INTERRUPT STATUS CONTROL (ISCA, ISCB)

The four interrupt peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register and detects active transitions on the interrupt inputs.

PERIPHERAL I/O PORTS (PA0-PA7, PB0-PB7)

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on the peripheral device by writing data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a 1 in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A 0 in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-up devices. These pull-up devices are resistive in nature and therefore allow the output voltage to go to VCC for a logic 1. The switches can sink a full 3.2 mA, making these buffers capable of driving two standard TTL loads.

In the input mode, the pull-up devices are still connected to the I/O pin and still supply current to this pin. For this reason, these lines also represent two standard TTL loads in the input mode.

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an output is similar to the Peripheral A port, as is the effect of reading or writing this port. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

Table 1. Control Registers Bit Designations

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
	7	6	5	4	3	2	1	0
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

The Peripheral B I/O port buffers are push-pull devices (i.e., the pull-up devices are switched OFF in the 0 state and ON for a logic 1. Since these pull-ups are active devices, the logic 1 voltage will not go higher than −2.4V.

Another difference between the PA0-PA7 lines and the PB0 through PB7 lines is that they have three-state capability which allows them to enter a high impedance state when programmed to be used as input lines. In addition, data on these lines will be read properly, when programmed as output lines, even if the data signals fall below 2.0 volts for a "high" state or are above 0.8 volts for a "low" state. When programmed as output, each line can drive at least a two TTL load and may also be used as a source of up to 3.2 milliamperes at 1.5 volts to directly drive the base of a transistor switch, such as a Darlington pair.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic is the high-impedance input state which is a function of the Peripheral B push-pull buffers. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

DATA BUS BUFFERS (D0-D7)

The Data Bus Buffers are 8-bit bidirectional buffers used for data exchange, on the D0-D7 Data Bus, between the microprocessor and the PIA. These buffers are tri-state and are capable of driving a two TTL load (when operating in an output mode) and represent a one TTL load to the microprocessor (when operating in an input mode).

INTERFACE SIGNALS

The PIA interfaces to the R6500, R6500/*, or the R65C00 microprocessor family with a reset line, a Ø2 clock line, a read/write line, two interrupt request lines, two register select lines, three chip select lines, and an 8-bit bidirectional data bus.

The PIA interfaces to the peripheral devices with four interrupt/control lines and two 8-bit bidirectional data buses.

Figure 1 (on the front page) shows the pin assignments for these interface signals and Figure 3 shows the interface relationship of these signal as they pertain to the CPU and the peripheral devices.

CHIP SELECT (CS0, CS1, $\overline{CS2}$)

The PIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. These three chip select lines are normally connected to the processor address lines either directly or through external decoder circuits. When the PIA is selected, data will be transferred between the data lines and PIA registers, and/or peripheral interface lines as determined by the R/$\overline{W}$, RS0, and RS1 lines and the contents of Control Registers A and B.

RESET SIGNAL ($\overline{RES}$)

The Reset ($\overline{RES}$) input initializes the R65C21 PIA. A low signal on the $\overline{RES}$ input causes all internal registers to be cleared.

CLOCK SIGNAL (Ø2)

The Phase 2 Clock Signal (Ø2) is the system clock that triggers all data transfers between the CPU and the PIA. Ø2 is generated by the CPU and is therefore the synchronizing signal between the CPU and the PIA.

READ/WRITE SIGNAL (R/$\overline{W}$)

Read/Write (R/$\overline{W}$) controls the direction of data transfers between the PIA and the data lines associated with the CPU and the peripheral devices. A high on the R/$\overline{W}$ line permits the peripheral devices to transfer data to the CPU from the PIA. A low on the R/$\overline{W}$ line allows data to be transfered from the CPU to the peripheral devices from the PIA.

REGISTER SELECT (RS0, RS1)

The two Register Select lines (RS0, RS1), in conjunction with the Control Registers (CRA, CRB) Data Direction Register access bits (see Table 1, bit 2) select the various R65C21 registers to be accessed by the CPU. RS0 and RS1 are normally connected to the microprocessor (CPU) address output lines. Through control of these lines, the CPU can write directly into the Control

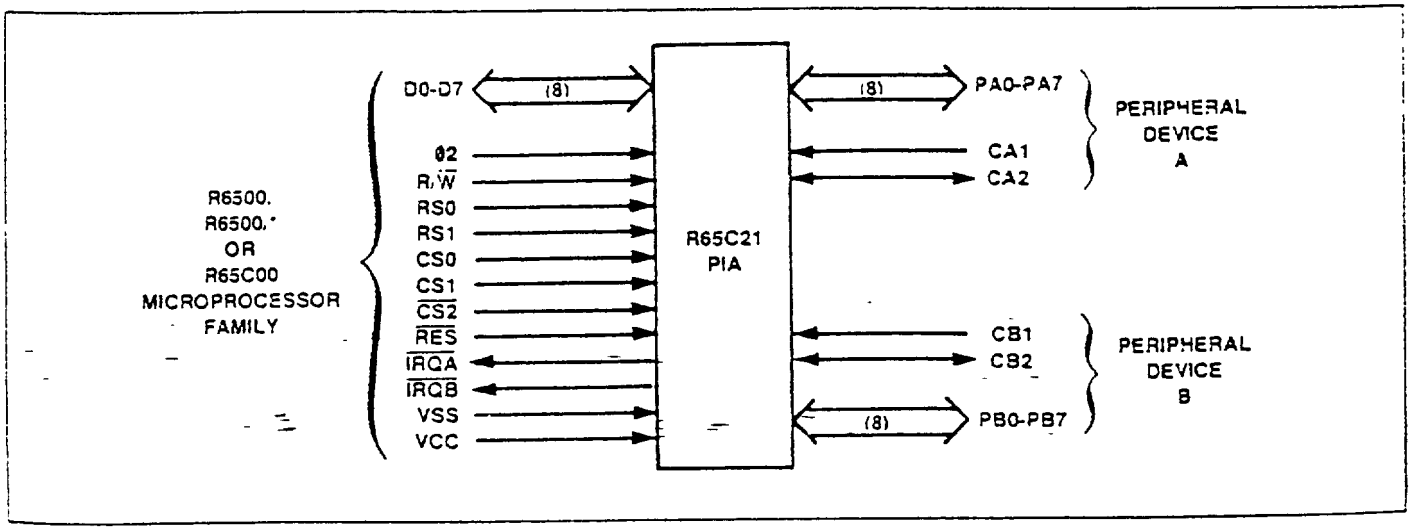


Figure 3. Interface Signals Relationship

Registers (CRA, CRB) the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and therefore are shown separately in Table 2.

Table 2. ORA and ORB Register Addressing

Register Address (Hex)	Register Select Lines		Data Direction Control		Register Operation	
	RS1	RS0	CRA (Bit 2)	CRB (Bit 2)	R/$\overline{W}$=H	R/$\overline{W}$=L
0	L	L	1	—	Read PIEA	Write ORA
0	L	L	0	—	Read DDRA	Write DDRA
1	L	H	—	—	Read CRA	Write CRA
2	H	L	—	1	Read PIEB	Write ORB
2	H	L	—	0	Read DDRB	Write DDRB
3	H	H	—	—	Read CRB	Write CRB

INTERRUPT REQUEST LINES ($\overline{IRQA}$, $\overline{IRQB}$)

The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the microprocessor either directly or through external interrupt priority circuitry. These lines are open drain and are capable of sinking 1.6 milliamps from an external source. This permits all interrupt request lines to be tied together in a wired-OR configuration. The A and B in the titles of these lines correspond to the peripheral port A and the peripheral port B so that each interrupt request line services one peripheral data port.

Each Interrupt Request line has two interrupt flag bits which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers (CRA, CRB). These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2). The four interrupt flags are set (enabled) by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

CRA bit 7 (IRQA1) is always set by an active transition of the CA1 interrupt input signal. However, $\overline{IRQA}$ can be disabled by setting bit 0 in CRA to a 0. Likewise, CRA bit 6 (IRQA2) can be set by an active transition of the CA2 interrupt input signal and $\overline{IRQA}$ can be disabled by setting bit 3 in CRA to a 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the read/write, proper data direction register and register select signals are provided to allow the processor to read the Peripheral A I/O port. A summary of $\overline{IRQA}$ control is shown in Table 3.

Control of $\overline{IRQB}$ is performed in exactly the same manner as that described above for $\overline{IRQA}$. Bit 7 in CRB (IRQB1) is set by an active transition on CB1 and $\overline{IRQB}$ from this flag is controlled by CRB bit 0. Likewise bit 6 (IRQB2) in CRB is set by an active transition on CB2, and $\overline{IRQB}$ from this flag is controlled by CRB bit 3.

Also both bit 6 and bit 7 of CRB are reset by a "Read Peripheral B Output Register" operation. A summary of $\overline{IRQB}$ control is shown in Table 3.

Table 3. $\overline{IRQA}$ and $\overline{IRQB}$ Control Summary

Control Register Bits	Action
CRA-7=1 and CRA-0=1	$\overline{IRQA}$ goes low (Active)
CRA-6=1 and CRA-3=1	$\overline{IRQA}$ goes low (Active)
CRB-7=1 and CRB-0=1	$\overline{IRQB}$ goes low (Active)
CRB-6=1 and CRB-3=1	$\overline{IRQB}$ goes low (Active)

Note

The flags act as the link between the peripheral interrupt signals and the processor interrupt inputs. The interrupt disable bits allow the processor to control the interrupt function.

INTERRUPT INPUT/PERIPHERAL CONTROL LINES (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 4 summarizes the operation of these control lines.

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a "0" in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a "1" if it is to be set on a positive transition.

NOTE:

A negative transition is defined as a transition from a high to a low, and a positive transition is defined as a transition from a low to a high voltage.

CA2 can act as a totally independent interrupt or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupt.

In the output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a 0 and CRA, bit 3 to a 1. This pulse output can be used to control the counters, shift registers, etc., which make sequential data available on the Peripheral input lines.

CONTROL REGISTER A (CRA)

CA2 INPUT MODE (BIT 5 = 0)

7	6	5	4	3	2	1	0
IRQA1 FLAG	IRQA2 FLAG	CA2 INPUT MODE SELECT (=0)	IRQA2 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA2	DRA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			IRQA2 CONTROL			$\overline{\text{IRQA}}$ IRQA1 CONTROL	

CA2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQA1 FLAG	0	CA2 OUTPUT MODE SELECT (=1)	CA2 OUTPUT CONTROL	CA2 RESTORE CONTROL	DRA SELECT	IRQA1 POSITIVE TRANSITION	$\overline{\text{IRQA}}$ ENABLE FOR IRQA1
			CA2 CONTROL			$\overline{\text{IRQA}}$ IRQA1 CONTROL	

CA2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7 IRQA1 FLAG
1 A transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria. This bit is cleared by a read of Output Register A or by $\overline{\text{RES}}$.
0 No transition has occurred on CA1 that satisfies the bit 1 IRQA1 transition polarity criteria.

Bit 2 OUTPUT REGISTER A SELECT
1 Select Output Register A.
0 Select Data Direction Register A.

Bit 1 IRQA1 POSITIVE TRANSITION
1 Set IRQA1 Flag (bit 7) on a positive (low-to-high) transition of CA1.
0 Set IRQA1 Flag (bit 7) on a negative (high-to-low) transition of CA1.

Bit 0 $\overline{\text{IRQA}}$ ENABLE FOR IRQA1
1 Enable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.
0 Disable assertion of $\overline{\text{IRQA}}$ when IRQA1 Flag (bit 7) is set.

CA2 INPUT MODE (BIT 5 = 0)

Bit 6 IRQA2 FLAG
1 A transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria. This flag is cleared by a read of Output Register A or by $\overline{\text{RES}}$.
0 No transition has occurred on CA2 that satisfies the bit 4 IRQA2 transition polarity criteria.

Bit 5 CA2 MODE SELECT
0 Select CA2 Input Mode

Bit 4 IRQA2 POSITIVE TRANSITION
1 Set IRQA2 Flag (bit 6) on a positive (low-to-high) transition of CA2.
0 Set IRQA2 Flag (bit 6) on a negative (high-to-low) transition of CA2.

Bit 3 $\overline{\text{IRQA}}$ ENABLE FOR IRQA2
1 Enable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.
0 Disable assertion of $\overline{\text{IRQA}}$ when IRQA2 Flag (bit 6) is set.

CA2 OUTPUT MODE (BIT 5 = 1)

Bit 6 NOT USED
0 Always zero.

Bit 5 CA2 MODE SELECT
1 Select CA2 Output Mode.

Bit 4 CA2 OUTPUT CONTROL
1 CA2 goes low when a zero is written into CRA bit 3. CA2 goes high when a one is written into CRA bit 3.
0 CA2 goes low on the first negative (high-to-low) Ø2 clock transition following a read of Output Register A. CA2 returns high as specified by bit 3.

Bit 3 CA2 READ STROBE RESTORE CONTROL (4 = 0)
1 CA2 returns high on the next Ø2 clock negative transition following a read of Output Register A.
0 CA2 returns high on the next active CA1 transition following a read of Output Register A as specified by bit 1.

Figure 4. Control Line Operations Summary (1 of 2)

CONTROL REGISTER B (CRB)

CB2 INPUT MODE (BIT 5 = 0)

7	6	5	4	3	2	1	0
IRQB1 FLAG	IRQB2 FLAG	CB2 INPUT MODE SELECT (=0)	IRQB2 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB2	CRB SELECT	IRQB1 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			$\overline{\text{IRQB}}$ IRQB2 CONTROL			$\overline{\text{IRQB}}$ IRQB1 CONTROL	

CB2 OUTPUT MODE (BIT 5 = 1)

7	6	5	4	3	2	1	0
IRQB1 FLAG	0	CB2 OUTPUT MODE SELECT (=1)	CB2 OUTPUT CONTROL	CB2 RESTORE CONTROL	CRB SELECT	IRQB1 POSITIVE TRANSITION	$\overline{\text{IRQB}}$ ENABLE FOR IRQB1
			CB2 CONTROL			$\overline{\text{IRQB}}$ IRQB1 CONTROL	

CB2 INPUT OR OUTPUT MODE (BIT 5 = 0 or 1)

Bit 7 IRQB1 FLAG
1 A transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria. This bit is cleared by a read of Output Register B or by $\overline{\text{RES}}$.
0 No transition has occurred on CB1 that satisfies the bit 1 IRQB1 transition polarity criteria.

Bit 2 OUTPUT REGISTER B SELECT
1 Select Output Register B.
0 Select Data Direction Register B

Bit 1 IRQB1 POSITIVE TRANSITION
1 Set IRQB1 Flag (bit 7) on a positive (low-to-high) transition of CB1
0 Set IRQB1 Flag (bit 7) on a negative (high-to-low) transition of CB1

Bit 0 $\overline{\text{IRQB}}$ ENABLE FOR IRQB1
1 Enable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set.
0 Disable assertion of $\overline{\text{IRQB}}$ when IRQB1 Flag (bit 7) is set.

CB2 INPUT MODE (BIT 5 = 0)

Bit 6 IRQB2 FLAG
1 A transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria. This flag is cleared by a read of Output Register B or by $\overline{\text{RES}}$.
0 No transition has occurred on CB2 that satisfies the bit 4 IRQB2 transition polarity criteria.

Bit 5 CB2 MODE SELECT
0 Select CB2 Input Mode.

Bit 4 IRQB2 POSITIVE TRANSITION
1 Set IRQB2 Flag (bit 6) on a positive (low-to-high) transition of CB2.
0 Set IRQB2 Flag (bit 6) on a negative (high-to-low) transition of CB2.

Bit 3 $\overline{\text{IRQB}}$ ENABLE FOR IRQB2
1 Enable assertion of $\overline{\text{IRQB}}$ when IRQB2 Flag (bit 6) is set.
0 Disable assertion of $\overline{\text{IRQB}}$ when IRQB2 Flag (bit 6) is set.

CB2 OUTPUT MODE (BIT 5 = 1)

Bit 6 NOT USED
0 Always zero.

Bit 5 CB2 MODE SELECT
1 Select CB2 Output Mode.

Bit 4 CB2 OUTPUT CONTROL
1 CB2 goes low when a zero is written into CRB bit 3. CB2 goes high when a one is written into CRB bit 3.
0 CB2 goes low on the first negative (high-to-low) Ø2 clock transition following a write to Output Register B CB2 returns high as specified by bit 3.

Bit 3 CB2 WRITE STROBE RESTORE CONTROL (BIT 4 = 0)
1 CB2 returns high on the next Ø2 clock negative transition following a write to Output Register B.
0 CB2 returns high on the next active CB1 transition following a write to Output Register B as specified by bit 1.

Figure 4. Control Line Operations Summary (2 of 2)

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of CRA to a 1 or a 0 respectively.

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

READING THE PERIPHERAL A I/O PORT

Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines to the data bus. In this situation, the data bus will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read by the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a TTL −2.4V DC when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

READING THE PERIPHERAL B I/O PORT

Reading the Peripheral B I/O port yields a combination of input and output data. In a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (CRB) for those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back to the processor on a Read operation.

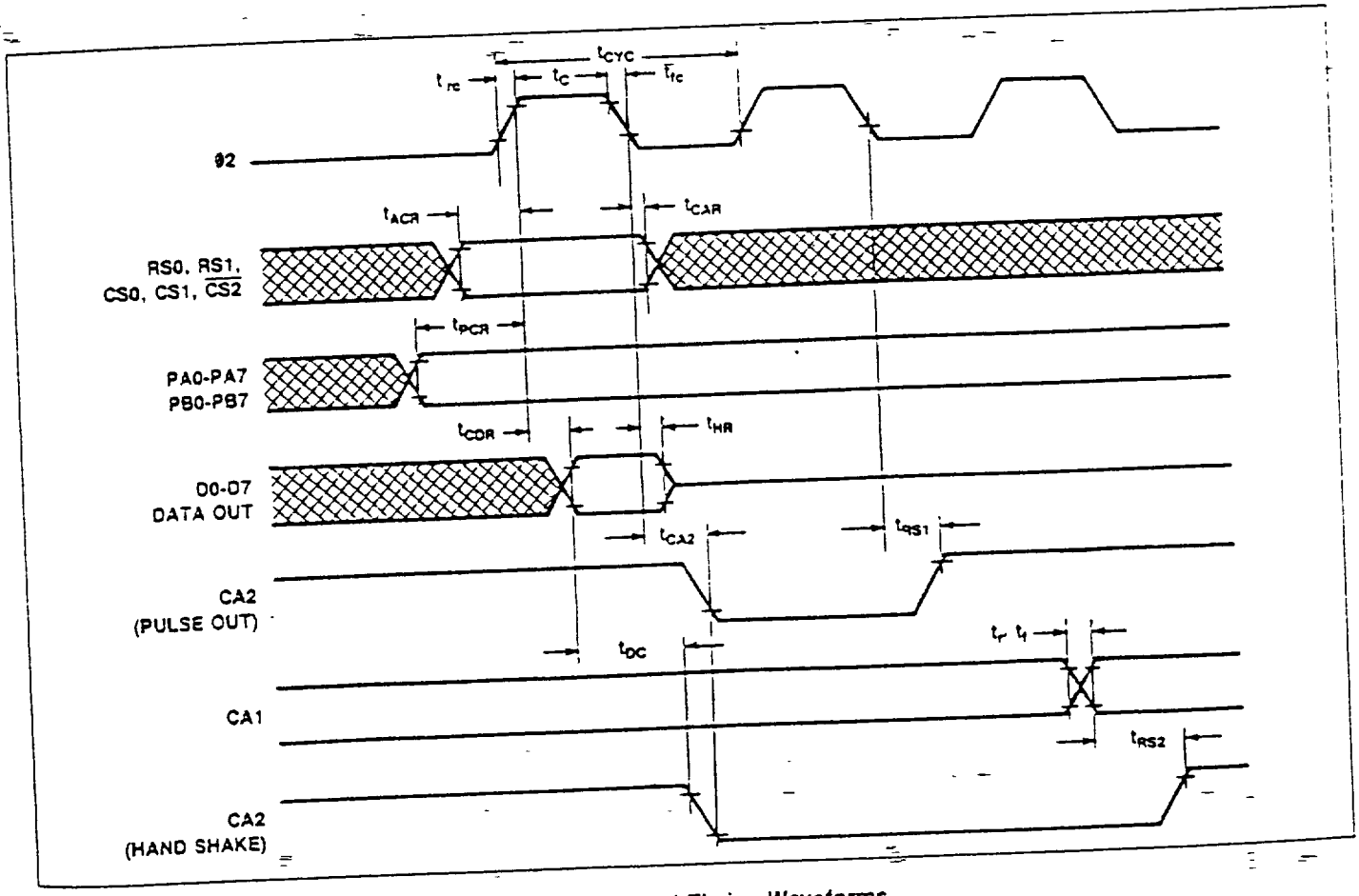


Figure 5. Read Timing Waveforms

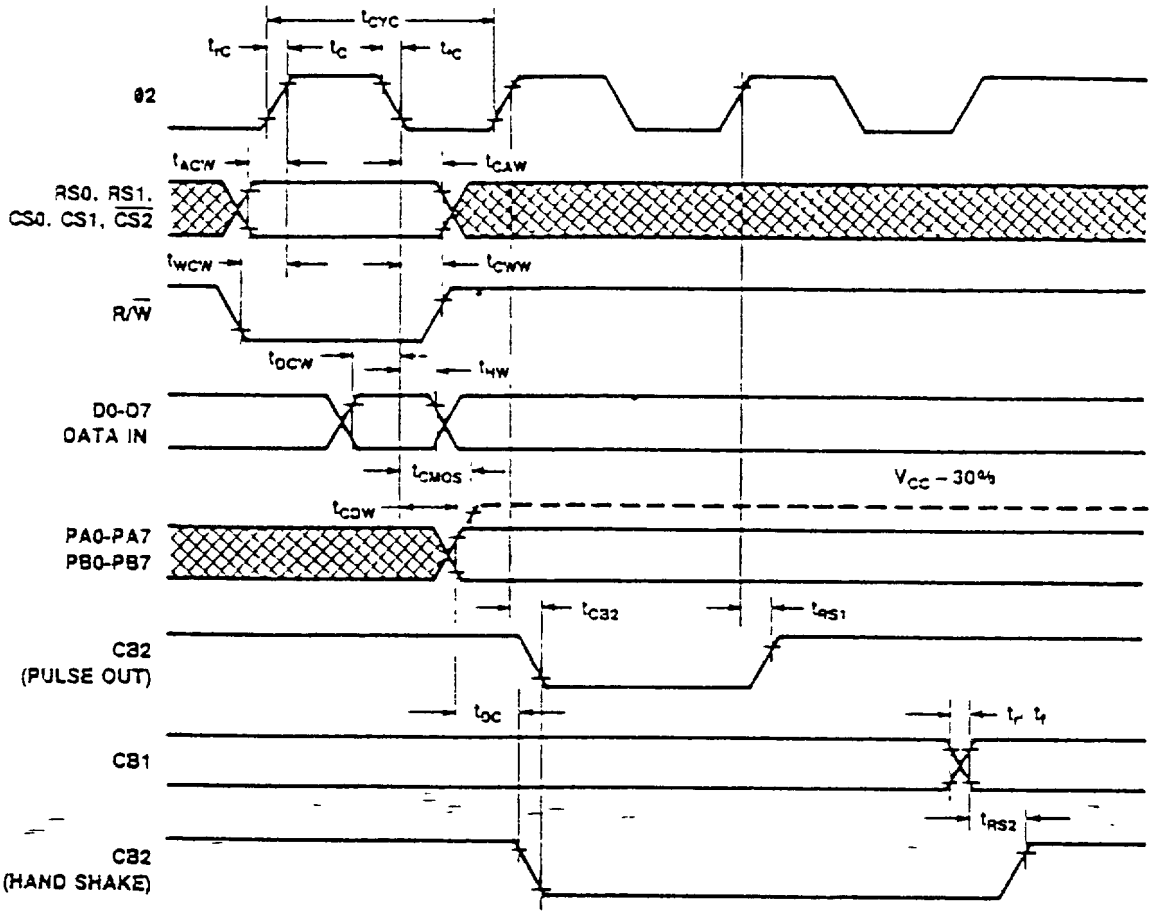


Figure 6. Write Timing Waveforms

BUS TIMING CHARACTERISTICS

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Unit
		Min.	Max.	Min	Max.	Min.	Max.	Min.	Max.	
Φ2 Cycle	t_{CYC}	1 0	—	0 5	—	0 33	—	0 25	—	µs
Φ2 Pulse Width	t_C	450	—	220	—	160	—	110	—	ns
Φ2 Rise and Fall Time	t_{rc}, t_{fc}	—	25	—	15	—	12	—	10	ns

READ TIMING

Address Set-Up Time	t_{ACR}	140	—	70	—	53	—	35	—	ns
Address Hold Time	t_{CAR}	0	—	0	—	0	—	0	—	ns
Peripheral Data Set-Up Time	t_{PCR}	300	—	150	—	110	—	75	—	ns
Data Bus Delay Time	t_{CDR}	—	335	—	145	—	105	—	80	ns
Data Bus Hold Time	t_{HR}	20	—	20	—	20	—	20	—	ns

WRITE TIMING

Address Set-Up Time	t_{ACW}	140	—	70	—	53	—	35	—	ns
Address Hold Time	t_{CAW}	0	—	0	—	0	—	0	—	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	180	—	90	—	67	—	45	—	ns
R/$\overline{W}$ Hold Time	t_{CWW}	0	—	0	—	0	—	0	—	ns
Data Bus Set-Up Time	t_{DCW}	180	—	90	—	67	—	45	—	ns
Data Bus Hold Time	t_{HW}	10	—	10	—	10	—	10	—	ns
Peripheral Data Delay Time	t_{CPW}	—	1 0	—	0.5	—	0 33	—	0.25	µs
Peripheral Data Delay Time to CMOS Level	t_{CMOS}	—	2.0	—	1.0	—	0.7	—	0 5	µs

PERIPHERAL INTERFACE TIMING

Peripheral Data Set-Up	t_{PCR}	300	—	150	—	110	—	75	—	ns
Φ2 Low to CA2 Low Delay	t_{CA2}	—	1.0	—	0.5	—	0.33	—	0 25	µs
Φ2 Low to CA2 High Delay	t_{RS1}	—	1.0	—	0.5	—	0.33	—	0 25	µs
CA1 Active to CA2 High Delay	t_{RS2}	—	2.0	—	1 0	—	0.67	—	0.5	µs
Φ2 High to CB2 Low Delay	t_{CB2}	—	1.0	—	0.5	—	0 33	—	0.25	µs
Peripheral Data Valid to CB2 Low Delay	t_{DC}	0	1 5	0	0.75	0	0.5	0	0.37	µs
Φ2 High to CB2 High Delay	t_{RS1}	—	1 0	—	0.5	—	0.33	—	0.25	µs
CB1 Active to CB2 High Delay	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.5	µs
CA1, CA2, CB1 and CB2 Input Rise and Fall Time	t_r, t_f	—	1.0	—	1 0	—	1.0	—	1 0	µs

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to V_{CC} +0.3	Vdc
Output Voltage	V_{OUT}	-0.3 to V_{CC} +0.3	Vdc
Operating Temperature Range Commercial Industrial	T_A	 0 to +70 -40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V ±5%
Temperature Range Commercial Industrial	T_A	 0°C to 70°C -40°C to +85°C

DC CHARACTERISTICS

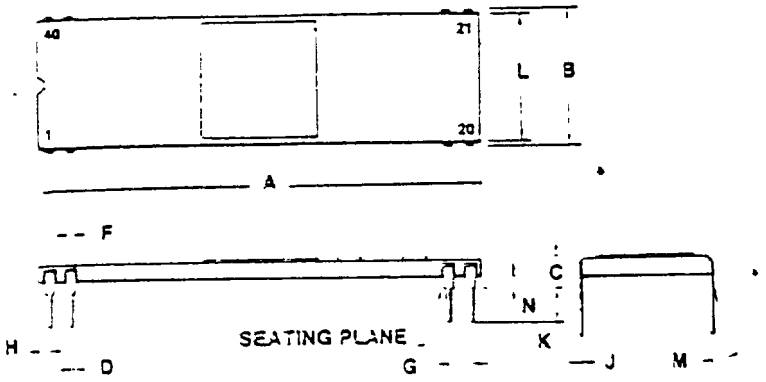
(V_{CC} = 5.0V ±5%, V_{SS} = 0, T_A = T_L to T_H, unless otherwise noted)

Parameter	Symbol	Min.	Typ.[3]	Max.	Unit[2]	Test Conditions
Input High Voltage All except PB0–PB7, $\overline{RES}$ PB0–PB7, $\overline{RES}$	V_{IH}	 +2.0 +2.4	 — —	 V_{CC} V_{CC}	 V V	
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V	
Input Leakage Current R/$\overline{W}$, $\overline{RES}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, Ø2	I_{IN}	—	±1	±2.5	µA	V_{IN} = 0V to V_{CC} V_{CC} = 5.25V
Input Leakage Current for Three-State Off D0–D7, PB0–PB7, CB2	I_{TSI}	—	±2	±10	µA	V_{IN} = 0.4V to 2.4V V_{CC} = 5.25V
Input High Current PA0–PA7, CA2	I_{IH}	-200	-300	—	µA	V_{IH} = 2.4V
Input Low Current PA0–PA7, CA2	I_{IL}	—	-2	-3.2	mA	V_{IL} = 0.4V
Output High Voltage Logic PB0–PB7, CB2 (Darlington Drive)	V_{OH}	 2.4 1.5	 — —	 — —		V_{CC} = 4.75V I_{LOAD} = -200µA I_{LOAD} = -3.2mA
Output Low Voltage PA0–PA7, CA2, PB0–PB7, CB2 D0–D7, $\overline{IRQA}$, $\overline{IRQB}$	V_{OL}	—	—	+0.4	V	V_{CC} = 4.75V I_{LOAD} = 3.2 mA I_{LOAD} = 1.6 mA
Output High Current (Sourcing) Logic PB0–PB7, CB2 (Darlington Drive)	I_{OH}	 -200 -3.2	 -1500 -6	 — —	 µA mA	 V_{OH} = 2.4V V_{OH} = 1.5V
Output Low Current (Sinking) PA0–PA7, PB0–PB7, CB2, CA2 D0–D7, $\overline{IRQA}$, $\overline{IRQB}$	I_{OL}	 3.2 1.6	 — —	 — —	 mA mA	V_{OL} = 0.4V
Output Leakage Current (Off State) $\overline{IRQA}$, $\overline{IRQB}$	I_{OFF}	—	1	±10	µA	V_{OH} = 2.4V V_{CC} = 5.25V
Power Dissipation	P_D		7	10		mW/MHz
Input Capacitance D0–D7, PA0–PA7, PB0–PB7, CA2, CB2 R/$\overline{W}$, $\overline{RES}$, RS0, RS1, CS0, CS1, $\overline{CS2}$ CA1, CB1, Ø2	C_{IN}	 — — —	 — — —	 10 7 20	 pF pF pF	V_{CC} = 5.0V V_{IN} = 0V f = 2 MHz T_A = 25°C
Output Capacitance	C_{OUT}	—	—	10	pF	

Notes:
1. All units are direct current (dc) except capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. Typical values are shown for V_{CC} = 5.0V and T_A = 25°C.

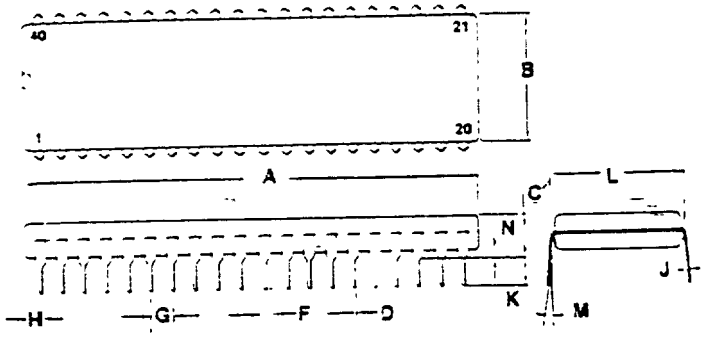
PACKAGE DIMENSIONS

40-PIN CERAMIC DIP



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	1.75	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	0°	10°	0°	10°
N	0.51	1.52	0.020	0.060

40-PIN PLASTIC DIP



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040