INTEGRATED CIRCUITS

DATA SHEET

74F2698-bit bidirectional binary counter

Product specification

1996 Jan 05

IC15 Data Handbook





8-bit bidirectional binary counter

74F269

FEATURES

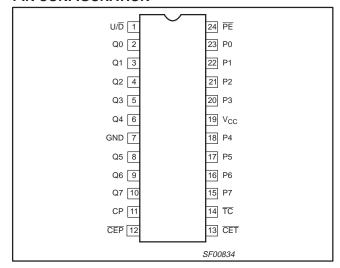
- Synchronous counting and loading
- Built-in look-ahead carry capability
- Count frequency 115MHz typ
- Supply current 95mA typ

DESCRIPTION

The 74F269 is a fully synchronous 8-stage Up/Down Counter featuring a preset capability for programmable operation, carry look-ahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

TYPE	TYPICAL f _{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F269	115MHz	95mA

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V $\pm 10\%$, T_{amb} = 0°C to +70°C	PKG DWG #
24-Pin Plastic Slim DIP (300mil)	N74F269N	SOT222-1
24-Pin Plastic SOL	N74F269D	SOT137-1
24-Pin Plastic SSOP type II	N74F269DB	SOT340-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
P0 - P7	Parallel Data inputs	1.0/1.0	20μA/0.6mA
PE	Parallel Enable input (active Low)	1.0/1.0	20μA/0.6mA
U/D	Up/Down count control input	1.0/1.0	20μA/0.6mA
CEP	Count Enable Parallel input (active Low)	1.0/1.0	20μA/0.6mA
CET	Count Enable Trickle input (active Low)	1.0/1.0	20μA/0.6mA
СР	Clock input	1.0/1.0	20μA/0.6mA
TC	Terminal Count output (active Low)	50/33	1.0mA/20mA
Q0 - Q7	Flip-flop outputs	50/33	1.0mA/20mA

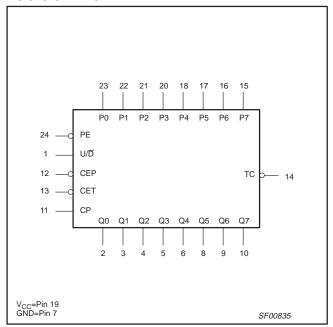
NOTE:

One (1.0) FAST Unit Load is defined as: $20\mu A$ in the High state and 0.6mA in the Low state.

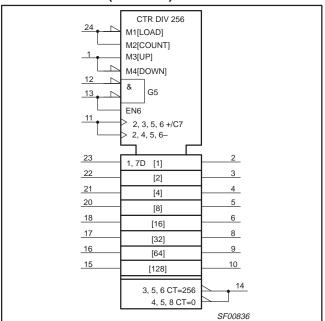
8-bit bidirectional binary counter

74F269

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



APPLICATION

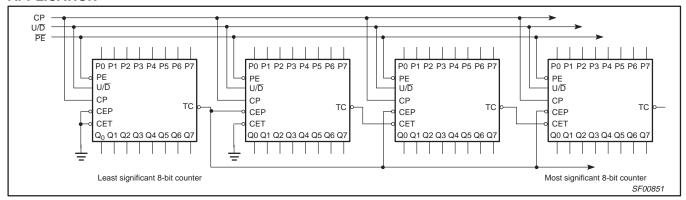


Figure 1. Synchronous Multistage Counting Scheme

MODE SELECT FUNCTION TABLE

		INP	UTS			OUTPUT	S	OPERATING MODE	
СР	CP U/D CEP		CET PE		P _n	Q _n	TC	OPERATING MODE	
1	Х	Х	Х	I	I	L	(a)	Parallel load	
↑	Х	Х	Х	I	h	Н	(a)	i arailei load	
1	h	I	I	h	Х	Count Up	(a)	Count Up	
1	I	I	I	h	Х	Count Down	(a)	Count Down	
1	Х	h	I	h	Х	q _n	(a)	Hold (do nothing)	
1	Х	Х	h	h	Х	q _n	Н	Hold (do nothing)	

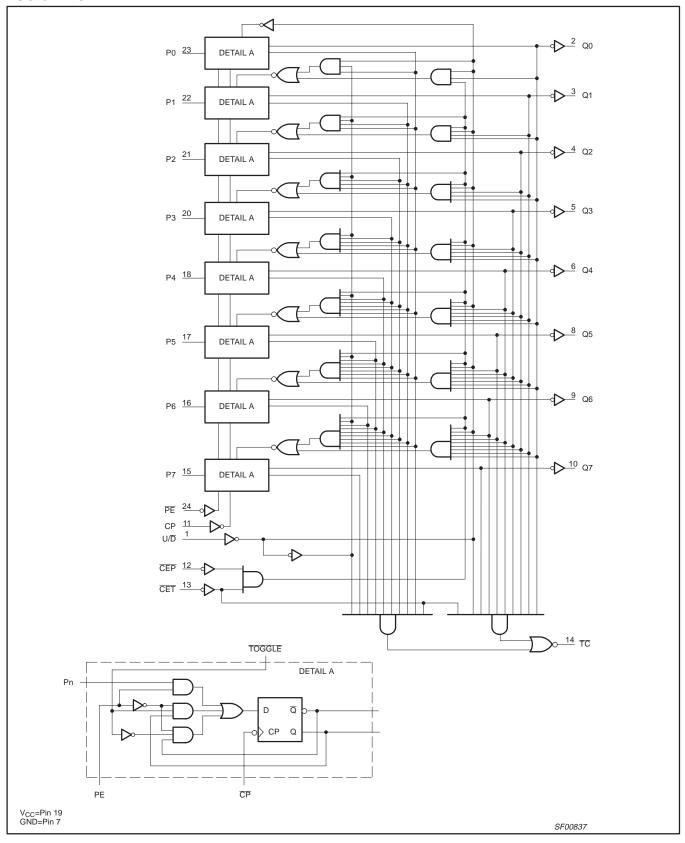
- H = High voltage level
- h = High voltage level one setup prior to the Low-to-High clock transition
- L = Low voltage level
- I = Low voltage level one setup time prior to the Low-to-High clock transition
- q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
- X = Don't care

 ↑ = Low-to-High
- \uparrow = Low-to-High clock transition
- (a) = TC is Low when CET is Low and the counter is at Terminal Count. Terminal Count Up is with all Q_n outputs High and Terminal Count Down is with all Qn outputs Low.

1996 Jan 05 3

74F269

LOGIC DIAGRAM



74F269

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	−0.5 to +7.0	V
I _{IN}	Input current	−30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	−0.5 to V _{CC}	V
I _{OUT}	Current applied to output in Low output state	40	mA
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{stg}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		UNIT			
STWIBUL	PARAMETER	MIN	NOM	MAX	Olviii	
V _{CC}	Supply voltage	4.5	5.0	5.5	V	
V _{IH}	High-level input voltage	2.0			V	
V _{IL}	Low-level input voltage			0.8	V	
I _{IK}	Input clamp current			-18	mA	
I _{OH}	High-level output current			-1	mA	
I _{OL}	Low-level output current			20	mA	
T _{amb}	Operating free-air temperature range	0		70	°C	

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

					LIMITS				
SYMBOL	PARAMETER	TEST	TEST CONDITIONS ^{NO TAG}				MAX	UNIT	
V	Lligh lovel output voltage		V _{CC} = MIN, V	V _{IL} = MAX	±10%V _{CC}	2.5			V
V _{OH}	High-level output voltage	V _{IH} = MIN, I _O	DH = MAX	±5%V _{CC}	2.7	3.4		V	
V	Low-level output voltage			V _{IL} = MAX	±10%V _{CC}		0.30	0.50	V
V _{OL}	Low-level output voltage	V _{IH} = MIN, I _O	DL = MAX	±5%V _{CC}		0.30	0.50	V	
V _{IK}	Input clamp voltage	$V_{CC} = MIN, I_I = I_{IK}$				-0.73	-1.2	V	
I _I	Input current at maximum input vo	oltage	$V_{CC} = MAX, V_I = 7.0V$					100	μΑ
I _{IH}	High-level input current		$V_{CC} = MAX, V_I = 2.7V$					20	μΑ
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.5V					-0.6	mA
I _{OS}	Short-circuit output currentNO TAG	;	$V_{CC} = MAX$	V _{CC} = MAX				-150	mA
		I _{CCH}	V _{CC} =	PE=CET=CEP=U/D=GND, Pn=4.5V, CP=↑			93	120	mA
Icc	Supply current (total)	I _{CCL}	MAX	PE=CET=CEP=U/D=GND, Pn=GND, CP=↑			98	125	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. 2. All typical values are at $V_{CC} = 5V$, $T_{amb} = 25^{\circ}C$.

^{3.} Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

8-bit bidirectional binary counter

74F269

AC ELECTRICAL CHARACTERISTICS

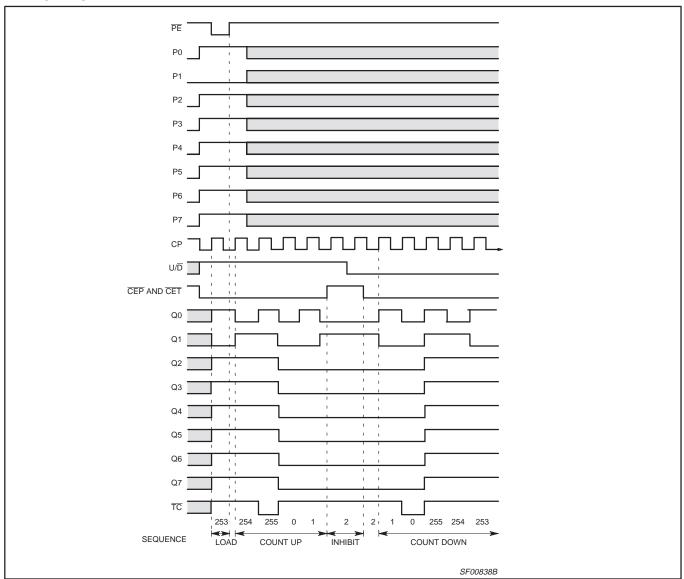
SYMBOL	PARAMETER	TEST CONDITIONS	1	_{imb} = +25° V _{CC} = +5V 50pF, R _L =	'	T _{amb} = 0°C V _{CC} = +5 C _L = 50pF,	UNIT	
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	Waveform 1	100	115		85		MHz
t _{PLH} t _{pPHL}	Propagation delay CP to Q_n (Load, \overline{PE} = Low)	Waveform 1	3.0 4.0	6.0 6.5	8.5 8.5	3.0 4.0	9.0 9.0	ns ns
t _{PLH} t _{PHL}	Propagation delay CP to Q_n (Count, $\overline{PE} = High$)	Waveform 1	3.0 4.5	6.0 7.0	9.0 10.0	3.0 4.0	10.0 10.5	ns ns
t _{PLH} t _{PHL}	Propagation delay CP to TC	Waveform 1	4.5 5.0	6.5 6.5	9.5 9.5	4.0 5.0	10.5 10.0	ns ns
t _{PLH} t _{PHL}	Propagation delay CET to TC	Waveform 2	3.5 3.0	6.0 6.5	9.0 9.0	3.0 3.0	10.0 10.0	ns ns
t _{PLH} t _{PHL}	Propagation delay U/D to TC	Waveform 3	4.5 4.5	7.0 7.0	9.0 9.5	4.0 4.0	10.0 10.0	ns ns

AC SETUP REQUIREMENTS

				LIMITS						
SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC} =	+25°C = +5V R _L = 500Ω	T _{amb} = 0°C V _{CC} = +5 C _L = 50pF,	UNIT				
			MIN	TYP	MIN	MAX				
$t_s(H)$ $t_s(L)$	Setup time, High or Low P _n to CP	Waveform 4	3.5 3.5		2.5 2.5		ns ns			
t _h (H) t _h (L)	Hold time, High or Low P _n to CP	Waveform 4	1.0 1.0		0 1.0		ns ns			
$t_s(H)$ $t_s(L)$	Setup time, High or Low PE to CP	Waveform 4	5.5 6.5		5.5 6.5		ns ns			
t _h (H) t _h (L)	Hold time, High or Low PE to CP	Waveform 4	0 0		0 0		ns ns			
t _s (H) t _s (L)	Setup time, High or Low CEP or CET to CP	Waveform 5	6.0 8.0		5.0 6.5		ns ns			
t _h (H) t _h (L)	Hold time, High or Low CEP or CET to CP	Waveform 5	0 0		0 0		ns ns			
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/D to CP	Waveform 6	8.0 6.5		6.5 6.5		ns ns			
t _h (H) t _h (L)	Hold time, High or Low U/D to CP	Waveform 6	0 0		0 0		ns ns			
t _w (H) t _w (L)	CP Pulse width High or Low	Waveform 1	4.0 4.5		4.0 5.0		ns ns			

74F269

TIMING DIAGRAM



1996 Jan 05 7

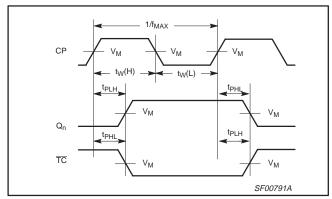
8-bit bidirectional binary counter

74F269

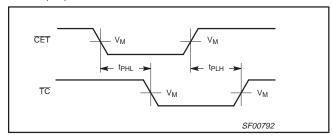
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$.

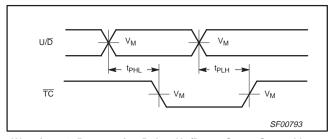
The shaded areas indicate when the input is permitted to change for predictable output performance.



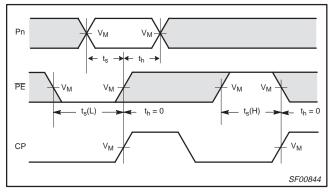
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



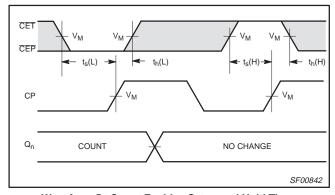
Waveform 2. Propagation Delay, CET Input to Terminal Count Output



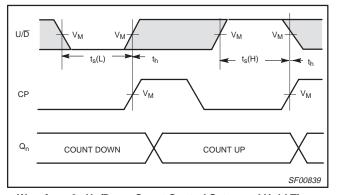
Waveform 3. Propagation Delay, Up/Down Count Control Input to Terminal Count Output



Waveform 4. Parallel Data and Parallel Enable Setup and Hold Times



Waveform 5. Count Enables Setup and Hold Times

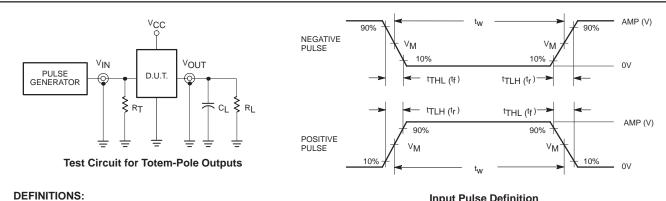


Waveform 6. Up/Down Count Control Setup and Hold Times

8-bit bidirectional binary counter

74F269

TEST CIRCUIT AND WAVEFORMS



R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of

pulse generators.

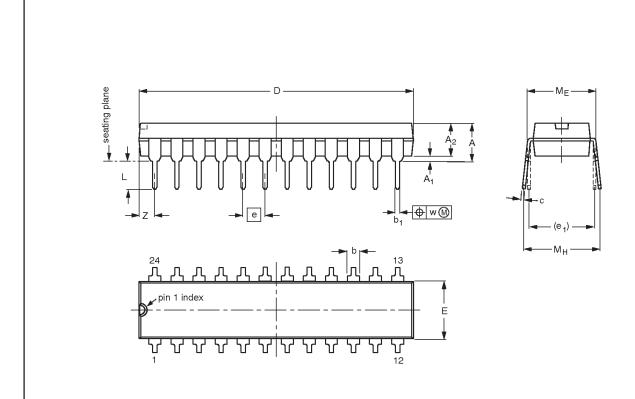
family	INP	INPUT PULSE REQUIREMENTS										
family	amplitude	V_{M}	rep. rate	t _w	t _{TLH}	t _{THL}						
74F	74F 3.0V		1MHz	500ns	2.5ns	2.5ns						

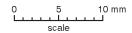
SF00006

74F269

DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ME	Мн	w	Z ⁽¹⁾ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

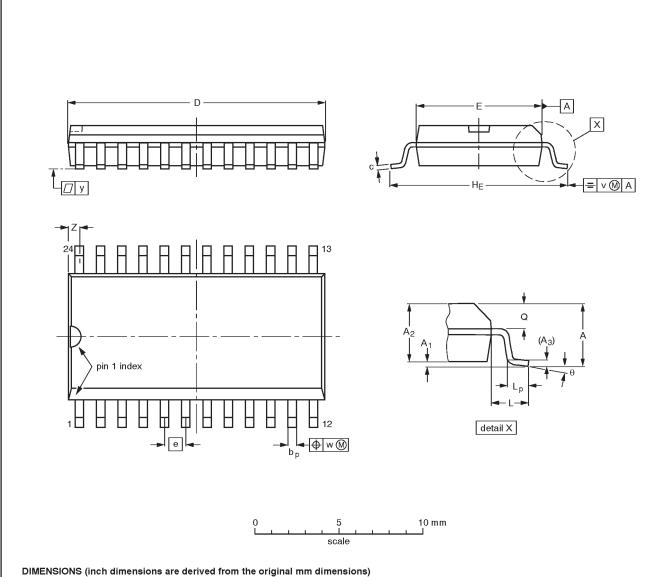
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE		EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	PROJECTION	ISSUE DATE		
SOT222-1		MS-001AF				95-03-11

74F269

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



UNIT	A max.	Α1	A ₂	A ₃	рb	С	D ⁽¹⁾	E ⁽¹⁾	Φ	HE	٦	Lp	Ø	v	w	у	z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0°

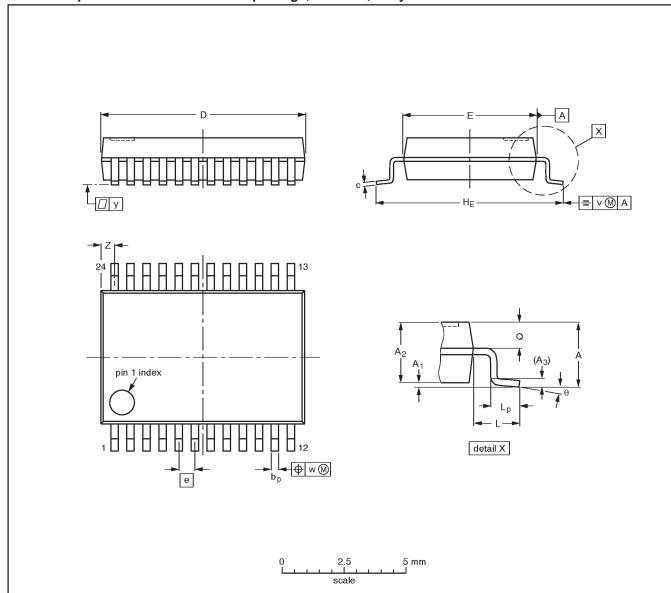
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC		PROJECTION	ISSUE DATE	
SOT137-1	075E05	MS-013AD				-92-11-17 95-01-24

74F269

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	Α1	A ₂	A ₃	bр	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Œ	v	w	у	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT340-1		MO-150AG				93-09-08 95-02-04	

1996 Jan 05 12

8-bit bidirectional binary counter

74F269

NOTES

8-bit bidirectional binary counter

74F269

	DEFINITIONS						
Data Sheet Identification	Product Status	Definition					
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.					
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.					
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.					

Philips Semiconductors and Philips Electronics North America Corporation reserve the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

LIFE SUPPORT APPLICATIONS

Philips Semiconductors and Philips Electronics North America Corporation Products are not designed for use in life support appliances, devices, or systems where malfunction of a Philips Semiconductors and Philips Electronics North America Corporation Product can reasonably be expected to result in a personal injury. Philips Semiconductors and Philips Electronics North America Corporation customers using or selling Philips Semiconductors and Philips Electronics North America Corporation Products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors and Philips Electronics North America Corporation for any damages resulting from such improper use or sale.

Philips Semiconductors 811 East Arques Avenue P.O. Box 3409 Sunnyvale, California 94088–3409 Telephone 800-234-7381 Philips Semiconductors and Philips Electronics North America Corporation register eligible circuits under the Semiconductor Chip Protection Act.

© Copyright Philips Electronics North America Corporation 1996

All rights reserved. Printed in U.S.A.

(print code) Date of release: July 1994

Document order number: 9397-750-05112