

Keynote Talk

Exascale Opportunities and Challenges

Katherine Yelick
University of California – Berkeley
and Lawrence Berkeley National Laboratory
Berkeley, CA, USA
yelick@eecs.berkeley.edu

Abstract

Despite the availability of petascale systems for scientific computing, demand for computational capability grows unabated, with areas of national and commercial interest including global climate change, alternative energy sources, defense and medicine, as well as basic science. Past growth in the high end has relied on a combination of faster clock speeds and larger systems, but the clock speed benefits of Moore's Law have ended, and 200-cabinet petascale machines are near a practical limit. In future computing systems, performance and energy optimization will be the combined responsibility of hardware and software developers. Since data movement dominates energy use in a computing system, minimizing the movement of data throughout the memory and communication fabric are essential. In this talk I will describe some of the hardware trends and open problems in developing and using an exascale system. In particular, how will an energy-constrained design affect the architecture, which in turn affects algorithms and programming models. In addition to these universal problems, fault resilience is a problem at the high end that will require novel system support, possibly propagating up the software stack to user level software and algorithms. Overall, the trends in hardware demand that the community undertake a broad set of research activities to sustain the growth in computing performance expected by users.

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Bio

Katherine Yelick is a Professor of Electrical Engineering and Computer Sciences at the University of California at Berkeley and is also the Associate Laboratory Director for Computing Sciences and the Director of the National Energy Research Scientific Computing Center (NERSC) at Lawrence Berkeley National Laboratory. She is the co-author of two books and more than 100 refereed technical papers on parallel languages, compilers, algorithms, libraries, architecture, and storage. She co-invented the UPC and Titanium languages and co-developed techniques for auto-tuning numerical libraries, including the first library for sparse matrix kernels which automatically adapt the code to properties of the matrix structure and machine. Her work includes performance analysis and modeling as well as optimization techniques for memory hierarchies, multicore processors, communication libraries, and processor accelerators. She earned her Ph.D. in Electrical Engineering and Computer Science from MIT and has been a professor of Electrical Engineering and Computer Sciences at UC Berkeley since 1991 with a joint research appointment at Berkeley Lab since 1996. She has received multiple research and teaching awards and is a member of the California Council on Science and Technology and a member of the National Academies committee on Sustaining Growth in Computing Performance.