Memory Read: Data Memory Read (For Loads)

Name: _____ Grade: _____

Course: Computer Architecture

Sample Quiz 5 Solution

Partial credit fo iple part questions will b

FP EX = 4 Cycles Integer EX = 1 Cycle

Iteration	Instruction	Issue Cycle	Execute Start	Execute End	Memory Read	CDB #1 Write	CDB #2 Write	Commit Cycle
1	L.D F0,0(R1)	1	2	2	3	4		5
1	ADD.D F2,F0,F0	1	5	8		9		10
1	MUL.D F4,F0,F0	2	5	8			9	10
1	SUB.D F6,F4,F2	2	10	13		14		15
1	DIV.D F8,F6,F2	3	15	18		19		20
1	S.D F8,8(R1)	3	4	4				20
1	DADDUI R1,R1,#16	4	5	5		6		21
1	BNE R1,R0,Loop	5	7	7				21
2	L.D F0,0(R1)	6	7	7	8	10		22
2	ADD.D F2,F0,F0	6	11	14		15		22
2	MUL.D F4,F0,F0	7	11	14			15	23
2	SUB.D F6,F4,F2	7	16	19		20		23
2	DIV.D F8,F6,F2	8	21	24		25		26
2	S.D F8,8(R1)	8	9	9				26
2	DADDUI R1,R1,#16	9	10	10		11		27
2	BNE R1,R0,Loop	10	12	12				27
3	L.D F0,0(R1)	11	12	12	13		14	28
3	ADD.D F2,F0,F0	11	15	18			19	28
3	MUL.D F4,F0,F0	12	15	18			20	29
3	SUB.D F6,F4,F2	12	21	24			25	29
3	DIV.D F8,F6,F2	13	26	29		30		31
3	S.D F8,8(R1)	13	14	14				31
3	DADDUI R1,R1,#16	14	15	15		16		32
3	BNE R1,R0,Loop	15	17	17				32

Branches Single Issue