Name: _____ Grade: _____

Course: Computer Architecture Sample Quiz 5

Partial credit for incorrect answers can be earned only if you show your work. Errors on multiple part questions will be carried though your answer only if work is provided.

1. Complete the summary table describing the execution of a two-way (2-issue) superscalar, speculative Tomasulo processor for three iterations of the provided MIPS64 loop. The points below describe the operation of the processor (10 points)

- Two-way (2-issue) superscalar, speculative Tomasulo execution
  - Two instructions can be issued and committed simultaneously every clock cycle
  - Branches are issued alone with no delay slot and perfect prediction
- The issue, write CDB, and commit stages each take one clock cycle
- The execution stage takes at least one clock cycle as outlined below
- Dual CDB (2 CDBs) channels - up to two instructions can be written to the CDB at any given clock cycle
- When there is contention for the CDB, instructions issued earlier have priority
- Data dependent instructions start execution the cycle after the final required data is written to the CDB
- Assume all reservation stations can read from both CDBs at once
- There are sufficient reservation stations and reorder buffers available
- Functional units are available as follows
  - 2 load units - loads have one memory access cycle
  - 2 store units - stores have one memory access cycle
  - 3 pipelined FP units - FP operations take 4 execution cycles
  - 7 integer units (2 load, 2 store, 1 branch, 2 ALU) - integer operations have one execution cycle
- Neither store nor branch instructions write to the CDB
- Loads operate as follows
  - One clock cycle to calculate the effective memory address using the integer unit
  - One clock cycle to access memory
  - For stores the memory access cycle is the same/rolled in the commit cycle

```
Loop: L.D      F0,0(R1)
      ADD.D    F2,F0,F0
      MUL.D    F4,F0,F0
      SUB.D    F6,F4,F2
      DIV.D    F8,F6,F2
      S.D      F8,8(R1)
      DADDUI   R1,R1,#16
      BNE      R1,R0,Loop
```

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Course: Computer Architecture Sample Quiz 5

Iteration	Instruction	Issue Cycle	Execute Start	Execute End	Memory Read	CDB #1 Write	CDB #2 Write	Commit Cycle
1	L.D F0,0(R1)							
1	ADD.D F2,F0,F0							
1	MUL.D F4,F0,F0							
1	SUB.D F6,F4,F2							
1	DIV.D F8,F6,F2							
1	S.D F8,8(R1)							
1	DADDUI R1,R1,#16							
1	BNE R1,R0,Loop							
2	L.D F0,0(R1)							
2	ADD.D F2,F0,F0							
2	MUL.D F4,F0,F0							
2	SUB.D F6,F4,F2							
2	DIV.D F8,F6,F2							
2	S.D F8,8(R1)							
2	DADDUI R1,R1,#16							
2	BNE R1,R0,Loop							
3	L.D F0,0(R1)							
3	ADD.D F2,F0,F0							
3	MUL.D F4,F0,F0							
3	SUB.D F6,F4,F2							
3	DIV.D F8,F6,F2							
3	S.D F8,8(R1)							
3	DADDUI R1,R1,#16							
3	BNE R1,R0,Loop