LETTER

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A III–V nanowire channel on silicon for high-performance vertical transistors

Katsuhiro Tomioka[1,2], Masatoshi Yoshimura[1] & Takashi Fukui[1]

Silicon transistors are expected to have new gate architectures, channel materials and switching mechanisms in ten years' time[1–4]. The trend in transistor scaling has already led to a change in gate structure from two dimensions to three, used in fin field-effect transistors, to avoid problems inherent in miniaturization such as high off-state leakage current and the short-channel effect. At present, planar and fin architectures using III–V materials, specifically InGaAs, are being explored as alternative fast channels on silicon[5–9] because of their high electron mobility and high-quality interface with gate dielectrics[10]. The idea of surrounding-gate transistors[11], in which the gate is wrapped around a nanowire channel to provide the best possible electrostatic gate control, using InGaAs channels on silicon, however, has been less well investigated[12,13] because of difficulties in integrating free-standing InGaAs nanostructures on silicon. Here we report the position-controlled growth of vertical InGaAs nanowires on silicon without any buffering technique and demonstrate surrounding-gate transistors using InGaAs nanowires and InGaAs/InP/InAlAs/InGaAs core–multishell nanowires as channels. Surrounding-gate transistors using core–multishell nanowire channels with a six-sided, high-electron-mobility transistor structure greatly enhance the on-state current and transconductance while keeping good gate controllability. These devices provide a route to making vertically oriented transistors for the next generation of field-effect transistors and may be useful as building blocks for wireless networks on silicon platforms.

$In_xGa_{1-x}As$ has attracted attention as an alternative fast channel on silicon for future n-type field-effect transistors (FETs) because of its higher electron mobility compared with that of bulk silicon and its small electron effective mass[13–16]. The Schottky barrier height at the insulator–$In_xGa_{1-x}As$ interface can be adjusted by changing the In content[10]. Using $In_{0.7}Ga_{0.3}As$ fin FETs on Si, it has recently been shown that device performance can be improved by exploiting the three-dimensional architecture and III–V materials[8,9]. As yet, however, there has been less investigation of vertical nanoscale transistors, such as surrounding-gate transistors (SGTs) or gate-all-around FETs using the $In_{0.7}Ga_{0.3}As$ channel on Si (ref. 13). This is because new epitaxial techniques for integrating one-dimensional InGaAs nanostructures on Si substrates must be developed to deal with crystallographic defects (threading dislocations, mis-fit dislocations, antiphase defects and so on) that form as a result of mismatched lattice constants, thermal expansion coefficients and polarities. Several methods using buffering techniques[8,17] have been investigated, but none of them can completely avoid the formation of defects.

Recent progress in selective-area metal–organic vapour phase epitaxy has allowed position-controlled integration of vertical III–V nanowires on Si substrates, regardless of mismatches in terms of the lattice constant, thermal expansion coefficient and polarity[18,19]. We further developed this bottom-up technique for aligning vertical $In_{0.7}Ga_{0.3}As$ nanowires on Si. The important step in aligning vertical $In_{0.7}Ga_{0.3}As$ nanowires on Si(111) is that of forming a (111)B polar surface on a non-polar Si(111) surface by changing from complex Si surface reconstructions to the 1×1 structure[18]. This can be done by annealing the Si(111) substrate at 900 °C in H_2 and then treating it in an AsH_3 atmosphere at 670 °C. During this treatment, the outermost Si atoms are replaced by As atoms in the AsH_3 atmosphere[18]. Flow-rate modulation epitaxy in which group-III and group-V gas source materials are alternately supplied is used to terminate the remaining dangling bonds on Si(111) with group-III atoms (Supplementary Fig. 1). The Si(111) surface terminated with these atoms is isostructural with the (111)B polar surface.

Figure 1a shows typical InGaAs nanowires on Si(111) grown by selective-area metal–organic vapour phase epitaxy (Supplementary Fig. 2). Vertically aligned InGaAs nanowires with $\{1\bar{1}0\}$ side walls and (111)B top surfaces were grown on the Si(111) substrate. The electron transport channel is in the [111] direction in the $\{1\bar{1}0\}$ planes. The transmission electron microscopy image in Fig. 1b reveals that the $\{1\bar{1}0\}$ side walls had atomically flat surfaces and the crystal structure was that of zincblende with rotational twins. The average diameter of the InGaAs nanowires was 90 nm, and the average height was 760 nm. The energy-dispersive X-ray spectroscopy (EDX) line-scan profile in Fig. 1c indicated that the In content of the InGaAs nanowire was $70 \pm 2\%$. The In content remained constant from the bottom to the top of the nanowire. Monosilane (SiH_4) gas was used for n-type doping. The carrier concentration (n) for the n-InGaAs nanowire, as evaluated from both a four-terminal current–voltage measurement[20] and the EDX analysis, was approximately $1 \times 10^{18}\ cm^{-3}$. Figure 1d, e shows the interface of an InGaAs nanowire epitaxially grown on the Si substrate. The heterointerface (Fig. 1d) was apparently free of threading dislocations and antiphase defects, but had periodical misfit dislocations (Fig. 1f). The average period of the misfit dislocation was 38 ± 3 Å. These dislocation networks were formed only at the heterointerface (within three monolayers; see Supplementary Fig. 3).

To characterize the transistor performance of the InGaAs nanowires on Si, we made vertical SGTs (Fig. 2a). We used a structure of stacked Si-doped ($n = 1 \times 10^{18}\ cm^{-3}$) and undoped ($n = 5 \times 10^{16}\ cm^{-3}$) InGaAs nanowires with diameters of 60 nm. The heights of the undoped and Si-doped nanowires were 180 nm and 1.2 μm, respectively. The fabrication processes included deposition of a low-k polymer (benzocyclobutene), and slight etch back using reactive-ion etching (Supplementary Fig. 4). We used $Hf_{0.8}Al_{0.2}O$ as gate oxide. The gate length (L_G) was 200 nm, and the gate–drain distance (L_{G-D}) was 50 nm. Fabricated devices include ten nanowires connected with each other in parallel to a contact pad. The device performance was evaluated at room temperature in the dark.

Figure 2b depicts the capacitance/gate voltage (C–V_G) curves of a single InGaAs nanowire SGT (the nanowire diameter was 90 nm) with an effective oxide thickness (EOT) of 2.75 nm. In this measurement, the drain metal was grounded to avoid the parasitic capacitance of the benzocyclobutene and SiO_2 layers on the Si, and the device comprises 250 nanowires in parallel. The capacitance shown in Fig. 2b is that for a single wire (the measured capacitance was divided by the number of nanowires). We note that in the accumulation region of the C–V_G

[1]Graduate School of Information Science and Technology, and Research Center for Integrated Quantum Electronics (RCIQE), Hokkaido University, Kita 13 Nishi 8, Sapporo 060-8628, Japan. [2]Japan Science and Technology Agency—PRESTO, Kawaguchi, Saitama 332-0012, Japan.

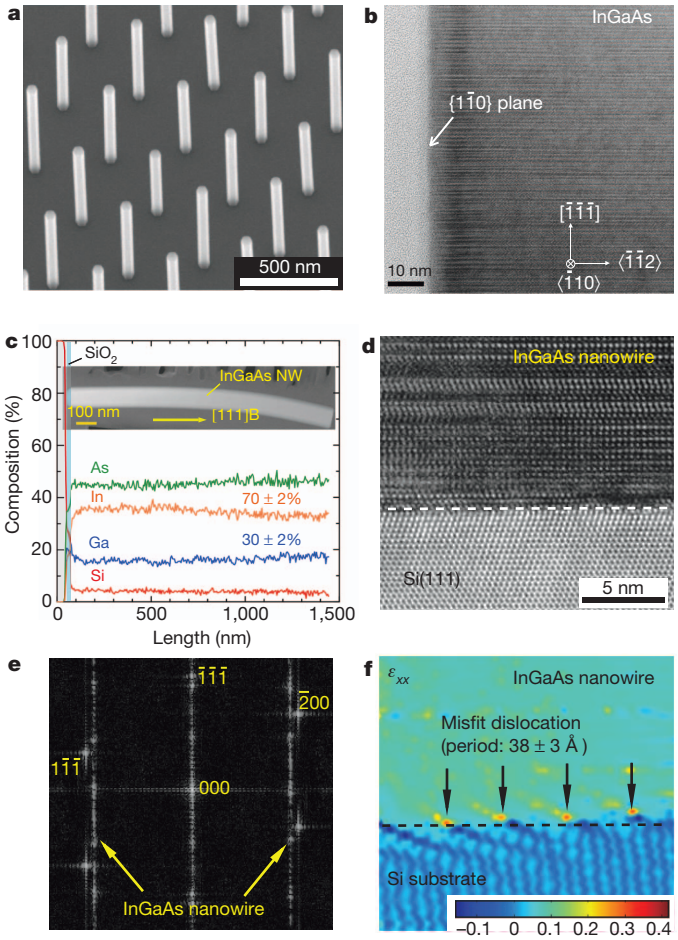

Figure 1 | Selective-area growth of InGaAs nanowires on Si(111). **a**, Typical scanning electron microscope (SEM) image showing selective-area growth of InGaAs nanowires on Si: vertically aligned nanowires were grown on a Si(111) substrate. The surface between the nanowires is covered with an SiO_2 film. The nanowires are 90 nm in diameter and 760 nm in height. They are surrounded by six-sided {1$\bar{1}$0} planes and a (111)B top surface. The electron transport is along the [111] direction. **b**, High-resolution transmission electron microscope (TEM) image of an InGaAs nanowire. The electron beam is incident in the [$\bar{1}$10] directions. The crystal structure is that of zincblende with rotational twins. **c**, Atomic content profiles for Si (red), Ga (blue), As (green) and In (yellow) evaluated along the wire by EDX line-scan profiling. The inset is a high-angle, annular dark-field scanning TEM (HAADF-STEM) image of an InGaAs nanowire with a diameter of 130 nm and a height of 1.4 μm. The In and Ga contents of the InGaAs nanowire were approximately 70 ± 2% and 30 ± 2%, respectively. **d**, High-resolution TEM image of near the heterointerface (dashed line) between the InGaAs nanowire and Si. **e**, Fast Fourier transformation image of **d**, showing diffraction spots of Si and InGaAs. The overlap indicates that the InGaAs nanowire is epitaxially grown on Si. **f**, Strain mapping (ε_{xx}) estimated from a filtered version of **d**.

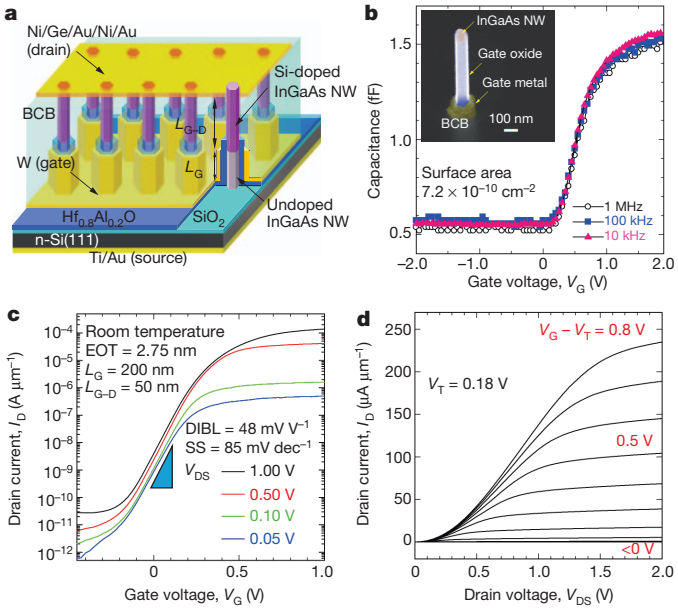

Figure 2 | Vertical InGaAs nanowire channel SGT on Si. **a**, Structure of an SGT with ten nanowires (NWs) connected in parallel with the drain metal. Each nanowire comprises Si-doped InGaAs ($n = 1 \times 10^{18}$ cm^{-3}) stacked on undoped InGaAs ($n = 5 \times 10^{16}$ cm^{-3}) and has a diameter of 60 nm. The heights of the undoped and Si-doped InGaAs nanowires are 180 nm and 1.2 μm, respectively. Each nanowire is wrapped with 14-nm-thick $Hf_{0.8}Al_{0.2}O$ gate oxide and tungsten (W) gate metal. The drain and source metals are respectively Ni/Ge/Au/Ni/Au and Ti/Au. The gate length and gate–drain distance are 200 nm and 50 nm, respectively. **b**, Capacitance/gate voltage curves of the SGT (nanowire diameter, 90 nm). The sample has 250 nanowires aligned in parallel. The capacitance indicated is that for a single wire. Inset is a representative SEM image showing the SGT structure. In this measurement, the drain metal is grounded to avoid the parasitic capacitance of the SGT and benzocyclobutene (BCB). **c**, Transfer characteristics of an SGT with InGaAs nanowires (nanowire diameter, 60 nm). The drain current indicated is that for one wire and is normalized by the outer perimeter of the gate (180 nm). The SS and DIBL are 85 mV per decade and 48 mV V^{-1}, respectively. **d**, Output characteristics of an SGT with InGaAs nanowire channels. The gate voltage (bias) is changed from −0.4 to 1.0 V in steps of 0.1 V. The threshold voltage is estimated to be 0.18 V using linear extrapolation of the output characteristics.

curves in Fig. 2b, the frequency dispersion between 10 kHz and 1 MHz was less than 4%, and that in this frequency range the flat-band voltage was no longer shifted. The C–V_G curves had no noticeable hysteresis, as revealed by bidirectional sweeps of V_G, and the gate leakage current obtained for various EOTs was small: 10^{-3}–10^{-5} A cm^{-2} (Supplementary Fig. 5). These data indicate that the $Hf_{0.8}Al_{0.2}O$–$In_{0.7}Ga_{0.3}As$ interface was of good quality, with few interface states.

Figure 2c, d show the transfer and output characteristics of the InGaAs nanowire SGT on Si. The drain currents are those for a single wire (calculated as for Fig. 2b) and are normalized by the outer perimeter of the gate, that is, channel width. The switching properties showed an n-type enhancement mode with a threshold voltage (V_T) of 0.18 V. The source–drain current (I_D) was modulated by V_G with a minimum subthreshold slope (SS = dV_G/d[log(I_D)]) of 85 mV per decade. The InGaAs nanowire SGT had an on/off current ratio (I_{ON}/I_{OFF}) of 10^6 and a peak transconductance (G_m) of 280 μS μm^{-1} at a drain–source voltage of $V_{DS} = 1.00$ V. The drain-induced barrier lowering (DIBL) was estimated to be 48 mV V^{-1}. After analysing InGaAs nanowires SGTs with various EOTs (Supplementary Fig. 6), we found that SS and the DIBL were independent of the EOT and averaged 82 mV dec^{-1} and 45 mV V^{-1}, respectively. These switching characteristics are much better than those of SGTs using InAs nanowire channels on Si (refs 21–24); however, this simple, InGaAs nanowire-based SGT requires further improvements to satisfy the technological demands of next-generation metal–oxide–semiconductor FETs[2]. In particular, the channel mobility must be enhanced by decreasing the number of surface states.

We therefore designed and fabricated an improved structure, that is, $In_{0.7}Ga_{0.3}As$/InP/$In_{0.5}Al_{0.5}As$/δ-doped $In_{0.5}Al_{0.5}As$/$In_{0.5}Al_{0.5}As$/$In_{0.7}Ga_{0.3}As$ modulation-doped core–multishell (MD-CMS) nanowires (Fig. 3a). The advantage of selective-area growth is the ability to form a CMS structure that allows surface passivation[19]. In addition, modulation-doped layers such as those on high-electron-mobility transistors[25] can be packed into the CMS layers. The InGaAs outer-shell layer is a cap designed to maintain good interface quality with the $Hf_{0.8}Al_{0.2}O$ layer, and confines carriers when $V_G < V_T$. The InAlAs/δ-doped layer/InAlAs structure forms the modulation-doped layers. The I_D and V_T depends on the confined carriers and the region to which they are confined. The InP layer is a barrier that allows the position of the

confined carriers to be controlled by varying V_G. These confined electrons do not contribute to the drain current because this layer is separated from the drain metal. However, electrons penetrate the InP barrier layer and are confined in the core InGaAs nanowire when $V_G > V_T$. The band diagram of the MD-CMS nanowire when $V_G = 0.5$ V (Fig. 3b, calculated using the one-dimensional Poisson–Schrödinger equation[26]) suggests that the carriers are confined in the nanowire for, in that case, $V_G = 0.50$ V. The MD-CMS nanowire SGT is thus normally off. Figure 3c is a representative SEM image of the vertical MD-CMS nanowires on Si. The HAADF-STEM image and EDX elemental mappings in Figs 3d–j show that the CMS layers formed around the InGaAs nanowire core. The thicknesses of the InP, InAlAs, δ-doped, InAlAs and InGaAs capping layers were respectively about 2.6, 5.5, 5.5, 5.5 and 5.0 nm (Supplementary Fig. 7). The dark regions at the corners of the outer MD-CMS layer (Fig. 3d) indicate that Al-rich InAlAs formed through segregation of Al. The Al-rich parts separate the tubular modulation-doped channels into six-sided transistor layers. Accordingly, the six-sided transistor layers could be integrated onto a single tiny nanowire.

Figure 4a, b shows the device performance of the SGTs using MD-CMS nanowire channels on Si. The diameter of the InGaAs nanowire cores was 90 nm. The drain currents shown are those for a single wire (measured current divided by the number of nanowires and normalized by gate outer perimeter). The SGT showed an n-type enhancement mode with a threshold voltage of 0.38 V. The C–V_G characteristic (Fig. 4c) shows a positive shift of the flat-band voltage and a reduction in capacitance due to the gate dielectric/CMS layers, relative to that of the InGaAs nanowire SGT. The I_{ON}/I_{OFF} ratio was approximately 10^8. The I_{OFF} was <10 pA μm^{-1}, which was much lower than that of a conventional Si metal–oxide–semiconductor FET[1]. The SS and DIBL were 75 mV per decade and 35 mV V^{-1}, respectively. The CMS nanowire SGTs achieved both a steep SS and a very low DIBL, indicating suppression of the short-channel effect owing to the multigate architecture[1]. The drain current reached 0.45 mA μm^{-1} at $V_G - V_T = 0.50$ V, and G_m was 1.42 mS μm^{-1} at $V_{DS} = 0.50$ V. The very large increase in I_D and G_m together with the steep SS indicates that the CMS multilayers acted as a modulation-doped, high-electron-mobility structure while maintaining good controllability of the surrounding-gate structure. These results are superior to those from

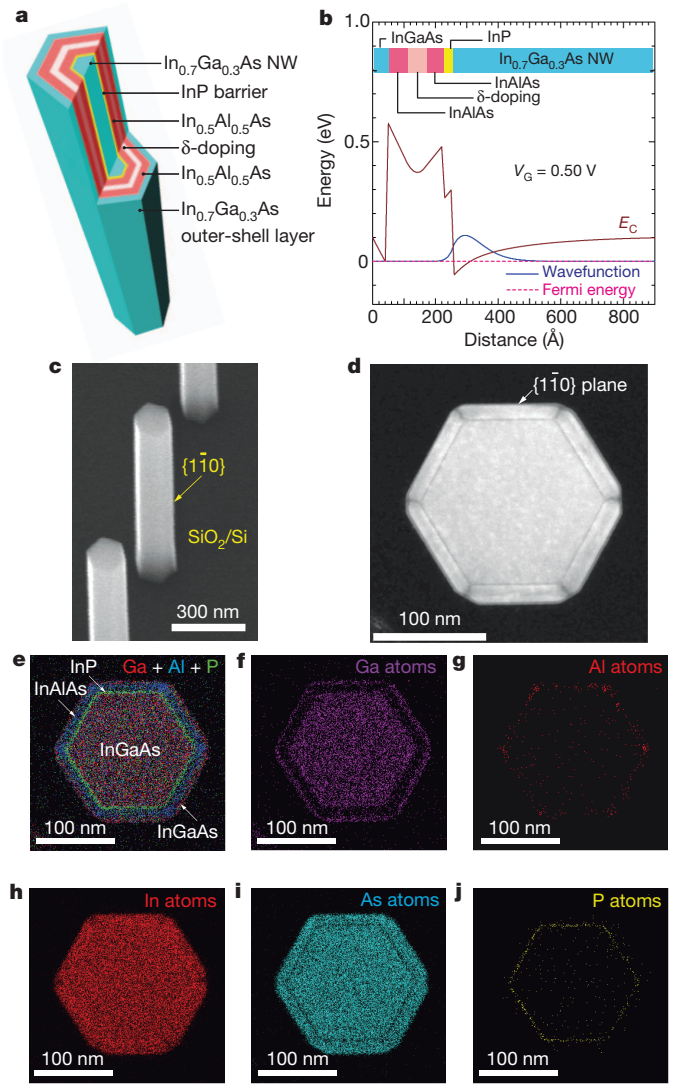

Figure 3 | Formation and characterization of InGaAs/InP/InAlAs/InGaAs CMS nanowires on Si. a, Illustration of designed and fabricated structure. The InGaAs nanowire core is wrapped with InP/InAlAs/δ-doped InAlAs/InAlAs/InGaAs multilayers. **b**, Band diagram of the MD-CMS nanowire at $V_G = 0.50$ V simulated using the one-dimensional Poisson–Schrödinger equation, suggesting confinement of carrier wavefunction (blue curve) in the InGaAs nanowire. The red dashed line denotes the Fermi level. The conduction band is denoted E_C. Without a gate bias, the carrier wavefunction is confined in the outer InGaAs shell layer. **c**, Typical SEM image showing vertical MD-CMS nanowires on Si. The average diameter and height of these nanowires are 180 nm and 1.2 μm, respectively. The CMS layers are grown on the side walls of the core InGaAs nanowires. **d**, HAADF-STEM image showing a representative cross-section of a CMS nanowire with a total diameter of 180 nm. **e–j**, EDX elemental mapping images: mixing of Ga, Al and P (**e**); Ga (**f**); Al (**g**); In (**h**); As (**i**); and P (**j**). The Al mapping (**g**) shows segregation of the Al at the corner of the CMS nanowire.

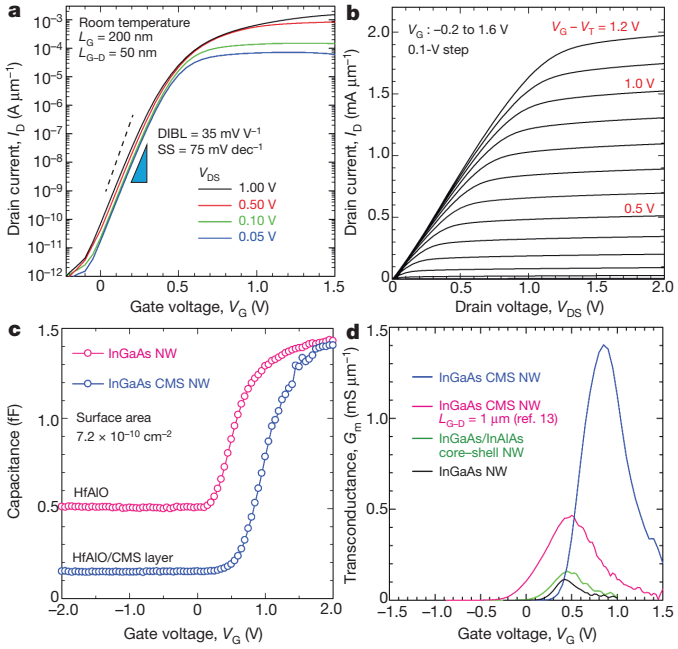

Figure 4 | Performance of an SGT using InGaAs/InP/InAlAs/InGaAs CMS nanowire channels on Si. a, Transfer characteristics of an SGT with $L_G = 200$ nm and $L_{G-D} = 50$ nm. SS is 75 mV per decade and DIBL is 35 mV V^{-1}. The dashed line indicates the physical limit of SS (60 mV per decade at room temperature). **b**, Output characteristics of an InGaAs CMS nanowire SGT. **c**, Capacitance/gate voltage curve of a InGaAs nanowire (pink circles) and a InGaAs CMS nanowire (blue circles). The capacitances shown are the measured values divided by the number of nanowires (250 for InGaAs nanowires and 512 for InGaAs CMS nanowires). The frequency in this measurement is 1 MHz. **d**, Transconductance of SGTs using InGaAs nanowires (black), InGaAs/InAlAs core–shell nanowires (green), MD-CMS nanowires with $L_{G-D} = 1$ μm (pink; ref. 13) and MD-CMS nanowires (blue). $V_{DS} = 0.50$ V.

devices made from similar materials and with similar dimensions[12,13]. Figure 4d shows G_m curves for the SGTs using InGaAs nanowires, InGaAs/InAlAs core–shell nanowires and MD-CMS nanowires. The MD-CMS nanowire channel results in a pronounced increase in G_m. The field effect mobility tentatively estimated from G_m (Supplementary Fig. 8) is much higher than the typical electron mobility of a Si metal–oxide–semiconductor FET[27]. Consequently, the SGT devices reported here could have the performance necessary for use in future Si transistor technology[28].

METHODS SUMMARY

The InGaAs nanowires and InGaAs/InP/InAlAs/InGaAs CMS nanowires were grown by using selective-area metal–organic vapour phase epitaxy. High-resolution TEM (H-9000UHR with acceleration voltage of 300 kV; Hitachi) was used to evaluate the crystal structure and to estimate the strain[29]. HAADF-STEM (JEM2100F with an acceleration voltage of 200 kV) and EDX (JEOL JED-2300T) were used to analyse the elemental mapping of the CMS nanowires. The SGTs were fabricated with a reactive-ion etching procedure. The current–voltage curves were measured with an Agilent 4192A impedance analyser. The transistor performance was evaluated with an Agilent 4156C parameter analyser. All current measurements were performed at room temperature (300 K) in the dark. For display, the measured capacitances were divided by the number of nanowires and the measured currents were divided by the number of nanowires and normalized by the gate outer perimeter.

Full Methods and any associated references are available in the online version of the paper.

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Supplementary Information is linked to the online version of the paper at www.nature.com/nature.

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Author Contributions K.T. designed the experiments, made the nanowires by metal–organic vapour phase epitaxy, fabricated the device and analysed all of the data. T.F. planned and supervised the study. M.Y. helped in the epitaxy experiments. All authors discussed the results and commented on the manuscript.

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METHODS

Selective-area metal–organic vapour phase epitaxy. After the Si(111) substrate was degreased with organic solvents, a 20-nm-thick SiO_2 film was formed by thermal oxidation. Circular openings arranged in a triangular lattice with a pitch of 3 μm were then formed on the SiO_2 films by using electron-beam lithography and wet chemical etching. The opening diameter, d_0, was 90 nm. The nanowires were grown using metal–organic vapour phase epitaxy.

Growth of InGaAs nanowires. The InGaAs nanowires were grown in a horizontal, low-pressure (0.1-atm) system. Trimethylgallium (TMGa), trimethylindium (TMIn) and arsine (AsH_3) gas were used as material sources and monosilane (SiH_4) was used as the n-type dopant. After thermal cleaning at 900 °C in H_2, AsH_3 treatment at 670 °C and flow-rate modulation epitaxy were carried out, in which the material source (TMGa + TMIn) and AsH_3 were supplied alternately with intervals of H_2. The TMGa + TMIn, AsH_3 and H_2 supply durations were respectively 1, 1 and 2 s. After that, InGaAs nanowires were grown for 20 min at 670 °C. The partial pressures of the TMGa, TMIn, AsH_3 and SiH_4 were respectively 5.7×10^{-7}, 9.7×10^{-7}, 2.5×10^{-4} and 2.5×10^{-7} atm.

Formation of InGaAs/InP/InAlAs/InGaAs CMS nanowires. After the growth of the InGaAs nanowires, InP/InAlAs/δ-doped InAlAs/InAlAs/InGaAs layers were grown at 580 °C. Trimethylaluminium (TMAl) and *tert*-butylphosphine (TBP) were used as the Al and P sources. The growth times for the InP, InAlAs, δ-doped InAlAs, InAlAs and InGaAs layer were respectively 10, 40, 40, 40 and 30 s. The partial pressures of the TMIn and TBP for the InP layer were respectively 4.4×10^{-6} and 1.6×10^{-4} atm. The partial pressures of the TMAl, TMIn, AsH_3 and SiH_4 for the InAlAs layer were respectively 5.3×10^{-7}, 4.9×10^{-7}, 2.5×10^{-4}, 2.5×10^{-4} and 1.2×10^{-7} atm.

Strain mapping. Strain mapping estimated from the displacement of bright spots in the TEM image is shown in Fig. 1f. The strains, ε_{xx} and ε_{yy} (Supplementary Fig. 3), were calculated from the displacement of bright spots in Fig. 1d by using a peak-pair algorithm[29], and the displacements of the bright spots are defined by $u_{xx} = \Delta x - a_{Si(x)}$ for the in-plane $\langle 2\bar{1}\bar{1} \rangle$ direction and by $u_{yy} = \Delta y - a_{Si(y)}$ for the vertical $\langle 111 \rangle$ direction. Here Δx and Δy are the displacements of the bright spots in each direction, and $a_{Si(x)}$ and $a_{Si(y)}$ are the lattice constants in the in-plane and vertical directions of the Si(111) substrate, estimated from the TEM image. The strains ε_{xx} and ε_{yy} are also given by $\varepsilon_{xx} = \partial u/\partial x$ and $\varepsilon_{yy} = \partial u/\partial y$, where $u = \sqrt{u_{xx}^2 + u_{yy}^2}$. We note that, because the displacement of the atoms is calculated on the basis of the position of the atoms in crystalline Si, InGaAs is mapped into a layer with a strain of +8.1% by definition. The error in the strain calculation is approximately ±0.5%.

Fabrication of SGTs. After the InGaAs nanowire growth, the nanowires were treated with an alkaline solution to etch away native oxides. The nanowires were then covered with $Hf_{0.8}Al_{0.4}O_x$ ($\varepsilon_{HfAlO} = 20.4$) film using atomic layer deposition. This oxide was used as the gate oxide, and it ranged in thickness from 10 nm (EOT = 1.86 nm) to 20 nm (EOT = 3.72 nm). Next the gate metal, tungsten (W), was deposited by radio-frequency sputtering (Supplementary Fig. 4b). After the W was lithography patterned for nanowire-grown masks ($50 \times 50\ \mu m^2$), the nanowires were spin-coated with benzocyclobutene (BCB) (Supplementary Fig. 4c) and etched back by reactive-ion etching (RIE) with CF_4/O_2 to etch the BCB, W and $Hf_{0.8}Al_{0.2}O$ gate oxide simultaneously (Supplementary Fig. 4d). After the RIE process, the nanowires were spin-coated with BCB, and etched back again by RIE (Supplementary Fig. 4e) to isolate the gate and drain metals. A Ni/Ge/Au/Ni/Au multilayer was evaporated onto a lithographically defined region to serve as the drain contact. A Ti/Au multilayer was deposited onto the Si substrate to serve as the source contact Supplementary Fig. 4f). The device had ten nanowires, which were connected in parallel to a single drain contact pad. The gate length was 200 nm. Finally, the nanowire SGT was annealed at 420 °C in N_2 to obtain ohmic contacts at the source and drain regions.