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ORIGINAL RESEARCH ARTICLE

Thermal Analysis of Gallium Oxide-Based Field-Effect Transistors on Different Substrates

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Abstract

In this paper, a compact model is presented for the calculation of thermal resistance of gallium oxide-based field-effect transistors (FETs). A gallium oxide epilayer with different substrates of gallium oxide, silicon carbide (SiC), silicon and sapphire is considered for the modeling. Thermal resistance is realized with different epilayer, substrate and gate width thickness. The model is compared and verified on the COMSOL simulation platform with different parametric variations. The model compares favorably with simulation counterparts, with very close agreement (2–3%). Furthermore, channel temperature is also calculated using analytical modeling which helps power device engineers to design the product accordingly. The paper also presents a comparative analysis of the gallium oxide epilayer with different substrates (sapphire, silicon, siC and gallium oxide) to reduce the self-heating effects, which will improve device performance. The gallium oxide epilayer with a SiC substrate-based device shows the best performance in terms of lower thermal resistance and channel temperature. This may help to explore a wide array of possibilities for reducing problems with the thermal characteristics of gallium oxide devices. The analytical modeling presented here helps elucidate the thermal properties of gallium oxide-based devices from both a simulation and fabrication point of view.

Keywords Thermal resistance · channel temperature · analytical model · thermal conductivity · gallium oxide

Introduction

Wide-band-gap semiconductors play a crucial role in the field of power electronics due to their material properties and advantages. Gallium nitride and silicon carbide-based devices are widely used for various power electronics applications including high-voltage switching, radio-frequency (RF) power amplifiers, satellite communication and electric vehicles.[1] Generally, wide-band-gap devices offer very high power density but at the same time require proper thermal management for their flawless operation. Recently, gallium oxide has emerged as a next-generation power electronics material due to its major advantages in the field, namely (i) very high critical electric field strength (8MV/cm), (ii) high-temperature operation compatibility due to its ultra-wide band gap, and (iii) ease of high-quality crystal growth with conventional melt-based techniques.[2,3] These advantages make gallium oxide a promising candidate over GaN and SiC in such applications. Researchers have devoted substantial effort to the further development of gallium oxide-based devices by improving their electrical properties and figures of merit. The practical demonstration of gallium oxide-based devices shows the limitation of these devices in terms of self-heating response due to the low thermal conductivity of gallium oxide (κ= 27 W/mK [010]) and electron-phonon scattering in high-field distribution.[3,4] This limitation requires further research and exploration in the field to improve the reliability of gallium oxide-based devices. The proper operation and reliability of these devices depend on device temperature and thermal resistance, which define the performance and characteristics of the device. Packaging and proper cooling mechanisms are used to reduce the device limitations due to the high-junction-temperature operability. Heat flow through the devices is limited by thermal resistance, which leads to an increase in the channel/junction temperature. Therefore, an accurate estimation of the thermal characteristics of the device is important. As

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the thermal behaviour of the device plays a crucial role in the overall device performance, a suitable analytical thermal model is required which can efficiently relate the thermal properties of gallium oxide-based devices in an accurate and time-effective manner. A few thermal models and simulations for estimation of the maximum temperature of gallium oxide metal–oxide–semiconductor field-effect transistors (MOSFETs) and other FETs have been reported experimentally and theoretically.[5–19] The availability of an analytical model will help power device design engineers in developing the optimized design for reduced thermal resistance and improved reliability. In this paper, we propose a simple Laplace equation in a spheroidal and cylindrical coordinate-based analytical model with closed expressions for the calculation of thermal resistance and maximum channel temperature for gallium oxide-based devices. The analytical model depicts the actual heat propagation to better visualize the thermal contours in the device. The proposed analytical model with accurate solvable equations can be applied to gallium oxide-based MOSFETs with various substrates. The feasibility and accuracy of the proposed analytical model are verified by comparison with COMSOL Multiphysics-based numerical simulations.

Simulation Setup and Analysis

Gallium oxide-based MOSFETs are considered with different substrates and gallium oxide epilayers. The MOSFET considered for thermal modelling consists of a gate terminal area ($L_g \times W_g$) as the heat source for the device, which generates a constant heat flux at a fixed bias. For the simplicity of the model, the heat flux is considered to be unidirectional (from top to bottom); the substrate acts as a heat sink and the bottom surface is considered isothermal whose temperature is kept at room temperature/ambient temperature (300 K). The gate dielectric is very thin (a few nanometers) and assumed to have no affect on the thermal resistance calculation, and so is neglected in this case. The cross-section of the device taken is presented in Fig. 1. The gallium oxide epilayer with thickness t_1 and comparatively very large substrate of thickness t_2 is taken into account for the calculation of thermal resistance. The assumptions taken for the thermal modelling of the device are as follows:

1. The gate area ($L_g \times W_g$) is considered as a constant heat source.
2. The substrate bottom is considered as an isothermal surface (constant room temperature).
3. All other boundaries are considered to be adiabatic, and no outer heat flux is allowed.
4. Different substrates and epilayers are considered with their respective constant thermal conductivity.

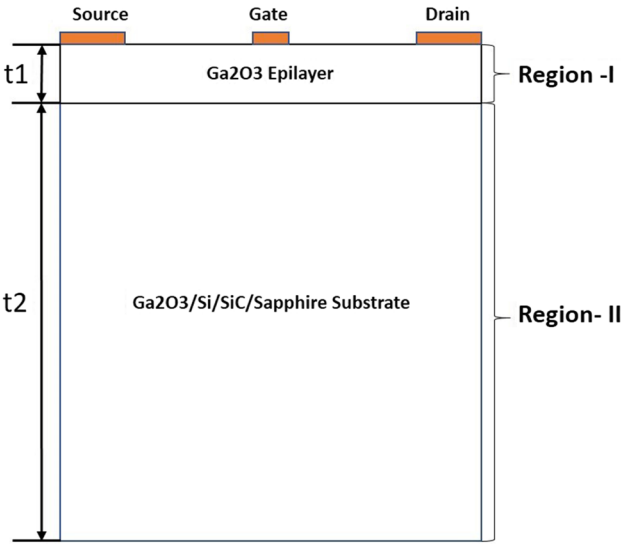

Fig. 1 Cross-sectional view of the modeled device.

The state of the two contacting surfaces can have a considerable impact on the interfacial thermal resistance at the interface of two materials. A surface's cleanliness, waviness, contact pressure, roughness, yield strength and thermal conductivities of the solids are a few of the characteristics that can have an impact on interfacial thermal resistance. The contact thermal resistance is subject to a wide range of influences, making it challenging to theoretically predict its value. Hence, due to the model's simplicity in this manuscript, interfacial resistance is not taken into account. The two main factors which contribute to heat dissipation are (i) the spreading of thermal resistance in the gallium oxide epilayer and (ii) the substrate or bulk thermal resistance. Therefore, the structure is considered as the two-layer problem, with region I consisting of a tiny heat source, and region II lying in the substrate part with an isothermal bottom surface as shown in Fig 2. In region I, isothermal lines are assumed to propagate as prolate spheroids, and in region II the isothermal lines are assumed to be elliptical cylinders with horizontal spreading. These coordinate systems are used to derive a closed-form expression for the exact calculation of thermal resistance (θ) of these layers. The total thermal resistance is the sum of the thermal resistance of these two regions.

$$\theta_{\text{total}} = \theta_1 + \theta_2 \tag{1}$$

Thermal resistance in region I belongs to the heat source with an epilayer of gallium oxide MOSFET, which plays a major role due to the very low thermal conductivity of gallium oxide, whereas region II represents the substrate part. In this work, we are primarily concerned with substrate characteristics. The interfacial resistance models are therefore

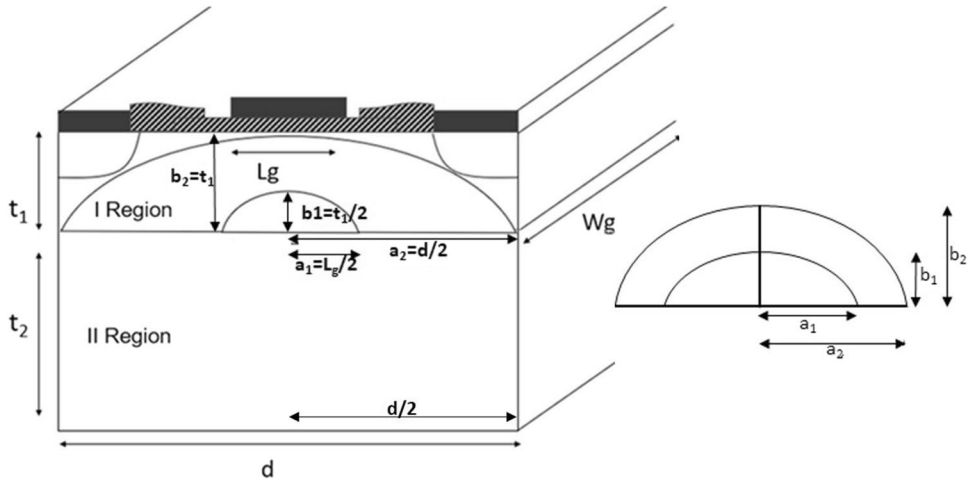

Fig. 2 Block diagram for modeling and assumptions.

simplified, and as a result, they are not currently taken into consideration for the sake of simplicity. The thermal resistance expression for each region is described below.

Region I Thermal Resistance

The isotropic lines in this region are assumed to be prolate spheroidal in nature, so thermal resistance in this region can be estimated by applying the Laplace solution to this coordinate system. For simplicity, cylindrical coordinates are used for the calculation. The thermal conductivity for this region is considered as the constant thermal conductivity of the epilayer ($\kappa = \kappa_{epi}$). For inner prolate, the inner radius is considered equal to half of the gate length (L_g), and the outer radius is assumed to be equivalent to half of the separation between the two gate fingers (d). Basic heat equations are used for the analytical modelling of the thermal resistance calculation in the gallium oxide-based FETs.[20,21] The heat distribution and temperature change per unit area in a given medium using Fourier law are given by the following expression:

$$\mathrm{q} = -\mathrm{kA}\frac{dT}{dr} \tag{2}$$

where k is thermal conductivity and r is the radius of the cylindrical region through which heat is distributed, and is solved as follows:

$$\int_{r_1}^{r_2} \frac{q}{kA} dr = \int_{T_1}^{T_2} -dT \tag{3}$$

$$\frac{q}{\pi kt}\left(\ln \mathrm{r}_2 - \ln \mathrm{r}_1\right) = -(\mathrm{T}_2 - \mathrm{T}_1) \tag{4}$$

$$\mathrm{q} = \frac{T_1 - T_2}{\frac{1}{\pi kt}\ln\frac{r2}{r1}} \tag{5}$$

Similarly,

$$q = \frac{\Delta T}{\theta} \tag{6}$$

Thus, by comparing Eqs. 5 and 6, we obtain the thermal resistance for the structure as θ_1

$$\theta = \frac{1}{\pi kt}\ln\frac{r_2}{r_1} \tag{7}$$

In this case k is thermal conductivity, so the thermal conductivity of the epilayer is considered as k_{epi}, and the gate width of the structure is W_g. The heat source is the gate area and the heat waves are assumed to be transferred in bulk in a ellipsoidal piped manner; hence the heat charge (q) for the ellipsoidal pipe is given by [22,23]

$$\mathrm{q} = \frac{2\pi k(T_1 - T_2)}{\ln\frac{(a_2+b_2)}{(a_1+b_1)}} \tag{8}$$

Therefore, from Eq. 8 the thermal resistance for region I (θ_1) is given by

$$\theta_1 = \frac{1}{\pi k_{epi} W_g}\ln\frac{(a_2+b_2)}{(a_1+b_1)} \tag{9}$$

where W_g is the gate width, L_g is gate length, t_1 is epilayer thickness, $\mathrm{k_{epi}}$ is the thermal conductivity of the gallium oxide epilayer, and d is the gate spacing between two heat sources. The dimension assumptions are considered as $a_2 = d/2, a_1 = L_g/2, b_2 = t_1, b_1 = t_1/2$ as shown in Fig. 2. After putting these values in Eq. 9, we obtain the final thermal resistance for region I as

$$\theta_1 = \frac{1}{\pi k_{epi} W_g}\ln\left(\frac{d+2t_1}{L_g+t_1}\right) \tag{10}$$

Region II Thermal Resistance

For calculations of thermal resistance in this region, Laplace solutions are calculated for isothermal lines which are assumed as elliptical cylinders with horizontal spreading. For simplicity, a rectangular coordinate system is used for calculation. This region represents the bulk resistance of the device, which has a negligible effect on the distance between two gates (d). Where $t_2 \gg L_g$ and $W_g \gg L_g$ these two assumptions based on gallium oxide-based practical configuration are considered. Hence, the thermal resistance for this region is calculated as:

$$\theta_2 = \frac{t_2}{k_{\text{Sub}} W_g d} \tag{11}$$

The total thermal resistance for the device can be given by the sum of the two individual areas. The total thermal resistance θ_{total} is given by:

$$\theta_{\text{total}} = \theta_1 + \theta_2 = \frac{1}{\pi k_{epi} W_g} \ln\left(\frac{d + 2t_1}{L_g + t_1}\right) + \frac{t_2}{k_{\text{Sub}} W_g d} \tag{12}$$

The substrate is very thick [$t_2 \gg$gate spacing (d)] and the thickness of the source, gate and drain terminal are also considered to be very thin (a few nanometres), so their heat capacity is ignored for the analytical modelling. In addition, the heat transfer through radiation and convection is assumed to be zero, and all other boundaries except the heat source (top side) are defined as adiabatic. Using this analytical modelling, the thermal resistance of the gallium oxide MOSFET is calculated. For better understanding and greater clarification of the effects of thermal conductivity, different substrates are included in the calculations. The thermal conductivity of gallium oxide plays a crucial role in the modelling. As, the anisotropic nature of gallium oxide thermal conductivity is reported in the literature.[24] We have used a standard equation for the thermal conductivity of gallium oxide [010] as follows:

$$k_{\text{Galliumoxide}}(T) = 0.234\left(\frac{T}{300}\right)^{-1.27} [\text{ W/cm.}K] \tag{13}$$

Other parameters including gate width, epilayer thickness and substrate thickness variation with different substrates are used to check the compatibility and feasibility of the model.

Model Verification

Thermal Resistance Calculation

Generally, power devices consist of multiple-gate fingers, but the maximum heat is typically observed at the middle finger. For simplicity, in this model, we have considered the single-finger gate structure which is considered as an adiabatic plane with regard to the surrounding faces. The heat flux is calculated with the help of Silvaco ATLAS software, which is simulated with the same geometry considered for the analytical modelling. The generated heat power on the gate terminal is taken into account for the numerical simulations carried out using the Heat Transfer module of COMSOL Multiphysics. Figure 5 shows the joule heat power distribution in a gallium oxide-based FET structure, which has maximum heat generation at the drain edge of the gate contact. However, no literature has reported the experimental demonstration of the effects of junction temperature on gallium oxide MOSFETs. Hence, these analytical models are required to predict the device behaviour for better design and reliability. Therefore, the thermal resistance for gallium oxide MOSFET is calculated using the analytical modelling. The following parameters are used for different comparisons. $t_1 = 300$ nm, $L_g = 2$ μm, d = 24 μm, $W_g = 500$ μm, $t_2 = 200$ μm, $k_{Ga2O3} = 0.27$ W/cm.K [010], $k_{Si} = 1.5$ W/cm.K, $k_{SiC} = 3.7$ W/cm.K, $k_{\text{Sapphire}} = 0.4$ W/cm.K. Overall calculations from Fig. 3(i), (ii), and (iii) shows that the thermal resistance increases with the increase in different device design parameters including gate width, substrate thickness and epilayer thickness. Figure 3(iv) shows enlarged view of thermal resistance for gallium oxide epilayer over gallium oxide substrate. Furthermore, simulation results show that the proposed analytical model predicts the heat flow within the device structure and its thermal resistance so accurately.

The thermal resistance calculated using this analytical model is independent of temperature. Furthermore, this model does not include any effects of packaging and mounting. The model is applied on gallium oxide epitaxial structures with homo and hetero substrates to analyse the thermal effects due to various factors. To verify our modelling we have used a standard finite element analysis software COMSOL Multiphysics (Heat Transfer Module). The analysis is conducted on the structure as shown in Fig. 4. We observed very good agreement with analytical

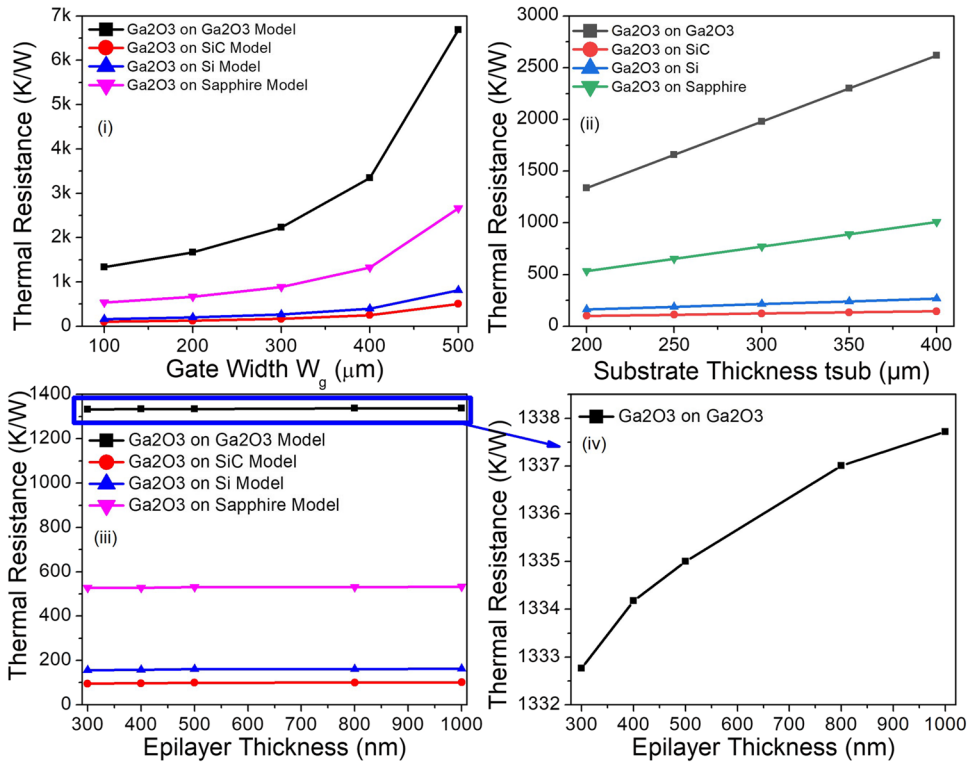

Fig. 3 Thermal resistance calculation with different parametric variations using analytical model. (i) Gate width variation, (ii) substrate thickness variation, (iii) epilayer thickness variation, (iv) shows enlarged view of thermal resistance for gallium oxide epilayer over gallium oxide substrate.

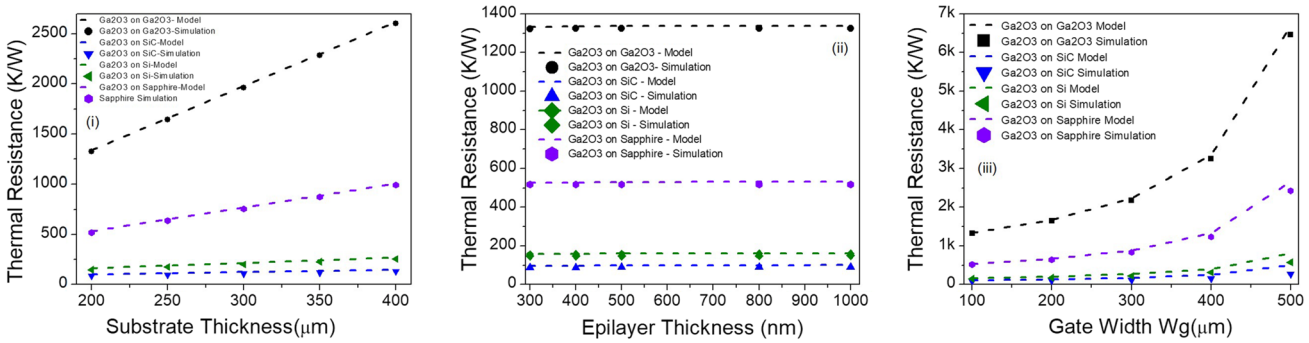

Fig. 4 Thermal resistance calculation validation with COMSOL simulations. (i) Substrate thickness variation, (ii) epilayer thickness variation, (iii) gate width variation.

Table I Analytical modeling and thermal simulation comparison for thermal resistance

Thermal resistance (K/W)	Ga2O3 On SiC	Ga2O3 On Si	Ga2O3 On sapphire	Ga2O3 On Ga2O3
COMSOL simulation	97.23	157	526.4	1322.97
This model	100.71	161.82	531.86	1337.72

modelling and COMSOL Multiphysics simulation results, as shown in Table I. These results with different parametric variations are discussed below.

Calculation of Channel Temperature

Junction temperature is an important parameter for predicting the performance quality of a device. Device engineers continuously look for ways to minimize the junction temperature for more efficient performance and long durability of the designed device. This model further uses the thermal resistance value for the calculation of channel temperature, using the following equations. The junction temperature is also calculated with the help of analytical modelling and the following equations:

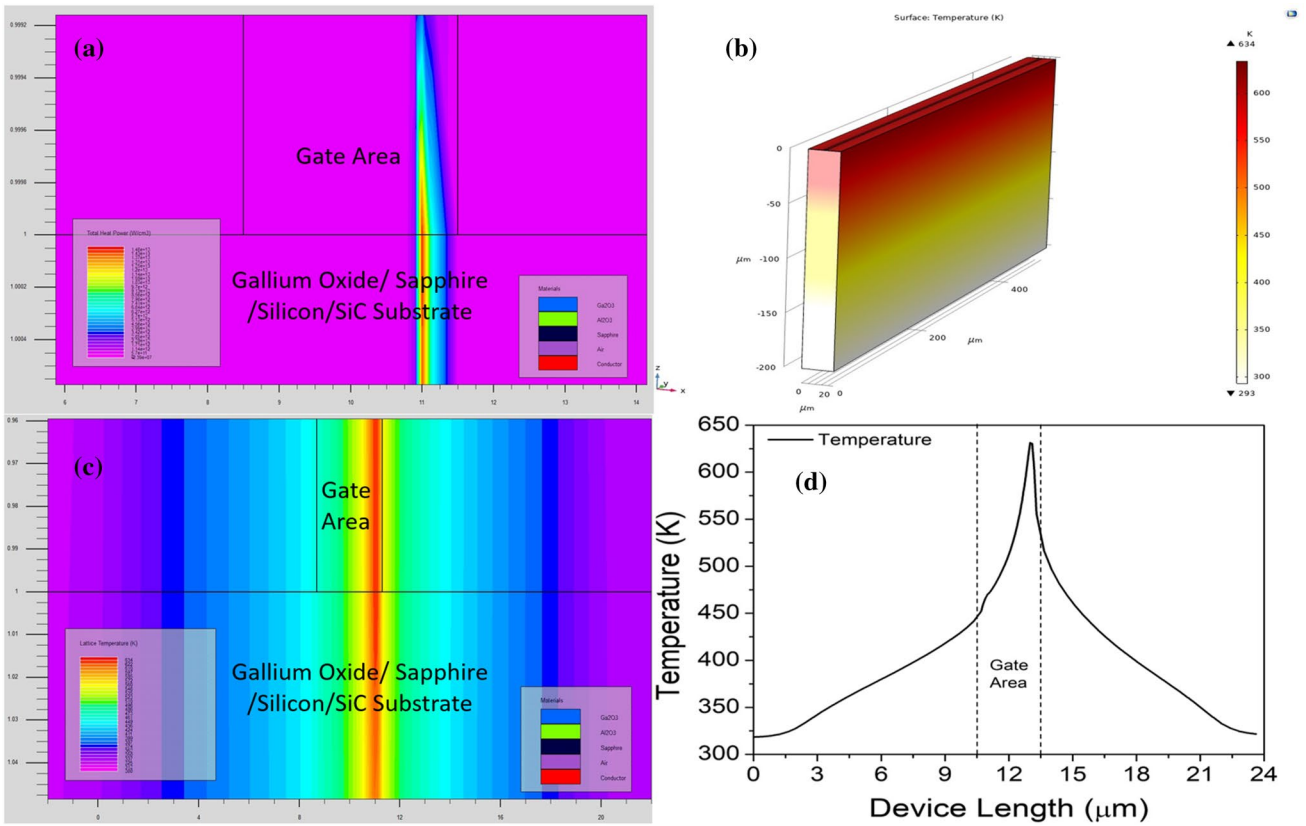

Fig. 5 (a) Heat power calculation in Silvaco ATLAS, (b) simulated structure in COMSOL Multiphysics, (c) cross-sectional view of the temperature distribution around the gate area, (d) temperature distribution across the device length.

$$T_1 = \theta_1 \cdot P_{\text{loss}} + T_2 \tag{14}$$

$$T_2 = \theta_2 \cdot P_{\text{loss}} + T_3 \tag{15}$$

Combining these equations and putting θ_1 and θ_2 values,

$$T_1 = \frac{1}{\pi k_{epi} W_g} \ln\left(\frac{d + 2t_1}{L_g + t_1}\right) \cdot P_{\text{loss}} + T_2 \tag{16}$$

$$T_2 = \frac{t_2}{k_{\text{Sub}} W_g d} \cdot P_{\text{loss}} + T_3 \tag{17}$$

$$T_{\max} = \left[\frac{1}{\pi k_{epi} W_g} \ln\left(\frac{d + 2t_1}{L_g + t_1}\right) + \frac{t_2}{k_{\text{Sub}} W_g d}\right] \cdot P_{\text{loss}} + T_3 \tag{18}$$

where T_1 is the maximum junction/channel temperature, T_2 is the initial temperature and T_3 is assumed as ambient temperature (300 K). To verify the analytical model we have to consider the heat flux density calculated for the reference structure in Silvaco ATLAS software.[25] The simulated heat power ($1.78 \times 10^{16} W/m^3$) is applied to the heat source in COMSOL Multiphysics and the channel temperature is simulated. We observed a similar channel temperature using this. In addition, the modelled structure is simulated in Silvaco ATLAS and the corresponding heat power is calculated. The same heat power is applied to the heat source (in this case, the gate electrode) in COMSOL Multiphysics, as shown in Fig. 5a and b. Figure 5c and d illustrates the cross-sectional view of the temperature distribution around the heat source and temperature variations across the device length, respectively. Figure 6 shows the calculation of channel temperature for different parametric variations of (i) gate width variation, (ii) substrate thickness variation and (iii) epilayer thickness variation using the proposed analytical model and (iv) shows the enlarged view for gallium oxide epilayer over gallium oxide substrate. Thermal modelling has been carried out to determine the channel temperature with different variations in the device parameters. We observed that thermal resistance also increased with an increase in device parameters, hence leading to an increase in channel temperature as well. The analytical model data and simulation data are also compared to validate the analytical model as shown in Fig. 7, which shows close agreement with simulation data.

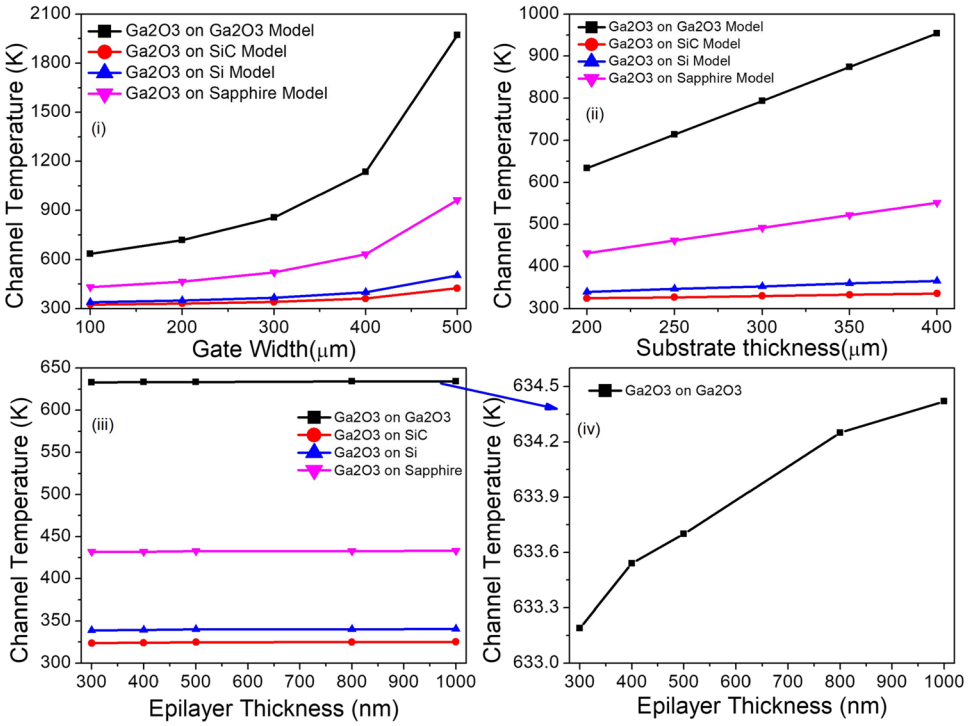

Fig. 6 Channel temperature calculation with different parametric variations using analytical model. (i) Gate width variation, (ii) substrate thickness variation, (iii) epilayer thickness variation, (iv) shows the enlarged view for gallium oxide epilayer over gallium oxide substrate.

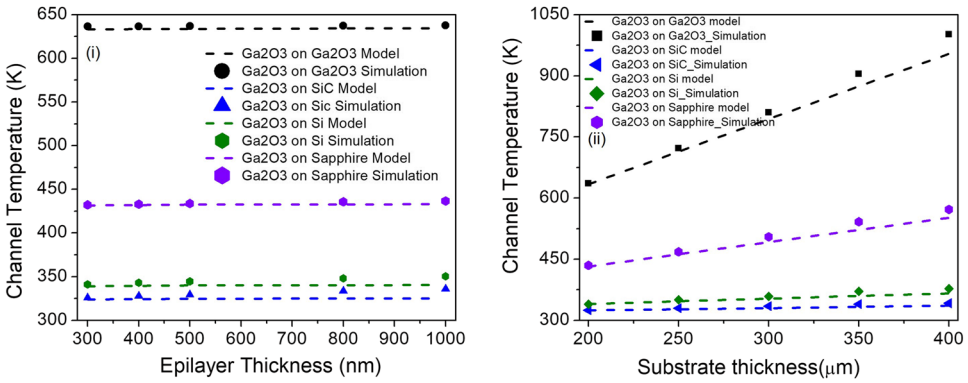

Fig. 7 Channel temperature calculation validation with COMSOL simulations. (i) Epilayer thickness variation, (ii) substrate thickness variation.

Table II Channel temperature calculation with different power and substrate structures

Substrate/ Power Dissipation	SiC Temp. (K)	Si Temp. (K)	Sapphire Temp. (K)	Ga2O3 Temp. (K)
0.25 W/mm	325.17	340.45	432.96	620.51
0.50 W/mm	350.35	380.91	565.93	968.86
0.75 W/mm	375.53	421.36	698.89	1303.29
1 W/mm	400.17	461.82	831.86	1637.72

These channel temperature calculations were conducted at 0.25 W/mm dissipated power. Table II shows the channel temperature variation with power dissipation of 0.25W/mm to 1 W/mm with varied substrate thickness. It can be observed that a foreign substrate with good thermal conductivity reduces the channel temperature and self-heating of gallium oxide-based devices to a great extent. This model can help device designers in choosing the device dimensions and predict the thermal properties of the designed devices.

Conclusion

An analytical model based on closed-form expressions is presented for gallium oxide-based FETs. This analytical model can be used to accurately determine the thermal resistance and channel temperature of the device. The Heat Transfer Module of the COMSOL Multiphysics standard finite element analysis tool is used to validate the model. As the low thermal conductivity of gallium oxide is the primary concern for device engineers, this model can be very useful for them to predict the thermal characteristics of the device for better performance and long durability.

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Author Contributions All authors contributed to the study conception and design. Material preparation, Design and simulation data collection and analysis were performed by Pharyanshu Kachhawa and Vaishali Chaudhary. The first draft of the manuscript was written by Pharyanshu Kachhawa. The conceptualization protocols, project monitoring and validation were done by Nidhi Chaturvedi. All authors read and approved the final manuscript.

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Code availability Not Applicable

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Ethics approval Not applicable

Consent to participate Not applicable

Consent for publication Not applicable

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