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Materials and Device Engineering for High-Performance Gallium Oxide Devices

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***Abstract*— Gallium Oxide is an ultra-wide band gap semiconductor that provides key benefits for high-performance power devices, including high electric breakdown field strength, good transport properties, well-controlled doping, and large-area melt-grown native substrates. The unique properties of this material also provide significant opportunities for heterostructure and device engineering. In this paper, we discuss some key advances toward achieving high-performance devices based on Gallium Oxide, and discuss future opportunities and challenges in this exciting area of research.**

Keywords— Gallium Oxide

I. Introduction

In the last decade there has been significant interest generated in Gallium Oxide (specifically, the monoclinic or β-phase of Gallium Oxide)[1,2,3,4]. The key electronic properties that make β-Ga_2O_3 promising for future devices include energy band gap in excess of 4.7 eV [2], an expected breakdown field strength of 8 MV/cm, and excellent control for n-type doping.

Table 1: Comparison of key material properties of semiconductors

	E_g (eV)	μ_n (cm^2/Vs)	E_c (MV/cm)	Baliga FOM
Si	1.1	1350	0.3	1
4H-SiC	3.2	900	2.5	320
GaN	3.4	1500	3	1400
β-Ga_2O_3	4.8	200	8	2400

The availability of melt-grown substrates [5] is a particular advantage since it enables low-defect density templates, with possibly low defect density in the future.

Table 1 shows some of the key material parameters and the Baliga Figure Of Merit [6], which is a measure of the suitability of different materials for power switching applications. Gallium Oxide shows comparable performance to Gallium Nitride, but provides the additional advantage of having melt-grown native substrates. One significant challenge is that since Schottky barriers cannot sustain the material breakdown field, new device designs will be necessary so that the internal fields can be scaled to achieve the maximum potential of Gallium Oxide.

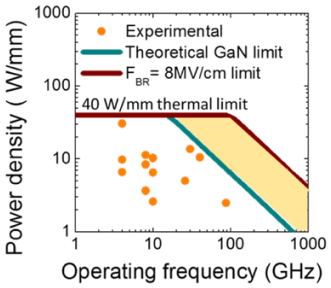

Fig. 1: Calculated and experimental output power density as a function of operating frequency. The experimental data points are from GaN AlGaN/GaN HEMTs

Another potential application for β-Ga_2O_3 electronics is high-power RF applications. The two most important parameters for RF amplifiers are power output density and maximum oscillation frequency. To estimate the transit time limited power density (P), we use an approximation for a Class A amplifier

$$P = \frac{I_{max} V_{br}}{8W}$$

where I_{max} is the maximum current density and V_{br} is the breakdown voltage of the transistor.

We can apply the relationship between the cutoff frequency

$$f_T = \frac{v_{sat}}{2\pi L_{GD}}$$

and the maximum oscillation frequency f_{MAX}:

$$f_{MAX} = f_T \sqrt{R_0 / R_{in}},$$

where R_0 and R_{in} are the real part of the output and input impedance. Recognizing that the operating frequency is related to the maximum oscillation frequency by $f = \frac{f_{MAX}}{G_P}$, where G_P is the power-gain, we can write the power density in terms of the operating frequency, and gain as:

$$P_{out} = \frac{I_{max} F_{br} v_{sat}}{16\pi W G_p f} \sqrt{\frac{R_0}{R_{in}}}$$

This allow us to predict performance of materials based their breakdown field and saturation velocity. The maximum

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theoretical output power density of GaN and β -Ga_2O_3 transistors can be calculated as a function of operation frequency (Fig.1). The breakdown field of GaN and β-Ga_2O_3 were assumed to be 3 MV/cm and 8 MV/cm, respectively. Electron saturation velocity of 1.5 x10^7 cm/s was set for GaN and 1x10^7 cm/s was set for β-Ga_2O_3. The experimental output power density results of GaN HEMTs (shown as orange dots) were also summarized. According to the calculation, GaN HEMTs can supply an output power density above 40 W/mm for applications that operate below 20 GHz. The maximum output power density decreases when GaN HEMTs are designed in the way to fulfill frequencies higher than 20 GHz. The predicted GaN HEMT power density is lower than 10 W/mm at frequencies above 70 GHz. β-Ga_2O_3, with high expected breakdown field and velocity, can provide a significant boost in the power density at frequencies above 70 GHz. Due to relatively low thermal conductivity, it is challenging for β-Ga_2O_3 transistors to be operated as Class A amplifiers to supply continuous high output power density within low frequency regime. With the large voltage-current product, β-Ga_2O_3 transistors potentially can be used on pulsed power amplifiers for simultaneous high power output, while a low average output power density can be retained for a safe thermal dissertation.

In the following sections, we discuss some key recent results related to Gallium Oxide lateral and vertical devices, including delta-doped transistors, modulation-doped transistors, and new methods for field management for Gallium Oxide vertical and lateral devices.

II. Delta Doped Gallium Oxide Transistors

Delta doped field effect transistors [7,8] are one possible approach to enable high sheet charge density in a scaled device. We review here recent results [9] demonstrating the high frequency performance in scaled delta-doped devices. The device structure (Fig. 2) used in this work was grown on (010) Fe-doped semi-insulating β -Ga_2O_3 substrates by O_2 plasma MBE. A silicon delta doped layer with Si concentration of 1.3 x 10^{13} cm^{-2} capped with 20 nm undoped Ga_2O_3 was grown on 450nm undoped buffer layer, and patterned regrown ohmic contacts [10] were used to make contact to the channel.

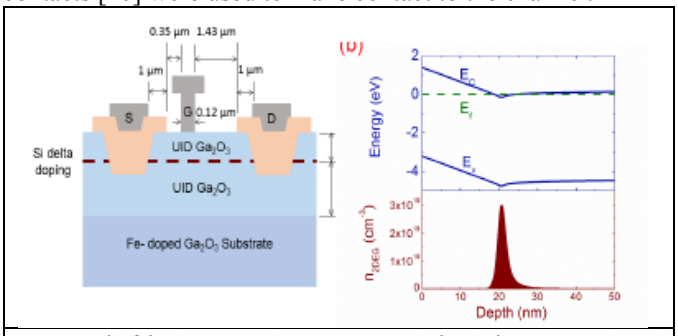

Fig. 2: (left) device schematic, and (right) energy band diagram for a delta-doped Gallium Oxide MESFET device [7,8]

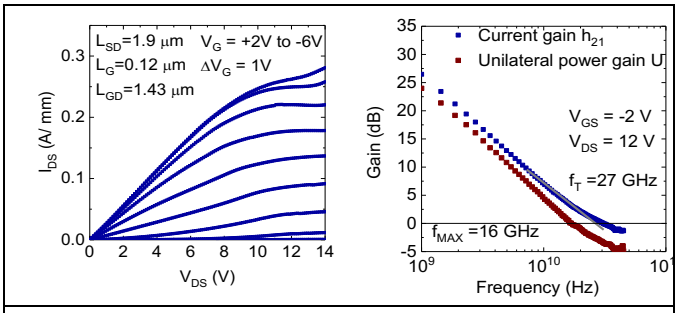

Fig. 3: I-V characteristics for a modulation-doped transistor, and (right) mobility and sheet charge density for various modulation-doped transistors [14]

Electron beam lithography was used to define a 120nm T-shaped gate (Fig. 2). A maximum DC drain current $I_{D,\,MAX}$ of 0.26 A/mm (Fig. 3) was measured at V_G =2 V and V_D =12 V, and a maximum transconductance gm_{max} of 44 mS/mm was measured at gate bias of -2.5 V. (Fig. 3) Using a drain current level of 0.1 mA/mm for breakdown, a breakdown voltage (V_{BR}) of 150 V was estimated in a 1.4 μm gate-drain spacing device. Peak f_T and f_{MAX} of 27 GHz and 16 GHz were obtained at V_G = -3 V and V_D = 12V. (Fig. 3). To estimate the device source resistance, source current was swept while the gate was forward biased reference to keep a 1 μA/mm forward current. The source resistance was estimated as the differential of the gate voltage with respect to source current. Based on this method, source resistance of 7.4 Ω mm was extracted. This resistance is significantly higher than that estimated from TLM measurement (3 Ω.mm), possibly due to surface depletion in the source access region. While this represents the highest frequency Gallium Oxide transistors to date, the frequency performance of the device is still considerably lower than that predicted based on simulations. Further investigation of the delay components in the device will help to engineer devices with better frequency performance.

III. Modulation Doped Transistors

We now discuss recent results on β -$(Al,Ga)_2O_3/Ga_2O_3$ modulation doped structures. Lateral β -Ga_2O_3 devices can enable superior performance if high sheet charge density can be achieved while maintaining good transport properties. This becomes a challenge in β-Ga_2O_3 with its inherently low bulk mobility (< 300 cm^2/V-s). $(Al,Ga)_2O_3/Ga_2O_3$ MODFETS [11,12] offer a possible solution to this problem as they can enable a 2D electron gas with enhanced mobility. $(AlGa)_2O_3/Ga_2O_3$ MODFETs with high mobility (180 cm^2/V-s) have been demonstrated [13] but these devices are limited to low sheet charge density (~2x10^{12} cm^{-2}) due to the low conduction band offset between $(AlGa)_2O_3$ and Ga_2O_3.

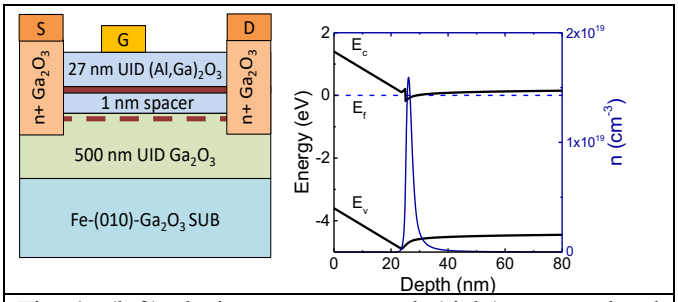

Fig 4: (left) device structure, and (right) energy band diagram and electron density profile for a thin-spacer modulation-doped structure [14]

We discuss recent work on increasing the sheet charge density by utilizing a thin spacer thickness of 1 nm [14]. The aggressive scaling of the spacer layer is not expected to significantly affect the 2DEG mobility since room temperature mobility is dominated by inherent polar optical phonon scattering [15].

The epitaxial stack reported here consists of 500 nm buffer layer of UID Ga_2O_3, 1nm spacer layer of $(Al,Ga)_2O_3$, Si delta doping (1 monolayer thick) followed by 25 nm $(Al,Ga)_2O_3$ on Tamura (010) Fe-doped substrates Fig. 4). The Al composition of 18% was confirmed from peak separation in high-resolution X-ray diffraction measurements. Ohmic contacts were realized using MBE-regrowth followed by deposition of Ti/Au metal stack while Pt/Au was utilized as schottky contacts.

Hall mobility and sheet charge density were measured to be 148 $cm^2/V\text{-}s$ and 5.1×10^{12} cm^{-2}, respectively. C-V measurements show a flat profile with integrated sheet charge density of 6×10^{12} cm^{-2}. Effective drift mobility was measured as a function of gate bias by extracting the drain conductance (g_d) on large gate length devices (100 μm), and had a peak value of 140 $cm^2/V\text{-}s$. Comparison with theoretical mobility calculations reveal that polar optical phonon scattering is the limiting factor in determining mobility at high sheet charge density, with small contribution from remote ionized impurity scattering at low carrier density. This confirms our hypothesis that thin spacer layers do not have a significant detrimental effect in the case of $(Al,Ga)_2O_3/Ga_2O_3$ heterostructures, and that the electrons reside primarily in the Ga_2O_3 channel layer. Previous reports on high sheet charge density β - $(Al,Ga)_2O_3/Ga_2O_3$ structures showed freeze-out of some fraction of the electron gas at low temperatures, which was attributed to parallel conduction in the barrier layer. In this case, the sheet charge density was found to be insensitive to temperature down to 80 K (measurement not shown), suggesting the absence of parallel conduction.

Output characteristics of transistors (L_g=0.7 um, L_{gd}=1.4 um, L_{sd}=1 um) show a peak drain current of 130 mA/mm (Figure 5) which is the highest reported in a single channel $(Al,Ga)_2O_3/Ga_2O_3$ MODFET device. A peak extrinsic transconductance (g_m) of 35 mS/mm was also measured. The three terminal breakdown voltage was measured to be 180 V. The high sheet charge density modulation-doped structures could provide a pathway toward future high-performance lateral Gallium Oxide device structures.

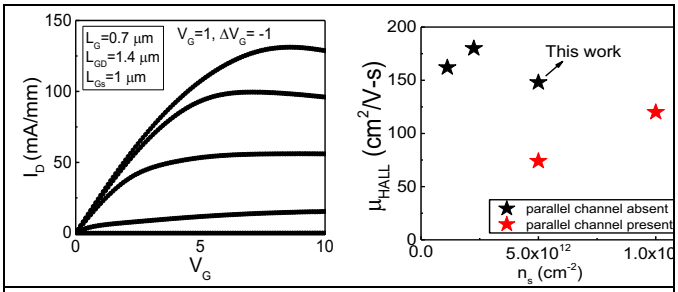

Fig. 5: Output IV characteristics for thin-spacer modulation doped transistors, and literature for mobility and sheet charge density in modulation-doped transistors [14]

IV. High Permittivity Dielectrics

The large breakdown electric field (6-8 MV/cm) of Ga_2O_3 and make it a promising material for power electronics. Due to the absence of a p-type dopant, the maximum breakdown field in vertical β-Ga_2O_3 devices is limited by the Schottky barrier height, and gate leakage. β-Ga_2O_3 planar Schottky diodes demonstrated to date show maximum breakdown fields below 3.5 MV/cm. Recently, we demonstrated [16] heterojunction engineering with extreme dielectric constant materials on semiconductors to achieve high breakdown and low on-resistance that approaches or exceeds ideal PN junction resistance. Proof-of-concept experimental data is presented to show that high reverse breakdown electric fields (5.7 MV/cm) can be achieved using this method.

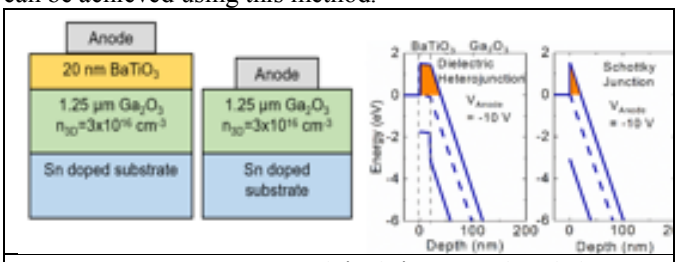

Fig 6: Device structure, and (right) energy band diagram under bias for a $BaTiO_3/Ga_2O_3$ and a Schottky diode, respectively. The higher permittivity of the $BaTiO_3$ layer enables a flat conduction band profile and higher barrier to metal-semiconductor tunneling.

The design principle of this device is as follows (Fig. 6). Ga_2O_3 Schottky barriers display reverse breakdown due to tunneling across the Schottky barrier at fields (typically ~3 MV/cm) that are significantly lower than breakdown field of Ga_2O_3 (>7 MV/cm). In the case of $BaTiO_3$/ Ga_2O_3 dielectric heterojunction, the dielectric constant discontinuity (ratio ~ 29) leads to a very low electric field in $BaTiO_3$.

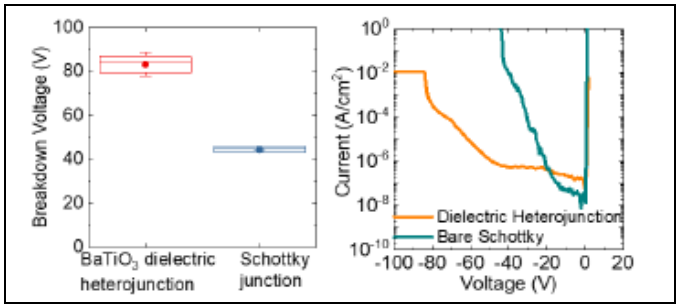

Fig 7: (left) ensemble, and (b) typical breakdown performance for dielectric heterojunction and bare Schottky devices.

The $BaTiO_3$ electron barrier stays almost flat under reverse bias. Therefore, the $BaTiO_3$/ Ga_2O_3 dielectric heterojunction maintains a barrier to electron tunneling at much higher voltages than the metal/semiconductor junction. Under forward bias, electrons must flow from the semiconductor, through the

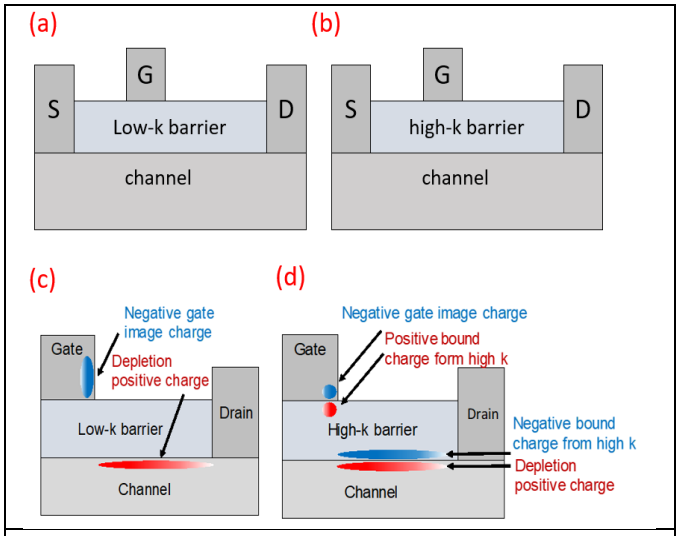

Fig 8: Schematics showing the impact of permittivity on the electrostatics in a lateral transistor structure.

high dielectric constant layer, into the metal. For small values of conduction band offset between $BaTiO_3$/ Ga_2O_3 (as predicted from the electron affinity difference) dielectric heterojunction is expected to support efficient transport.

To characterize the breakdown field of the dielectric heterojunction without additional field termination processes, we fabricated Schottky diodes with relatively thin drift regions consisting of 150 nm UID Ga_2O_3 on n-type substrates. Schottky diodes consisting of Pt/150 nm UID Ga2O3/n-type substrate were fabricated, and compared with dielectric heterojunction diodes consisting of Pt/$BaTiO_3$/Ga_2O_3/n-type substrate. The Schottky barrier diode had typical breakdown voltage of 45 V (maximum field 3.4 MV/cm), while the dielectric heterojunction diode showed significantly higher breakdown voltage of 85 V (maximum field 5.7 MV/cm). This is the highest parallel-plate breakdown field reported for any Ga_2O_3 vertical device. 2D device simulations show when the electric field at the center of the device is 5.67 MV/cm , the edge of the device is expected to have an electric field of 7 MV/cm. However, the electric field in $BaTiO_3$ remains very low 0.2 MV/cm as expected from the dielectric discontinuity. Preliminary investigation suggests the breakdown is due to interband tunneling between the $BaTiO_3$ and Ga_2O_3. The dielectric heterojunction idea demonstrated here provides a promising pathway toward realizing high-breakdown field, high-performance power device topologies that can exploit the full potential of Gallium Oxide without the need for p-type doping.

V. DIELECTRIC SUPERJUNCTION TRANSISTORS

In the previous section, $BaTiO_3$/Ga_2O_3 dielectric heterojunctions show the potential show support a peak electric field above 5.7 MV/cm. High permittivity dielectrics can also help to engineer electrical fields and make them more uniform profile in lateral diodes and transistors. The conventional approach to manage electric fields in lateral devices involve field plates or complementarily doped layers (such as RESURF). Achieving the optimal electric field profile using field plates is usually not practically feasible since it requires three-dimensional shaping of the field plate. Also, field plates increase the gate-drain capacitance and degrade the cutoff frequency devices. Superjunction and RESURF designs using p-type layers have been used for Si devices to surpass the unipolar figure of merit. However, such field termination structures may not be feasible material systems like Gallium Oxide where p-type doping is less efficient or controllable. In this section, dielectric superjunction transistors that use high permittivity dielectrics is introduced for field management in semiconductor devices.

Table 2: Material parameters used for simulations.

Material	$SrTiO_3$	β-Ga_2O_3
Band gap (eV)	3.2	4.7
Dielectric constant	300	10
Effective mass	1.8	0.2
Electron mobility (cm^2/Vs)	10	300
Saturation velocity (cm/s)	$1x10^7$	$1x10^7$

The concept of the dielectric superjunction transistor [17] is illustrated in Figure 9. In the gate-drain region of a field effect transistor in pinched-off condition, net positive charges are induced in the gate-drain region. In a conventional field effect transistor (without a high permittivity dielectric), these positive charges are imaged on the gate metal edge on the drain side and lead to a non-uniform lateral electric distribution with a peak near the gate-drain edge. When a high permittivity dielectric is introduced, due to large permittivity differences between channel and barrier layer, the electric field leads to a gradient in the dielectric polarization in the high permittivity layer and therefore a net negative bound polarization charge. The excess net negative polarization bound charges (shown in blue) are induced at the high k/ low k interface in the depleted region. The negative polarization bound charge comes from the electric dipole of dielectric material. Thus, a net positive polarization bound charge is induced below the drain edge of the gate in the high k barrier. As a result, the field due to the negative bound

charge compensates that from the positive charge in the depletion region, reducing the electric field profile, and making the electric field flat. This high permittivity field management is analogous to a conventional superjunction design where the equal number of p- and n- dopants are used to compensate each other, leading to a flat electric field [REF] and the breakdown voltage becomes less dependent on the sheet charge density.

To quantitively estimate the potential of this concept, device simulations were performed using a 2D device simulator Silvaco. A schematic of a heterostructure is shown in Figure 10. It consists of a β-Ga_2O_3 delta-doped MESFET with $1x10^{13}$ cm^{-2} sheet charge density and a 20 nm high-k material barrier layer ($SrTiO_3$).

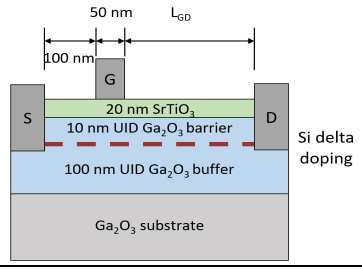

Fig 9: Schematic of device used for simulation of the high permittivity dielectric superjunction transistor.

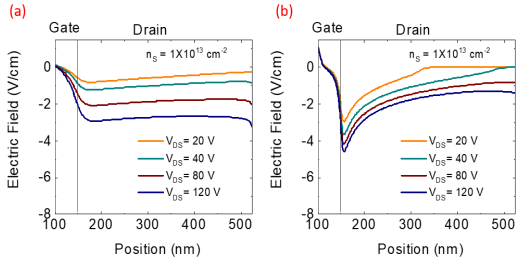

Fig 10: Electric field profiles along the channel (from gate to drain) for a structure with (a) high permittivity, and (b) low permittivity dielectric barrier, showing the uniform field profiles enabled by the high permittivity barrier layer.

The material constants assumed for these simulations are shown in Table 3. A control structure with $SrTiO_3$ replaced with low permittivity barrier material (ε_r = 10) was also simulated. Contact resistance 0.1 Ω.mm is assumed. The off-state breakdown scenarios were simulated for both structures. Negative gate bias was applied to pinch off the device. The lateral electric field at various drain bias in channel region was extracted, as shown in Figure 11. The low permittivity barrier devices have a large peak lateral field at the gate edge on the drain side. On the other hand, the dielectric superjunction transistor showed a nearly uniform electric profile at a charge density of $1x10^{13}$ cm^{-2}. Assuming the breakdown field of 5 MV /cm, the dielectric heterojunction transistors breakdown at 300 V and the control device breakdown at 120 V. The dielectric superjunction transistor showed nearly 3 times higher breakdown field.

Recent work along these lines has enabled us to achieve excellent characteristics from Gallium Oxide-based transistors. In Figure 11, we show $BaTiO_3/Ga_2O_3$ transistors based on a double heterojunction modulation doped structure.

Using a composite dielectric layer consisting of a high-k/low-k heterojunction overlapped over the gate electrode. Utilizing this strategy in β-Ga_2O_3 double heterojunction field effect transistor helped achieve a record average breakdown field of 5.7 MV/cm at a gate-drain spacing of 1.1μm along with an improved power figure of merit performance of 586 MW/cm^2. The sheet charge density below the gate in this structure was measured to be $2x10^{13}cm^{-2}$. This shows the effectiveness of integrating high-k dielectrics with ultra-wide band gap materials in significantly improving breakdown performance.

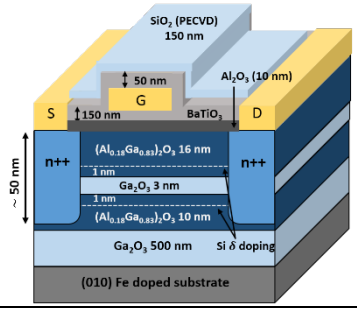

Fig 11: Cross sectional diagram of the epitaxial and device structure for a high-permittivity/Ga_2O_3 transistor. Average breakdown fields up to 5.7 MV/cm over 1.1 μm were obtained in this device,

VI. Summary

This paper discusses some of the recent advances in the area of Gallium Oxide devices, and outlines some future pathways toward achieving high-performance electronics. While significant performance gains have been made in the last years through device engineering, there are many opportunities for improving the device parameters. Novel device engineering methods for epitaxial design, as well as for field engineering will play a critical role in enabling Gallium Oxide electronic devices to reach their full potential.

Acknowledgment

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