Bacharelado em Ciência da Computação – DINF / UFPR
CI 068 – Circuitos Digitais
3ª Lista de Exercícios – 27/05/2011

Data de Entrega: 08/06/2011

Exercise 3.1 Given the input waveforms shown in Figure 3.59, sketch the output, Q, of an SR latch.

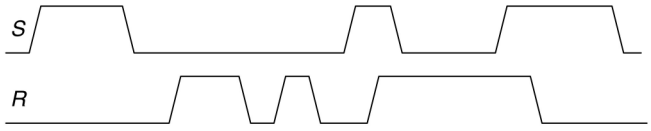

Figure 3.59 Input waveform of SR latch

Exercise 3.2 Given the input waveforms shown in Figure 3.60, sketch the output, Q, of a D latch.

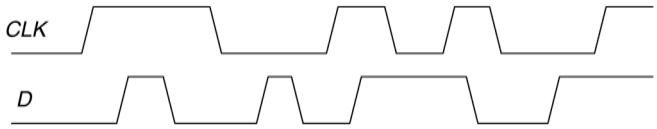

Figure 3.60 Input waveform of D latch or flip-flop

Exercise 3.10 Design an asynchronously resettable D flip-flop using logic gates.

Exercise 3.12 Design an asynchronously settable D flip-flop using logic gates.

Exercise 3.19 Describe in words what the state machine in Figure 3.65 does. Using binary state encodings, complete a state transition table and output table for the FSM. Write Boolean equations for the next state and output and sketch a schematic of the FSM.

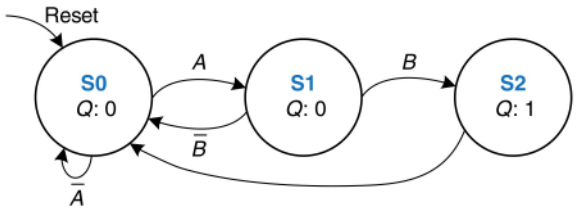

Figure 3.65 State transition diagram

Exercise 3.20 Describe in words what the state machine in Figure 3.66 does. Using binary state encodings, complete a state transition table and output table for the FSM. Write Boolean equations for the next state and output and sketch a schematic of the FSM.

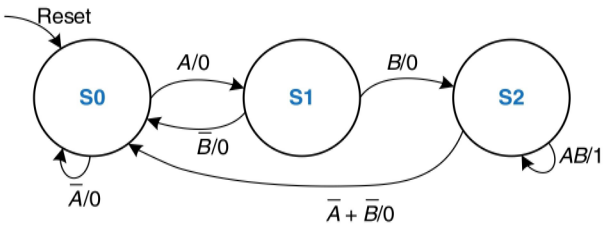

Figure 3.66 State transition diagram

Exercise 3.24 Gray codes have a useful property in that consecutive numbers differ in only a single bit position. Table 3.17 lists a 3-bit Gray code representing the numbers 0 to 7. Design a 3-bit modulo 8 Gray code counter FSM with no inputs and three outputs. (A modulo N counter counts from 0 to $N-1$, then repeats. For example, a watch uses a modulo 60 counter for the minutes and seconds that counts from 0 to 59.) When reset, the output should be 000. On each clock edge, the output should advance to the next Gray code. After reaching 100, it should repeat with 000.

Table 3.17 3-bit Gray code

Number	Gray code		
0	0	0	0
1	0	0	1
2	0	1	1
3	0	1	0
4	1	1	0
5	1	1	1
6	1	0	1
7	1	0	0

Exercise 3.26 Your company, Detect-o-rama, would like to design an FSM that takes two inputs, A and B, and generates one output, Z. The output in cycle n, Z_n, is either the Boolean AND or OR of the corresponding input A_n and the previous input A_{n-1}, depending on the other input, B_n:

$$Z_n = A_n \, A_{n-1} \quad \text{if } B_n = 0$$
$$Z_n = A_n + A_{n-1} \text{ if } B_n = 1$$

(a) Sketch the waveform for Z given the inputs shown in Figure 3.67.

(b) Is this FSM a Moore or a Mealy machine?

(c) Design the FSM. Show your state transition diagram, encoded state transition table, next state and output equations, and schematic.

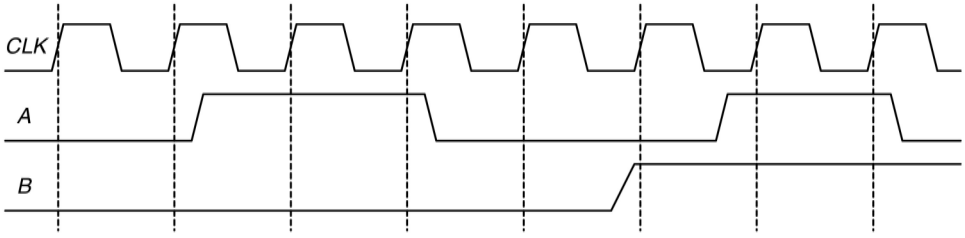

Figure 3.67 FSM input waveforms

Exercise 3.28 Analyze the FSM shown in Figure 3.68. Write the state transition and output tables and sketch the state transition diagram. Describe in words what the FSM does.

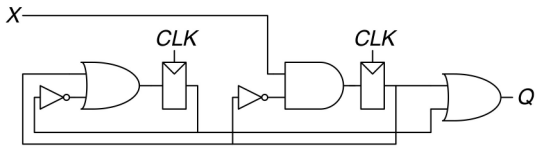

Figure 3.68 FSM schematic

Exercício 10 Um flip-flop JK possui duas entradas (J e K), além do clock, e apresenta o seguinte comportamento:

J	K	Q(t+1)	
0	0	Q(t)	No Change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Complement

Projeto um flip-flop JK utilizando um flip-flop D e portas lógicas.

Exercício 11 Um flip-flop T possui apenas uma entrada (T), além do clock, e apresenta o seguinte comportamento. Se a entrada T for 0, a saída mantém-se no valor atual. Se a entrada T for 1, o novo estado será o complemento do estado atual. Projete um flip-flop T utilizando um flip-flop JK.

Exercício 12 Refaça o exercício 3.19 utilizando FF's JK.

Exercício 13 Refaça o exercício 3.20 utilizando FF's T.