DG645 Specifications

Delays

Channels	4 independent pulses controlled in position and width. 8 delay channels available as an option (see *Output Options*).
Range	0 to 2000 s
Resolution	5 ps
Accuracy	1 ns + (timebase error × delay)
Jitter (rms)	
Ext. trig. to any output	25 ps + (timebase jitter × delay)
T_0 to any output	15 ps + (timebase jitter × delay)
Trigger delay	85 ns (ext. trig. to T_0 output)

Timebases

Model #	Type	Jitter *(s/s)*	Stability *(20 to 30 °C)*	Aging *(ppm/yr)*
Std.	crystal	10^{-8}	2×10^{-6}	5
Opt. 4	OCXO	10^{-11}	1×10^{-9}	0.2
Opt. 5	Rb	10^{-11}	1×10^{-10}	0.0005

External input	10 MHz ± 10 ppm, sine >0.5 Vpp, 1 kΩ impedance
Output	10 MHz, 2 Vpp sine into 50 Ω

External Trigger

Rate	DC to 1/(100 ns + longest delay) (maximum of 10 MHz)
Threshold	±3.50 VDC
Slope	Trigger on rising or falling edge
Impedance	1 MΩ + 15 pF

Internal Rate Generator

Trigger modes	Continuous, line or single shot
Rate	100 µHz to 10 MHz
Resolution	1 µHz
Accuracy	Same as timebase
Jitter (rms)	<25 ps (10 MHz/N trigger rate) <100 ps (other trigger rates)

Burst Generator

Trigger to first T_0	
Range	0 to 2000 s
Resolution	5 ps
Period between pulses	
Range	100 ns to 42.9 s
Resolution	10 ns
Delay cycles per burst	1 to $2^{32} - 1$

Outputs (T_0, AB, CD, EF, and GH)

Source impedance	50 Ω
Transition time	<2 ns
Overshoot	<100 mV + 10 % of pulse amplitude
Offset	±2 V
Amplitude	0.5 to 5.0 V (level + offset <6.0 V)
Accuracy	100 mV + 5 % of pulse amplitude

General

Computer interfaces	GPIB (IEEE-488.2), RS-232, and Ethernet. All instrument functions can be controlled through the interfaces.
Non-volatile memory	Nine sets of instrument configurations can be stored and recalled.
Power	<100 W, 90 to 264 VAC, 47 Hz to 63 Hz
Dimensions	8.5" × 3.5" × 13" (WHD)
Weight	9 lbs.
Warranty	One year parts and labor on defects in materials & workmanship

Output Options

Option 01 (8 Delay Outputs on Rear Panel)

Outputs (BNC)	T_0, A, B, C, D, E, F, G and H
Source impedance	50 Ω
Transition time	<1 ns
Overshoot	<100 mV
Level	+5 V CMOS logic
Pulse characteristics	
Rising edge	At programmed delay
Falling edge	25 ns after longest delay

Option 02 (8 High-Voltage Delay Outputs on Rear Panel)

Outputs (BNC)	T_0, A, B, C, D, E, F, G and H
Source impedance	50 Ω
Transition time	<5 ns
Levels	0 to 30 V into high impedance 0 to 15 V into 50 Ω (amplitude decreases by 1 %/kHz)
Pulse Characteristics	
Rising Edge	At programmed delay
Falling Edge	100 ns after the rising edge

Option 03 (Combinatorial Outputs on Rear Panel)

Outputs (BNC)	T_0, AB, CD, EF, GH, (AB + CD), (EF + GH), (AB + CD + EF), (AB + CD + EF + GH)
Source impedance	50 Ω
Transition time	<1 ns
Overshoot	<100 mV + 10 % of pulse amplitude
Pulse characteristics	
T_0, AB, CD, EF, GH	Logic high for time between delays
(AB + CD), (EF + GH)	Two pulses created by the logic OR of the given channels
(AB + CD + EF)	Three pulses created by the logic OR of the given channels
(AB + CD + EF + GH)	Four pulses created by the logic OR of the given channels

Option SRD1 (Fast Rise Time Module)

Rise time	<100 ps
Fall time	<3 ns
Offset	0.8 V to 1.1 V
Amplitude	0.5 V to 5.0 V
Load	50 Ω