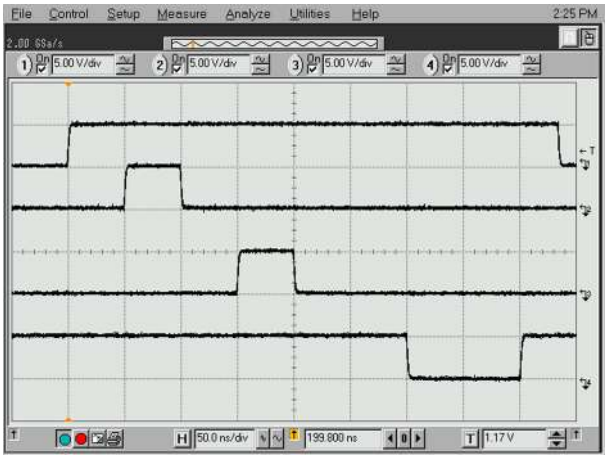
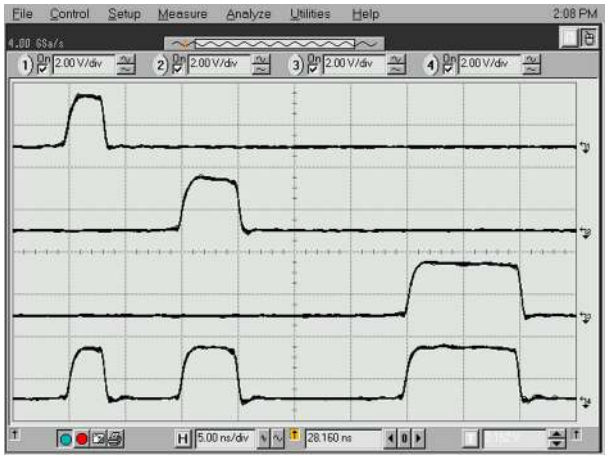


Front-panel outputs (50 ns/div)



Combinatorial outputs showing 3 ns, 5 ns and 10 ns pulses with 1 ns transition times (5 ns/div)

from 100 µHz to 10 MHz with 1 µHz resolution. An external trigger input, with adjustable threshold and slope, can trigger a timing cycle, a burst of cycles, or a single shot. A single shot can be triggered with a key press. A line trigger operates synchronously with the AC mains. A rear-panel trigger inhibit input can disable the trigger or any of the pulse outputs during a timing cycle.

The DG645 supports a number of complex triggering requirements via a trigger holdoff and prescaling feature.

Trigger holdoff sets the minimum time between successive triggers. This is useful if a trigger event in your application generates a significant noise transient that needs time to decay away before the next trigger is generated. Trigger holdoff can also be used to trigger the DG645 at a sub-multiple of the input trigger rate.

Trigger prescaling enables the DG645 to be triggered synchronously with a much faster source, but at a sub-multiple of the original trigger frequency. For example, the DG645 can be triggered at 1 kHz, but synchronously with a mode locked laser running at 80 MHz, by prescaling the trigger input by 80,000. Furthermore, the DG645 also contains a separate prescaler for each front-panel output, enabling each output to operate at a sub-multiple of the trigger rate.

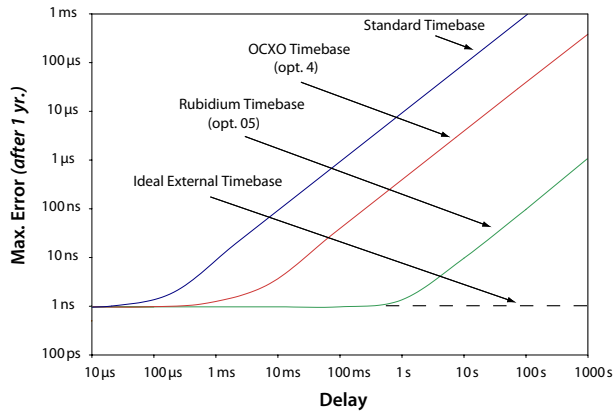
Front-Panel Outputs

There are five front-panel outputs: T_0, AB, CD, EF and GH. The T_0 output is asserted for the duration of the timing cycle. The leading edge of T_0 is the zero time reference. The programmed delays (A, B, C, D, E, F, G and H) are set from 0 s to 2000 s, with 5 ps resolution, to control the timing of the leading and trailing edges of the four pulse outputs.

Each front-panel output can drive a 50 Ω load and has a 50 Ω source impedance. Output amplitudes can be set from 0.5 to 5.0 V, and output offsets can range over ±2 VDC to source virtually any logic level (NIM, ECL, PECL, CMOS, etc.). Output transition times are less than 2 ns at any output amplitude.

Rear-Panel Outputs

Optional rear-panel outputs are available to support diverse applications. Option 01 provides a T_0 output and eight programmed delays (A, B, C, D, E, F, G and H) at 5 V logic levels, with transition times less than 1 ns. Option 02 provides these same outputs but as 30 V, 100 ns pulses with less than 5 ns transition times for timing distribution in high noise environments. Option 03 provides eight combinatorial outputs which deliver one to four pulses at 5 V logic levels with less than 1 ns transition times. Each output has a 50 Ω source impedance.



Timing error vs. programmed delay