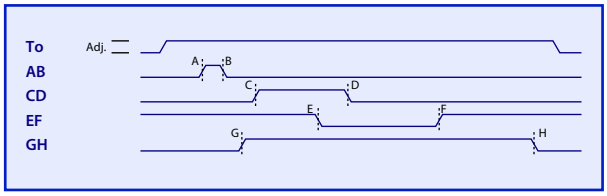
SRS Tech Note

More About the Outputs

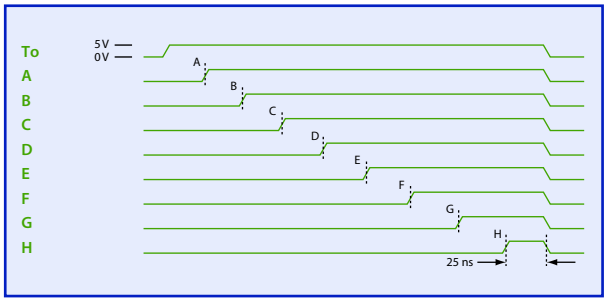
A timing cycle is initiated by an internal or external trigger. The T_0 output, whose leading edge is the zero-time reference, is asserted 85 ns after the trigger. The delay settings (A, B, C, D, E, F, G and H) determine the timing of the front-panel and rear-panel outputs.

The front-panel outputs have adjustable amplitude, offset, and polarity (non-inverted or inverted).



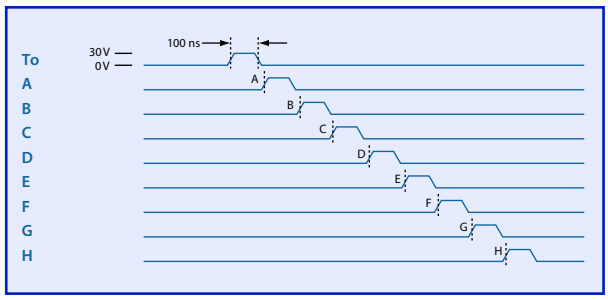
Front-panel outputs (adjustable)

Option 01 rear-panel outputs provide T_0 and eight delay outputs (A, B, C, D, E, F, G and H) to allow the DG645 to be used as an 8-channel delay generator. The outputs go from 0 to 5 V at their programmed delays, and return low 25 ns after the longest delay.



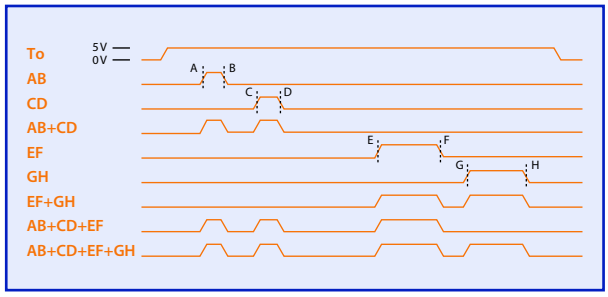
Opt. 01 rear-panel outputs (5 V)

Option 02 rear-panel outputs provide 30 V, 100 ns timing pulses at T_0, A, B, C, D, E, F, G and H. Output amplitudes are reduced to 15 V when driving 50 Ω loads.



Opt. 02 rear-panel outputs (30 V)

Option 03 rear-panel outputs provide outputs T_0, AB, CD, EF, GH (with the same definition as the front-panel outputs), and (AB+CD), (EF+GH), (AB+CD+EF), (AB+CD+EF+GH) which provide two, three, or four pulses per trigger.



Opt. 03 rear-panel combinatorial outputs (5 V)

DG645 rear panel with Opt. 01 outputs