
STM32
CubeMX

1. Description

1.1. Project

Project Name	AMC
Board Name	custom
Generated with:	STM32CubeMX 6.3.0
Date	11/16/2021

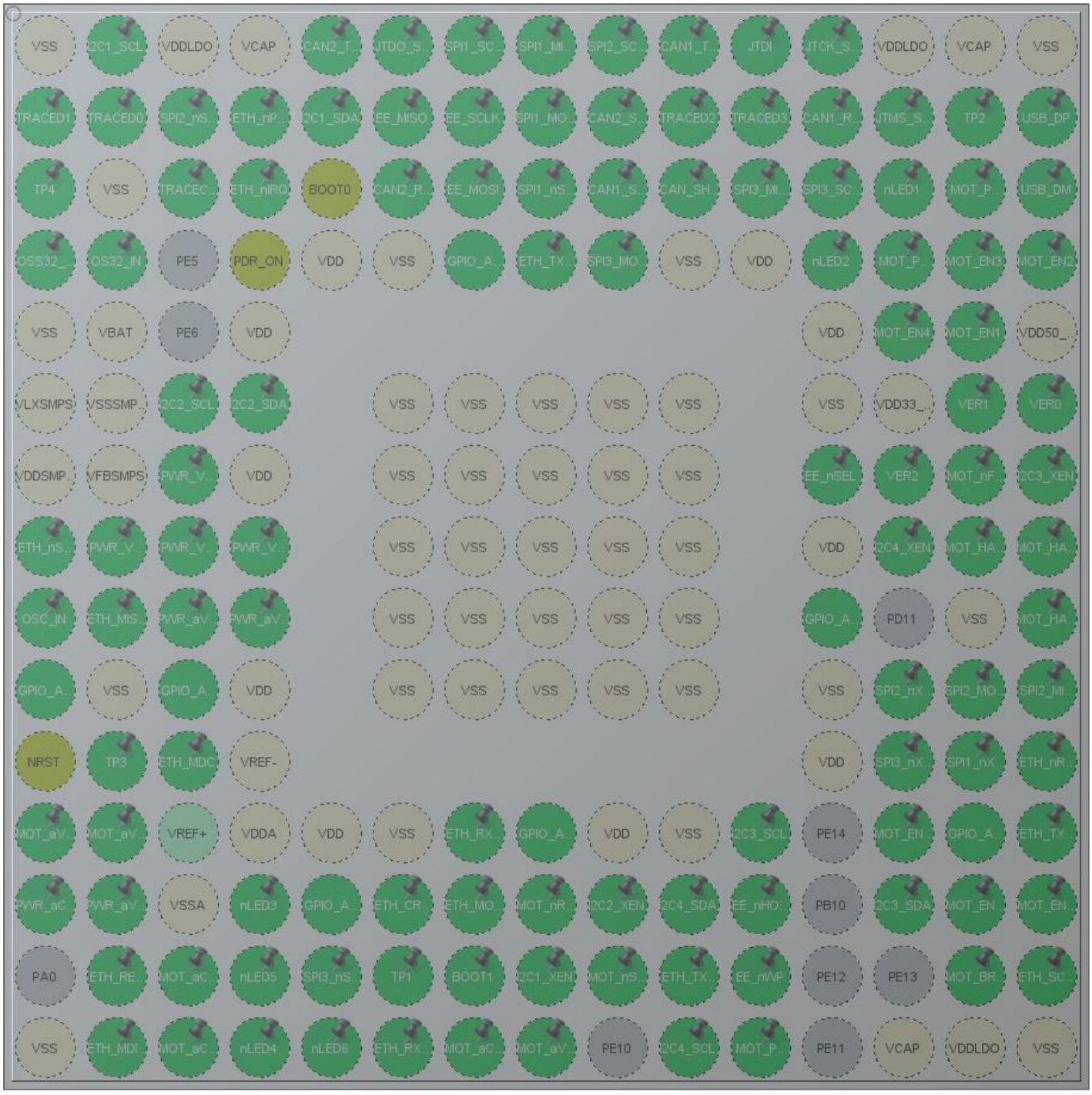
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H745/755
MCU name	STM32H745IIKx
MCU Package	UFBGA176
MCU Pin number	201

1.3. Core(s) information

Core(s)	ARM Cortex-M7 ARM Cortex-M4

2. Pinout Configuration



UFBGA176 +25 (Top view)

3. Pins Configuration

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	VSS	Power		
A2	PB8	I/O	I2C1_SCL	I2C1_SCL
A3	VDDLDO	Power		
A4	VCAP	Power		
A5	PB6	I/O	FDCAN2_TX	CAN2_TXD
A6	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	JTDO_SWO
A7	PG11	I/O	SPI1_SCK	SPI1_SCLK
A8	PG9	I/O	SPI1_MISO	SPI1_MISO
A9	PD3	I/O	SPI2_SCK	SPI2_SCLK
A10	PD1	I/O	FDCAN1_TX	CAN1_TXD
A11	PA15 (JTDI)	I/O	DEBUG_JTDI	JTDI
A12	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	JTCK_SWCK
A13	VDDLDO	Power		
A14	VCAP	Power		
A15	VSS	Power		
B1	PE4	I/O	DEBUG_TRACED1	TRACED1
B2	PE3	I/O	DEBUG_TRACED0	TRACED0
B3	PB9	I/O	SPI2_NSS	SPI2_nSEL
B4	PE0	I/O	GPIO_EXTI0	ETH_nPME
B5	PB7	I/O	I2C1_SDA	I2C1_SDA
B6	PB4 (NJTRST)	I/O	SPI6_MISO	EE_MISO
B7	PG13	I/O	SPI6_SCK	EE_SCLK
B8	PD7	I/O	SPI1_MOSI	SPI1_MOSI
B9	PD5 *	I/O	GPIO_Output	CAN2_STBY
B10	PD2	I/O	DEBUG_TRACED2	TRACED2
B11	PC12	I/O	DEBUG_TRACED3	TRACED3
B12	PH14	I/O	FDCAN1_RX	CAN1_RXD
B13	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	JTMS_SWDIO
B14	PA8	I/O	RCC_MCO_1	TP2
B15	PA12	I/O	USB_OTG_FS_DP	USB_DP
C1	PC13 *	I/O	GPIO_Output	TP4
C2	VSS	Power		
C3	PE2	I/O	DEBUG_TRACECLK	TRACECLK
C4	PE1	I/O	GPIO_EXTI1	ETH_nIRQ
C5	BOOT0	Boot		
C6	PB5	I/O	FDCAN2_RX	CAN2_RXD

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
C7	PG14	I/O	SPI6_MOSI	EE_MOSI
C8	PG10	I/O	SPI1_NSS	SPI1_nSEL
C9	PD4 *	I/O	GPIO_Output	CAN1_STBY
C10	PD0 *	I/O	GPIO_Output	CAN_SHDN
C11	PC11	I/O	SPI3_MISO	SPI3_MISO
C12	PC10	I/O	SPI3_SCK	SPI3_SCLK
C13	PH13 *	I/O	GPIO_Output	nLED1
C14	PA10	I/O	TIM1_CH3	MOT_PWM3
C15	PA11	I/O	USB_OTG_FS_DM	USB_DM
D1	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	OSS32_OUT
D2	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	OS32_IN
D4	PDR_ON	Reset		
D5	VDD	Power		
D6	VSS	Power		
D7	PG15 *	I/O	GPIO_Analog	
D8	PG12	I/O	ETH_TXD1	
D9	PD6	I/O	SPI3_MOSI	SPI3_MOSI
D10	VSS	Power		
D11	VDD	Power		
D12	PH15 *	I/O	GPIO_Output	nLED2
D13	PA9	I/O	TIM1_CH2	MOT_PWM2
D14	PC8 *	I/O	GPIO_Output	MOT_EN3
D15	PC7 *	I/O	GPIO_Output	MOT_EN2
E1	VSS	Power		
E2	VBAT	Power		
E4	VDD	Power		
E12	VDD	Power		
E13	PC9 *	I/O	GPIO_Output	MOT_EN4
E14	PC6 *	I/O	GPIO_Output	MOT_EN1
E15	VDD50_USB	Power		
F1	VLXSMPS	Power		
F2	VSSSMPS	Power		
F3	PF1	I/O	I2C2_SCL	I2C2_SCL
F4	PF0	I/O	I2C2_SDA	I2C2_SDA
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		

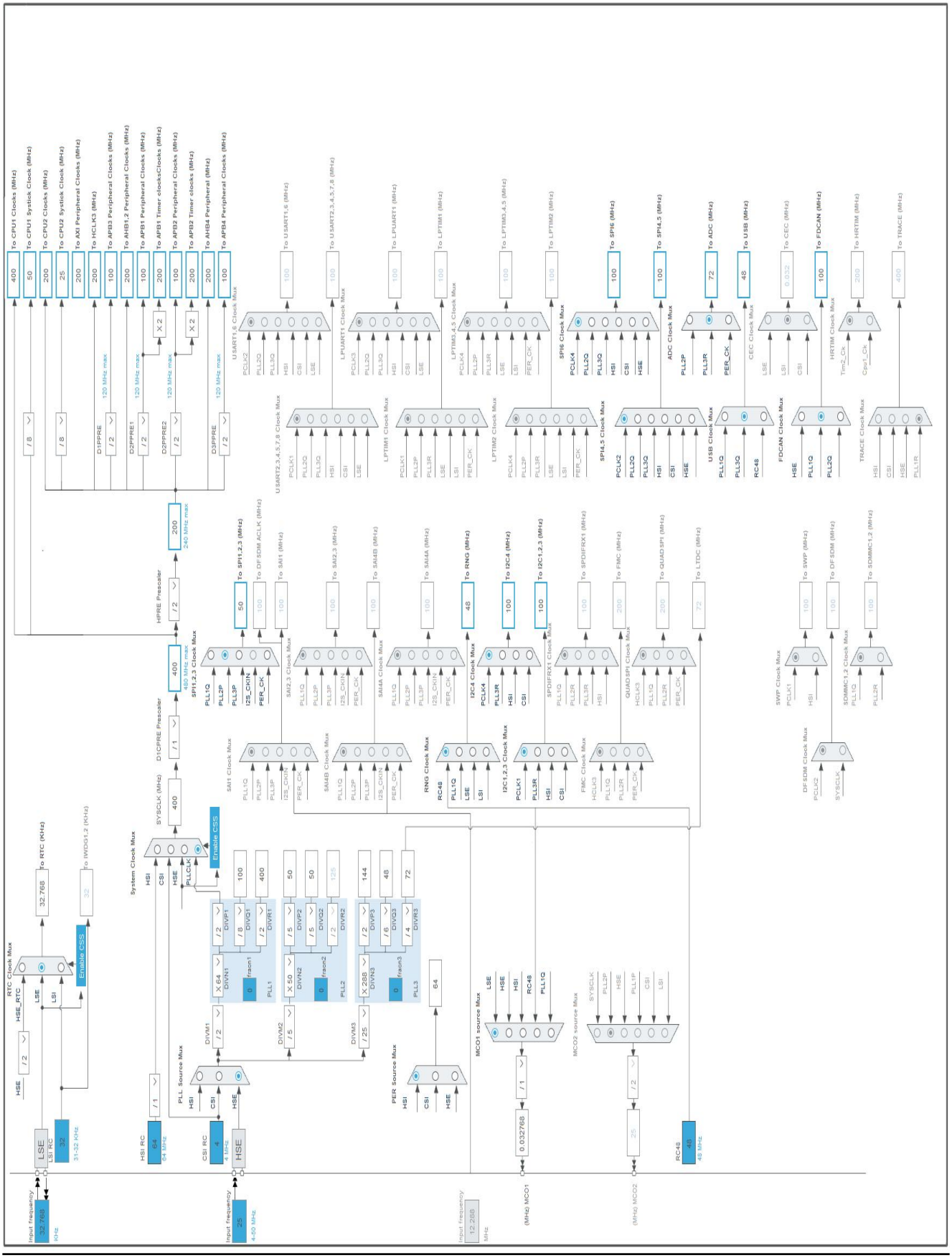
Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
F10	VSS	Power		
F12	VSS	Power		
F13	VDD33_USB	Power		
F14	PG6 *	I/O	GPIO_Input	VER1
F15	PG5 *	I/O	GPIO_Input	VER0
G1	VDDSMPS	Power		
G2	VFBSMPS	Power		
G3	PF2	I/O	GPIO_EXTI2	PWR_VCCOK
G4	VDD	Power		
G6	VSS	Power		
G7	VSS	Power		
G8	VSS	Power		
G9	VSS	Power		
G10	VSS	Power		
G12	PG8 *	I/O	GPIO_Output	EE_nSEL
G13	PG7 *	I/O	GPIO_Input	VER2
G14	PG4	I/O	TIM1_BKIN2	MOT_nFAULT
G15	PG2 *	I/O	GPIO_Output	I2C3_XEN
H1	PF6 *	I/O	GPIO_Output	ETH_nSEL
H2	PF4	I/O	GPIO_EXTI4	PWR_VAUXOK
H3	PF5 *	I/O	GPIO_Output	PWR_VAUXEN
H4	PF3	I/O	GPIO_EXTI3	PWR_VCOREOK
H6	VSS	Power		
H7	VSS	Power		
H8	VSS	Power		
H9	VSS	Power		
H10	VSS	Power		
H12	VDD	Power		
H13	PG3 *	I/O	GPIO_Output	I2C4_XEN
H14	PD14	I/O	TIM4_CH3	MOT_HALL3
H15	PD13	I/O	TIM4_CH2	MOT_HALL2
J1	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	OSC_IN
J2	PF8	I/O	SPI5_MISO	ETH_MISO
J3	PF7	I/O	ADC3_INP3	PWR_aVCORE
J4	PF9	I/O	ADC3_INP2	PWR_aVAUX
J6	VSS	Power		
J7	VSS	Power		
J8	VSS	Power		
J9	VSS	Power		

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
J10	VSS	Power		
J12	PD15 *	I/O	GPIO_Analog	
J14	VSS	Power		
J15	PD12	I/O	TIM4_CH1	MOT_HALL1
K1	PH1-OSC_OUT (PH1) *	I/O	GPIO_Analog	
K2	VSS	Power		
K3	PF10 *	I/O	GPIO_Analog	
K4	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K12	VSS	Power		
K13	PD9 *	I/O	GPIO_Output	SPI2_nXEN
K14	PB15	I/O	SPI2_MOSI	SPI2_MOSI
K15	PB14	I/O	SPI2_MISO	SPI2_MISO
L1	NRST	Reset		
L2	PC0 *	I/O	GPIO_Output	TP3
L3	PC1	I/O	ETH_MDC	
L4	VREF-	Power		
L12	VDD	Power		
L13	PD10 *	I/O	GPIO_Output	SPI3_nXEN
L14	PD8 *	I/O	GPIO_Output	SPI1_nXEN
L15	PB13 *	I/O	GPIO_Output	ETH_nRST
M1	PC2	I/O	ADC1_INP12, ADC2_INP12	MOT_aVPH2
M2	PC3	I/O	ADC1_INP13, ADC2_INP13	MOT_aVPH3
M4	VDDA	Power		
M5	VDD	Power		
M6	VSS	Power		
M7	PC5	I/O	ETH_RXD1	
M8	PB1 *	I/O	GPIO_Analog	
M9	VDD	Power		
M10	VSS	Power		
M11	PH7	I/O	I2C3_SCL	I2C3_SCL
M13	PH11	I/O	TIM5_CH2	MOT_ENCB
M14	PH9 *	I/O	GPIO_Analog	
M15	PB12	I/O	ETH_TXD0	
N1	PC2_C	I/O	ADC3_INP0	PWR_aCIN

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
N2	PC3_C	I/O	ADC3_INP1	PWR_aVIN
N3	VSSA	Power		
N4	PH2 *	I/O	GPIO_Output	nLED3
N5	PA3 *	I/O	GPIO_Analog	
N6	PA7	I/O	ETH_CRS_DV	
N7	PF11	I/O	SPI5_MOSI	ETH_MOSI
N8	PE8 *	I/O	GPIO_Output	MOT_nRESET
N9	PG1 *	I/O	GPIO_Output	I2C2_XEN
N10	PF15	I/O	I2C4_SDA	I2C4_SDA
N11	PF13 *	I/O	GPIO_Output	EE_nHOLD
N13	PH8	I/O	I2C3_SDA	I2C3_SDA
N14	PH10	I/O	TIM5_CH1	MOT_ENCA
N15	PH12	I/O	TIM5_CH3	MOT_ENCZ
P2	PA1	I/O	ETH_REF_CLK	
P3	PA1_C	I/O	ADC1_INP1, ADC2_INP1	MOT_aCPH2
P4	PH4 *	I/O	GPIO_Output	nLED5
P5	PA4	I/O	SPI3_NSS	SPI3_nSEL
P6	PA5	I/O	DAC1_OUT2	TP1
P7	PB2 *	I/O	GPIO_Analog	BOOT1
P8	PG0 *	I/O	GPIO_Output	I2C1_XEN
P9	PE7 *	I/O	GPIO_Output	MOT_nSLEEP
P10	PB11	I/O	ETH_TX_EN	
P11	PF12 *	I/O	GPIO_Output	EE_nWP
P14	PE15	I/O	TIM1_BKIN	MOT_BREAK
P15	PH6	I/O	SPI5_SCK	ETH_SCLK
R1	VSS	Power		
R2	PA2	I/O	ETH_MDIO	
R3	PA0_C	I/O	ADC1_INP0, ADC2_INP0	MOT_aCPH1
R4	PH3 *	I/O	GPIO_Output	nLED4
R5	PH5 *	I/O	GPIO_Output	nLED6
R6	PC4	I/O	ETH_RXD0	
R7	PA6	I/O	ADC1_INP3, ADC2_INP3	MOT_aCPH3
R8	PB0	I/O	ADC1_INP9, ADC2_INP9	MOT_aVPH1
R10	PF14	I/O	I2C4_SCL	I2C4_SCL
R11	PE9	I/O	TIM1_CH1	MOT_PWM1
R13	VCAP	Power		
R14	VDDLDO	Power		
R15	VSS	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	AMC
Project Folder	D:\Repositories\electronics-boards\amc\sw\AMC
Toolchain / IDE	MDK-ARM V5.27
Firmware Package Name and Version	STM32Cube FW_H7 V1.9.0
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	M4-0x4000
Minimum Stack Size	M4-0x8000

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	Yes
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls ARM Cortex-M7

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_FDCAN1_Init	FDCAN1
5	MX_FDCAN2_Init	FDCAN2
6	MX_RTC_Init	RTC
7	MX_SPI5_Init	SPI5
8	MX_SPI6_Init	SPI6
9	MX_CRC_Init	CRC
10	MX_RNG_Init	RNG
11	MX_USB_DEVICE_Init	USB_DEVICE_M7

Rank	Function Name	Peripheral Instance Name
12	MX_FREERTOS_Init	FREERTOS_M7
13	MX_ETH_Init	ETH
14	MX_TIM17_Init	TIM17
15	MX_ADC3_Init	ADC3
16	MX_TIM6_Init	TIM6

5.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	MX_I2C1_Init	I2C1
4	MX_I2C2_Init	I2C2
5	MX_I2C3_Init	I2C3
6	MX_I2C4_Init	I2C4
7	MX_RTC_Init	RTC
8	MX_SPI1_Init	SPI1
9	MX_SPI2_Init	SPI2
10	MX_SPI3_Init	SPI3
11	MX_TIM4_Init	TIM4
12	MX_TIM5_Init	TIM5
13	MX_CRC_Init	CRC
14	MX_ADC1_Init	ADC1
15	MX_ADC2_Init	ADC2
16	MX_DAC1_Init	DAC1
17	MX_TIM1_Init	TIM1
18	MX_RNG_Init	RNG
19	MX_FREERTOS_Init	FREERTOS_M4
20	MX_TIM16_Init	TIM16

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H745/755
MCU	STM32H745IIKx
Datasheet	DS12923_Rev1

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(DD36000)
Capacity	36000.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	450.0 mA
Max Pulse Current	1000.0 mA
Cells in series	1
Cells in parallel	1

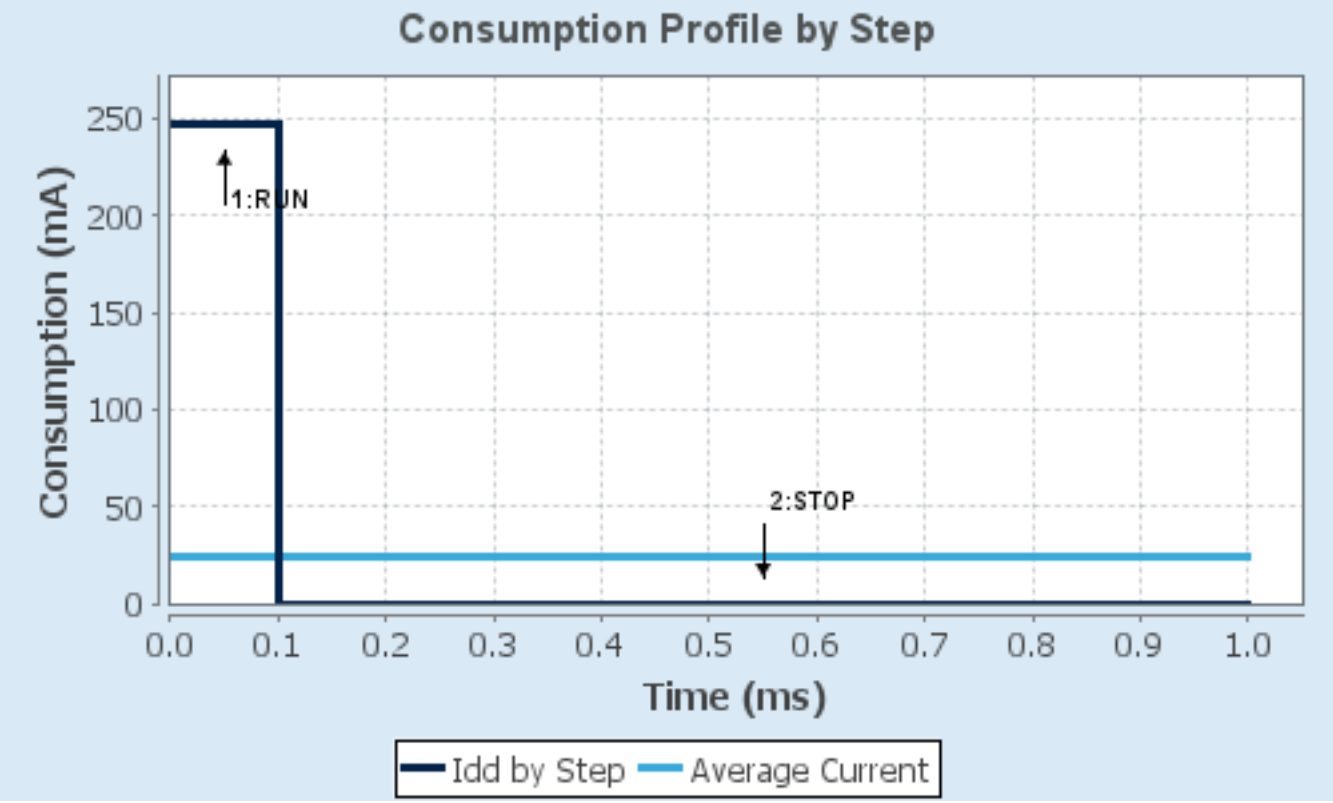
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0: Scale0	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DRUN/CRUN	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	CM7: ITCM/Cache / CM4: FLASH_B/ART	CM7: NA / CM4: NA
CM7 Frequency	480 MHz	0 Hz
Clock Configuration	HSE BYP PLL ALL_IPs_ON	LSE Flash-ON
CM4 Frequency	240 MHz	0 Hz
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	247 mA	145 µA
Duration	0.1 ms	0.9 ms
DMIPS	1027.0	0.0
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	24.83 mA
Battery Life	1 month, 29 days, 21 hours	Average DMIPS	1027.2001 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
250
200
150
100
50
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN0

IN1: IN1 Single-ended

IN3: IN3 Single-ended

mode: IN9

IN12: IN12 Single-ended

mode: IN13

7.1.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

ADCs_Common_Settings:

Mode	**Dual regular simultaneous mode only ***
DMA Access Mode	DMA access mode enabled
Delay between 2 sampling phases	**9 Cycles ***

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 2
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	**Enabled ***
Number Of Discontinuous Conversions	1
End Of Conversion Selection	End of single conversion
Overrun behaviour	**Overrun data overwritten ***
Left Bit Shift	No bit shift
Conversion Data Management Mode	**DMA Circular Mode ***
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	**3 ***
External Trigger Conversion Source	**Timer 1 Trigger Out event 2 ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1

Channel	Channel 0
Sampling Time	**8.5 Cycles ***
Offset Number	**1 offset ***
Offset	**29789 ***
Right offset shift	Disable
Offset Signed Saturation	**Enable ***
Signed saturation	**Enable ***
Rank	**2 ***
Channel	**Channel 1 ***
Sampling Time	**8.5 Cycles ***
Offset Number	**2 offsets ***
Offset	**29789 ***
Right offset shift	Disable
Offset Signed Saturation	**Enable ***
Signed saturation	**Enable ***
Rank	**3 ***
Channel	**Channel 3 ***
Sampling Time	**8.5 Cycles ***
Offset Number	**3 offsets ***
Offset	**29789 ***
Right offset shift	Disable
Offset Signed Saturation	**Enable ***
Signed saturation	**Enable ***

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC2

mode: IN0

IN1: IN1 Single-ended

IN3: IN3 Single-ended
mode: IN9
IN12: IN12 Single-ended
mode: IN13

7.2.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

ADCs_Common_Settings:

Mode	**Dual regular simultaneous mode only ***
DMA Access Mode	DMA access mode enabled
Delay between 2 sampling phases	**9 Cycles ***

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 2
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	**Enabled ***
Number Of Discontinuous Conversions	1
End Of Conversion Selection	End of single conversion
Overrun behaviour	**Overrun data overwritten ***
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	**3 ***
Rank	1
Channel	**Channel 9 ***
Sampling Time	**16.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**2 ***
Channel	**Channel 12 ***
Sampling Time	**16.5 Cycles ***

Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**3 ***
Channel	**Channel 13 ***
Sampling Time	**16.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. ADC3

mode: IN0

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

mode: Vbat Channel

mode: Temperature Sensor Channel

mode: Vrefint Channel

7.3.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D3

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 2
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	**Enabled ***

Number Of Discontinuous Conversions	1
End Of Conversion Selection	**End of sequence of conversion ***
Overrun behaviour	**Overrun data overwritten ***
Left Bit Shift	No bit shift
Conversion Data Management Mode	**DMA Circular Mode ***
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	**6 ***
External Trigger Conversion Source	**Timer 6 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 0
Sampling Time	**64.5 Cycles ***
Offset Number	**1 offset ***
Offset	**29789 ***
Right offset shift	Disable
Offset Signed Saturation	Disable
Signed saturation	Disable
Rank	**2 ***
Channel	**Channel 1 ***
Sampling Time	**64.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**3 ***
Channel	**Channel 2 ***
Sampling Time	**64.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**4 ***
Channel	**Channel 3 ***
Sampling Time	**64.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	**5 ***
Channel	**Channel Temperature Sensor ***
Sampling Time	**387.5 Cycles ***
Offset Number	No offset

Offset Signed Saturation	Disable
Rank	**6 ***
Channel	**Channel Vrefint ***
Sampling Time	**387.5 Cycles ***
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.4. CORTEX_M7

7.4.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Cortex Interface Settings:

CPU ICache	**Enabled ***
CPU DCache	**Enabled ***

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	**Background Region Privileged accesses only + MPU Enabled during hard fault, NMI and FAULTMASK handlers ***

Cortex Memory Protection Unit Region 0 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x08000000 ***
MPU Region Size	**1MB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	level 0
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	ENABLE

MPU Shareability Permission	DISABLE
MPU Cacheable Permission	**ENABLE ***
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 1 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x20000000 ***
MPU Region Size	**128KB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	**level 1 ***
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	ENABLE
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	**ENABLE ***
MPU Bufferable Permission	**ENABLE ***

Cortex Memory Protection Unit Region 2 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x2400000 ***
MPU Region Size	**512KB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	**level 1 ***
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	**ENABLE ***
MPU Bufferable Permission	**ENABLE ***

Cortex Memory Protection Unit Region 3 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x30000000 ***
MPU Region Size	**256KB ***
MPU SubRegion Disable	**0xC0 ***
MPU TEX field level	**level 1 ***
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 4 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x30040000 ***
MPU Region Size	**32KB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	**level 1 ***
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 5 Settings:

MPU Region	**Enabled ***
MPU Region Base Address	**0x38000000 ***
MPU Region Size	**64KB ***
MPU SubRegion Disable	**0x0 ***
MPU TEX field level	**level 1 ***
MPU Access Permission	**ALL ACCESS PERMITTED ***
MPU Instruction Access	**DISABLE ***
MPU Shareability Permission	DISABLE
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 6 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 7 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 8 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 9 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 10 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 11 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 12 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 13 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 14 Settings:

MPU Region	Disabled

Cortex Memory Protection Unit Region 15 Settings:

MPU Region	Disabled

7.5. CRC

mode: Activated

7.5.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D3

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

7.6. DAC1

OUT2 connected to: only external pin

7.6.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

DAC Out2 Settings:

Mode selected	Normal Mode
Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming

7.7. DEBUG

Debug: JTAG with Trace Synchro(4 bits)

7.7.1. Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	

7.8. ETH

Mode: RMII

7.8.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Ethernet MAC Address	**70:9A:0B:00:00:00 ***
Tx Descriptor Length	4
First Tx Descriptor Address	**0x30046060 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30046000 ***
Rx Buffers Address	**0x30046200 ***
Rx Buffers Length	1524

7.9. FDCAN1

mode: Activated

7.9.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Basic Parameters:

Frame Format	**FD mode with BitRate Switshing ***
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	**Enable ***
Nominal Prescaler	1
Nominal Sync Jump Width	**20 ***
Nominal Time Seg1	**79 ***
Nominal Time Seg2	**20 ***
Data Prescaler	1
Data Sync Jump Width	**8 ***
Data Time Seg1	**11 ***
Data Time Seg2	**8 ***
Message Ram Offset	0
Std Filters Nbr	0
Ext Filters Nbr	**1 ***
Rx Fifo0 Elmts Nbr	0
Rx Fifo0 Elmt Size	**64 bytes data field ***
Rx Fifo1 Elmts Nbr	0
Rx Fifo1 Elmt Size	**64 bytes data field ***
Rx Buffers Nbr	**1 ***
Rx Buffer Size	**64 bytes data field ***
Tx Events Nbr	0
Tx Buffers Nbr	**1 ***
Tx Fifo Queue Elmts Nbr	0
Tx Fifo Queue Mode	FIFO mode
Tx Elmt Size	**64 bytes data field ***

7.10. FDCAN2

mode: Activated

7.10.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Basic Parameters:

Frame Format	**FD mode with BitRate Switshing ***
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	**Enable ***
Nominal Prescaler	1
Nominal Sync Jump Width	**20 ***
Nominal Time Seg1	**79 ***
Nominal Time Seg2	**20 ***
Data Prescaler	1
Data Sync Jump Width	**8 ***
Data Time Seg1	**11 ***
Data Time Seg2	**8 ***
Message Ram Offset	**1280 ***
Std Filters Nbr	0
Ext Filters Nbr	**1 ***
Rx Fifo0 Elmts Nbr	0
Rx Fifo0 Elmt Size	**64 bytes data field ***
Rx Fifo1 Elmts Nbr	0
Rx Fifo1 Elmt Size	**64 bytes data field ***
Rx Buffers Nbr	**1 ***
Rx Buffer Size	**64 bytes data field ***
Tx Events Nbr	0
Tx Buffers Nbr	**1 ***
Tx Fifo Queue Elmts Nbr	0
Tx Fifo Queue Mode	FIFO mode
Tx Elmt Size	**64 bytes data field ***

7.11. I2C1

I2C: I2C

7.11.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10C0ECFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.12. I2C2

I2C: I2C

7.12.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0

Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10C0ECFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.13. I2C3

I2C: I2C

7.13.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10C0ECFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.14. I2C4

I2C: I2C

7.14.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D3

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10C0ECFF ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.15. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

mode: Master Clock Output 1

7.15.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	D3

Power Parameters:

SupplySource	**PWR_EXTERNAL_SOURCE_SUPPLY ***

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	2 WS (3 CPU cycle)
Product revision	rev.Y

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL2 input frequency range	Between 4 and 8 MHz
PLL3 input frequency range	Between 1 and 2 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range
PLL3 clock Output range	Wide VCO range

7.16. RESMGR_UTILITY

mode: Resource assignment request

7.16.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	RESMGR_UTILITY version

h7/v1.4.0

7.16.2. Resources assignment:

Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M7

Power Domain:	request resource assignment for BDMA_Channel0 in resource table
no	request resource assignment for BDMA_Channel1 in resource table
no	request resource assignment for BDMA_Channel2 in resource table
no	request resource assignment for BDMA_Channel3 in resource table
no	request resource assignment for BDMA_Channel4 in resource table
no	request resource assignment for BDMA_Channel5 in resource table
no	request resource assignment for BDMA_Channel6 in resource table
no	request resource assignment for BDMA_Channel7 in resource table
no	request resource assignment for DFSDM1_Channel0 in resource table
no	request resource assignment for DFSDM1_Channel1 in resource table
no	request resource assignment for DFSDM1_Channel2 in resource table
no	request resource assignment for DFSDM1_Channel3 in resource table
no	request resource assignment for DFSDM1_Channel4 in resource table
no	request resource assignment for DFSDM1_Channel5 in resource table
no	request resource assignment for DFSDM1_Channel6 in resource table
no	request resource assignment for DFSDM1_Channel7 in resource table
no	request resource assignment for DFSDM1_Filter0 in resource table
no	request resource assignment for DFSDM1_Filter1 in resource table
no	request resource assignment for DFSDM1_Filter2 in resource table
no	request resource assignment for DFSDM1_Filter3 in resource table
no	request resource assignment for DMA1_Stream0 in resource table
no	request resource assignment for DMA1_Stream1 in resource table
no	request resource assignment for DMA1_Stream2 in resource table
is assigned to Cortex-M7 *	request resource assignment for DMA1_Stream3 in resource table
is assigned to Cortex-M7 *	request resource assignment for DMA1_Stream4 in resource table
no	request resource assignment for DMA1_Stream5 in resource table
no	request resource assignment for DMA1_Stream6 in resource table
no	request resource assignment for DMA1_Stream7 in resource table
no	request resource assignment for DMA2_Stream0 in resource table
no	request resource assignment for DMA2_Stream1 in resource table
no	request resource assignment for DMA2_Stream2 in resource table
no	request resource assignment for DMA2_Stream3 in resource table
no	request resource assignment for DMA2_Stream4 in resource table
no	request resource assignment for DMA2_Stream5 in resource table
no	request resource assignment for DMA2_Stream6 in resource table
no	request resource assignment for DMA2_Stream7 in resource table
no	request resource assignment for DMAMUX1_RequestGenerator0 in resource table
no	request resource assignment for DMAMUX1_RequestGenerator1 in resource table
no	request resource assignment for DMAMUX1_RequestGenerator2 in resource table
no	request resource assignment for DMAMUX1_RequestGenerator3 in resource table
no	request resource assignment for DMAMUX1_RequestGenerator4 in resource table
no	request resource assignment for DMAMUX1_RequestGenerator5 in resource table
no	request resource assignment for DMAMUX1_RequestGenerator6 in resource table

no	request resource assignment for DMAMUX1_RequestGenerator7 in resource table
no	request resource assignment for DMAMUX2_RequestGenerator0 in resource table
no	request resource assignment for DMAMUX2_RequestGenerator1 in resource table
no	request resource assignment for DMAMUX2_RequestGenerator2 in resource table
no	request resource assignment for DMAMUX2_RequestGenerator3 in resource table
no	request resource assignment for DMAMUX2_RequestGenerator4 in resource table
no	request resource assignment for DMAMUX2_RequestGenerator5 in resource table
no	request resource assignment for DMAMUX2_RequestGenerator6 in resource table
no	request resource assignment for DMAMUX2_RequestGenerator7 in resource table
no	request resource assignment for FDCAN_CCU in resource table
is assigned to Cortex-M7	request resource assignment for GPIOA in resource table
no	request resource assignment for GPIOB in resource table
no	request resource assignment for GPIOC in resource table
no	request resource assignment for GPIOD in resource table
no	request resource assignment for GPIOE in resource table
no	request resource assignment for GPIOF in resource table
no	request resource assignment for GPIOG in resource table
no	request resource assignment for GPIOH in resource table
no	request resource assignment for GPIOI in resource table
no	request resource assignment for GPIOJ in resource table
no	request resource assignment for GPIOK in resource table
no	request resource assignment for HSEM in resource table
is assigned to Cortex-M7 *	request resource assignment for MDMA_Channel0 in resource table
no	request resource assignment for MDMA_Channel1 in resource table
no	request resource assignment for MDMA_Channel2 in resource table
no	request resource assignment for MDMA_Channel3 in resource table
no	request resource assignment for MDMA_Channel4 in resource table
no	request resource assignment for MDMA_Channel5 in resource table
no	request resource assignment for MDMA_Channel6 in resource table
no	request resource assignment for MDMA_Channel7 in resource table
no	request resource assignment for MDMA_Channel8 in resource table
no	request resource assignment for MDMA_Channel9 in resource table
no	request resource assignment for MDMA_Channel10 in resource table
no	request resource assignment for MDMA_Channel11 in resource table
no	request resource assignment for MDMA_Channel12 in resource table
no	request resource assignment for MDMA_Channel13 in resource table
no	request resource assignment for MDMA_Channel14 in resource table
no	request resource assignment for MDMA_Channel15 in resource table
no	request resource assignment for PWR in resource table
is assigned to Cortex-M7	request resource assignment for VREFBUF in resource table
is assigned to Cortex-M7	request resource assignment for ADC1 in resource table
is assigned to Cortex-M4	request resource assignment for ADC12_COMMON in resource table
is assigned to Cortex-M4 (by ADC1 assignment)	request resource assignment for ADC2 in resource table

is assigned to Cortex-M4	request resource assignment for ADC3 in resource table
is assigned to Cortex-M7	request resource assignment for BDMA in resource table
is assigned to Cortex-M7	request resource assignment for HDMI_CEC in resource table
no	request resource assignment for COMP1 in resource table
no	request resource assignment for COMP2 in resource table
no	request resource assignment for CRC in resource table
is assigned to Cortex-M4	request resource assignment for CRS in resource table
is assigned to Cortex-M7	request resource assignment for DAC1 in resource table
is assigned to Cortex-M4	request resource assignment for DBGMCU in resource table
is assigned to Cortex-M7	request resource assignment for DCMI in resource table
no	request resource assignment for DFSDM1 in resource table
no	request resource assignment for DLYB_QUADSPI in resource table
no	request resource assignment for DLYB_SDMMC1 in resource table
no	request resource assignment for DLYB_SDMMC2 in resource table
no	request resource assignment for DMA1 in resource table
is assigned to Cortex-M7	request resource assignment for DMA2 in resource table
is assigned to Cortex-M7	request resource assignment for DMA2D in resource table
no	request resource assignment for DMAMUX1 in resource table
is assigned to Cortex-M7	request resource assignment for DMAMUX1_Channel0 in resource table
no	request resource assignment for DMAMUX1_Channel1 in resource table
no	request resource assignment for DMAMUX1_Channel2 in resource table
is assigned to Cortex-M7	request resource assignment for DMAMUX1_Channel3 in resource table
is assigned to Cortex-M7	request resource assignment for DMAMUX1_Channel4 in resource table
no	request resource assignment for DMAMUX1_Channel5 in resource table
no	request resource assignment for DMAMUX1_Channel6 in resource table
no	request resource assignment for DMAMUX1_Channel7 in resource table
no	request resource assignment for DMAMUX1_Channel8 in resource table
no	request resource assignment for DMAMUX1_Channel9 in resource table
no	request resource assignment for DMAMUX1_Channel10 in resource table
no	request resource assignment for DMAMUX1_Channel11 in resource table
no	request resource assignment for DMAMUX1_Channel12 in resource table
no	request resource assignment for DMAMUX1_Channel13 in resource table
no	request resource assignment for DMAMUX1_Channel14 in resource table
no	request resource assignment for DMAMUX1_Channel15 in resource table
no	request resource assignment for DMAMUX2 in resource table
is assigned to Cortex-M7	request resource assignment for DMAMUX2_Channel0 in resource table
no	request resource assignment for DMAMUX2_Channel1 in resource table
no	request resource assignment for DMAMUX2_Channel2 in resource table
no	request resource assignment for DMAMUX2_Channel3 in resource table
no	request resource assignment for DMAMUX2_Channel4 in resource table
no	request resource assignment for DMAMUX2_Channel5 in resource table
no	request resource assignment for DMAMUX2_Channel6 in resource table
no	request resource assignment for DMAMUX2_Channel7 in resource table

no	request resource assignment for DSIHOST in resource table
no	request resource assignment for ETH in resource table
is assigned to Cortex-M7	request resource assignment for EXTI in resource table
no	request resource assignment for EXTI_D1 in resource table
no	request resource assignment for EXTI_D2 in resource table
no	request resource assignment for FDCAN1 in resource table
is assigned to Cortex-M7	request resource assignment for FDCAN2 in resource table
is assigned to Cortex-M7	request resource assignment for FLASH in resource table
no	request resource assignment for FMC in resource table
no	request resource assignment for HRTIM in resource table
is assigned to Cortex-M4	request resource assignment for I2C1 in resource table
is assigned to Cortex-M4	request resource assignment for I2C2 in resource table
is assigned to Cortex-M4	request resource assignment for I2C3 in resource table
is assigned to Cortex-M4	request resource assignment for I2C4 in resource table
is assigned to Cortex-M4	request resource assignment for IWDG1 in resource table
is assigned to Cortex-M7	request resource assignment for IWDG2 in resource table
is assigned to Cortex-M4	request resource assignment for JPEG in resource table
no	request resource assignment for LPTIM1 in resource table
is assigned to Cortex-M4	request resource assignment for LPTIM2 in resource table
no	request resource assignment for LPTIM3 in resource table
no	request resource assignment for LPTIM4 in resource table
no	request resource assignment for LPTIM5 in resource table
no	request resource assignment for LPUART1 in resource table
no	request resource assignment for LTDC in resource table
no	request resource assignment for MDIOS in resource table
no	request resource assignment for MDMA in resource table
is assigned to Cortex-M7	request resource assignment for OPAMP1 in resource table
no	request resource assignment for OPAMP2 in resource table
no	request resource assignment for QUADSPI in resource table
no	request resource assignment for RCC in resource table
no	request resource assignment for RCC_C1 in resource table
no	request resource assignment for RCC_C2 in resource table
no	request resource assignment for RNG in resource table
is assigned to Cortex-M7	request resource assignment for RTC in resource table
is assigned to Cortex-M7	request resource assignment for SAI1 in resource table
no	request resource assignment for SAI2 in resource table
no	request resource assignment for SAI3 in resource table
no	request resource assignment for SAI4 in resource table
no	request resource assignment for SDMMC1 in resource table
no	request resource assignment for SDMMC2 in resource table
no	request resource assignment for SPDIFRX1 in resource table
no	request resource assignment for SPI1 in resource table
is assigned to Cortex-M4	request resource assignment for SPI2 in resource table

is assigned to Cortex-M4	request resource assignment for SPI3 in resource table
is assigned to Cortex-M4	request resource assignment for SPI4 in resource table
no	request resource assignment for SPI5 in resource table
is assigned to Cortex-M7	request resource assignment for SPI6 in resource table
is assigned to Cortex-M7	request resource assignment for SWPMI1 in resource table
no	request resource assignment for SYS in resource table
is assigned to Cortex-M7	request resource assignment for TIM1 in resource table
is assigned to Cortex-M4	request resource assignment for TIM12 in resource table
no	request resource assignment for TIM13 in resource table
no	request resource assignment for TIM14 in resource table
no	request resource assignment for TIM15 in resource table
no	request resource assignment for TIM16 in resource table
is assigned to Cortex-M4	request resource assignment for TIM17 in resource table
is assigned to Cortex-M7	request resource assignment for TIM2 in resource table
no	request resource assignment for TIM3 in resource table
no	request resource assignment for TIM4 in resource table
is assigned to Cortex-M4	request resource assignment for TIM5 in resource table
is assigned to Cortex-M4	request resource assignment for TIM6 in resource table
is assigned to Cortex-M7	request resource assignment for TIM7 in resource table
no	request resource assignment for TIM8 in resource table
no	request resource assignment for UART4 in resource table
no	request resource assignment for UART5 in resource table
no	request resource assignment for UART7 in resource table
no	request resource assignment for UART8 in resource table
no	request resource assignment for USART1 in resource table
no	request resource assignment for USART2 in resource table
no	request resource assignment for USART3 in resource table
no	request resource assignment for USART6 in resource table
no	request resource assignment for USB_OTG_HS in resource table
no	request resource assignment for USB_OTG_FS in resource table
is assigned to Cortex-M7	request resource assignment for WWDG1 in resource table
is assigned to Cortex-M7	request resource assignment for WWDG2 in resource table
is assigned to Cortex-M4	

7.17. RNG

mode: Activated

7.17.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7

	Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	D2
Clock Error Detection	Enable

7.18. RTC

mode: Activate Clock Source

mode: Activate Calendar

7.18.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
	Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	D3

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

7.19. SPI1

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.19.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**25.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.20. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.20.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4

Initialized Context:	Cortex-M4
Power Domain:	D2

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**25.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.21. SPI3

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.21.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits

First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**25.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.22. SPI5

Mode: Full-Duplex Master

7.22.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**50.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	**Disabled ***
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	**01 Cycle ***
Master Receiver Auto Susp	**Enable ***
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.23. SPI6

Mode: Full-Duplex Master

7.23.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D3

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**12.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low

Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.24. SYS

Timebase Source: SysTick

7.24.1. Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	

7.25. SYS_M4

Timebase Source: SysTick

7.25.1. Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	

7.26. TIM1

Clock Source : Internal Clock
Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel6: PWM Generation No Output
Activate-Break-Input: Activate Break Input
Activate-Break-Input-2: Activate Break Input 2

7.26.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	**Center Aligned mode1 ***
Counter Period (AutoReload Register - 16 bits value)	**1024 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***
Trigger Event Selection TRGO2	**Output Compare (OC6REF) ***

Break And Dead Time management - BRK Configuration:

BRK State	Enable
BRK Polarity	High
BRK Filter (4 bits value)	**15 ***
BRK Sources Configuration	
- Digital Input	Enable
Digital Input Polarity	**Polarity Low ***
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Enable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Enable
Digital Input Polarity	**Polarity Low ***
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Enable
Off State Selection for Idle Mode (OSSI)	Enable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 6:

Mode	**PWM mode 2 ***
Pulse (16 bits value)	**752 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.27. TIM4

Clock Source : Internal Clock

Combined Channels: XOR ON / Hall Sensor Mode

7.27.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	

	Cortex-M4
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**200 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection TRGO	Output Compare (OC2REF)

Hall Sensor:

Prescaler Division Ratio	No division
Polarity	Rising Edge
Input Filter	**4 ***
Commutation Delay	0

7.28. TIM5

Channel3: Input Capture direct mode

Channel4: Input Capture indirect mode

Combined Channels: Encoder Mode

7.28.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	4294967295
Internal Clock Division (CKD)	**Division by 4 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	**8 ***

Input Capture Channel 4:

Polarity Selection	**Falling Edge ***
IC Selection	Indirect
Prescaler Division Ratio	No division

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**8 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**15 ***

7.29. TIM6

mode: Activated

7.29.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**200 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000 ***
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

7.30. TIM16

mode: Activated

7.30.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**199 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	**Enable ***

7.31. TIM17

mode: Activated

7.31.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2

Counter Settings:

Prescaler (PSC - 16 bits value)	**199 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	**Enable ***

7.32. USB_OTG_FS

Mode: Device_Only

7.32.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D2
Speed	Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Low power	Disabled
Battery charging	Disabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

7.33. VREFBUF

VREFBUF Mode: External voltage reference

7.33.1. Core(s) Settings:

Context(s):	Cortex-M7 Cortex-M4
Initialized Context:	Cortex-M7
Power Domain:	

7.34. FREERTOS_M4

Interface: CMSIS_V1

7.34.1. Config parameters:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4

Power Domain:	D2
API:	
FreeRTOS API	CMSIS v1
Versions:	
FreeRTOS version	10.3.1
CMSIS-RTOS version	1.02
MPU/FPU:	
ENABLE_MPU	Disabled
ENABLE_FPU	Disabled
Kernel settings:	
USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemD2Clock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	**Enabled ***
USE_COUNTING_SEMAPHORES	**Enabled ***
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled
Memory management settings:	
Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	**16384 ***
Memory Management scheme	heap_4
Hook function related definitions:	
USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled
Run time and task stats gathering related definitions:	
GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled

USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

7.34.2. Include parameters:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	**Enabled ***
xSemaphoreGetMutexHolder	**Enabled ***
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	**Enabled ***
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	**Enabled ***

uxTaskGetStackHighWaterMark2	Disabled

7.34.3. Advanced settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	D2

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

7.35. FREERTOS_M7

Interface: CMSIS_V1

7.35.1. Config parameters:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.3.1
CMSIS-RTOS version	1.02

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16

USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	**Enabled ***
USE_COUNTING_SEMAPHORES	**Enabled ***
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled
Memory management settings:	
Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	**65536 ***
Memory Management scheme	heap_4
Hook function related definitions:	
USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled
Run time and task stats gathering related definitions:	
GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled
Co-routine related definitions:	
USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2
Software timer definitions:	
USE_TIMERS	Disabled
Interrupt nesting behaviour configuration:	
LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5
Added with 10.2.1 support:	
MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

7.35.2. Include parameters:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	**Enabled ***
xSemaphoreGetMutexHolder	**Enabled ***
pcTaskGetTaskName	**Enabled ***
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	**Enabled ***
eTaskGetState	**Enabled ***
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	**Enabled ***
uxTaskGetStackHighWaterMark2	Disabled

7.35.3. Advanced settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

7.36. USB_DEVICE_M7

Class For FS IP: Communication Device Class (Virtual Port Com)

7.36.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message

Class Parameters:

USB CDC Rx Buffer Size	2048
USB CDC Tx Buffer Size	2048

7.36.2. Device Descriptor:

Core(s) Settings:

Context(s):	Cortex-M7
Initialized Context:	Cortex-M7
Power Domain:	D1

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
ADC1	PC2	ADC1_INP12	Analog mode	No pull-up and no pull-down	n/a	MOT_aVPH2	Cortex-M4	D2
	PC3	ADC1_INP13	Analog mode	No pull-up and no pull-down	n/a	MOT_aVPH3	Cortex-M4	D2
	PA1_C	ADC1_INP1	Analog mode	No pull-up and no pull-down	n/a	MOT_aCPH2	Cortex-M4	D2
	PA0_C	ADC1_INP0	Analog mode	No pull-up and no pull-down	n/a	MOT_aCPH1	Cortex-M4	D2
	PA6	ADC1_INP3	Analog mode	No pull-up and no pull-down	n/a	MOT_aCPH3	Cortex-M4	D2
	PB0	ADC1_INP9	Analog mode	No pull-up and no pull-down	n/a	MOT_aVPH1	Cortex-M4	D2
ADC2	PC2	ADC2_INP12	Analog mode	No pull-up and no pull-down	n/a	MOT_aVPH2	Cortex-M4	D2
	PC3	ADC2_INP13	Analog mode	No pull-up and no pull-down	n/a	MOT_aVPH3	Cortex-M4	D2
	PA1_C	ADC2_INP1	Analog mode	No pull-up and no pull-down	n/a	MOT_aCPH2	Cortex-M4	D2
	PA0_C	ADC2_INP0	Analog mode	No pull-up and no pull-down	n/a	MOT_aCPH1	Cortex-M4	D2
	PA6	ADC2_INP3	Analog mode	No pull-up and no pull-down	n/a	MOT_aCPH3	Cortex-M4	D2
	PB0	ADC2_INP9	Analog mode	No pull-up and no pull-down	n/a	MOT_aVPH1	Cortex-M4	D2
ADC3	PF7	ADC3_INP3	Analog mode	No pull-up and no pull-down	n/a	PWR_aVCORE	Cortex-M7	D3
	PF9	ADC3_INP2	Analog mode	No pull-up and no pull-down	n/a	PWR_aVAUX	Cortex-M7	D3
	PC2_C	ADC3_INP0	Analog mode	No pull-up and no pull-down	n/a	PWR_aCIN	Cortex-M7	D3
	PC3_C	ADC3_INP1	Analog mode	No pull-up and no pull-down	n/a	PWR_aVIN	Cortex-M7	D3
DAC1	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	TP1	Cortex-M4	D2
DEBUG	PB3 (JTDO/TRACESWO	DEBUG_JTDO-SWO	n/a	n/a	n/a	JTDO_SWO	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PA15 (JTDI)	DEBUG_JTDI	n/a	n/a	n/a	JTDI	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PA14	DEBUG_JTC	n/a	n/a	n/a	JTCK_SWCK	Cortex-M7*	Cortex-M7*

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	(JTCK/SWCLK)	K-SWCLK					Cortex-M4	Cortex-M4
	PE4	DEBUG_TRACED1	n/a	n/a	n/a	TRACED1	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PE3	DEBUG_TRACED0	n/a	n/a	n/a	TRACED0	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PD2	DEBUG_TRACED2	n/a	n/a	n/a	TRACED2	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PC12	DEBUG_TRACED3	n/a	n/a	n/a	TRACED3	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	JTMS_SWDIO	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
	PE2	DEBUG_TRACECLK	n/a	n/a	n/a	TRACECLK	Cortex-M7* Cortex-M4	Cortex-M7* Cortex-M4
ETH	PG12	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***		Cortex-M7	D2
FDCAN1	PD1	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	CAN1_TXD	Cortex-M7	D2
	PH14	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	CAN1_RXD	Cortex-M7	D2
FDCAN2	PB6	FDCAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	CAN2_TXD	Cortex-M7	D2
	PB5	FDCAN2_RX	Alternate Function	No pull-up and no pull-		CAN2_RXD	Cortex-M7	D2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
			Push Pull	down	**Very High ***			
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	**Pull-up ***	**Very High ***	I2C1_SCL	Cortex-M4	D2
	PB7	I2C1_SDA	Alternate Function Open Drain	**Pull-up ***	**Very High ***	I2C1_SDA	Cortex-M4	D2
I2C2	PF1	I2C2_SCL	Alternate Function Open Drain	**Pull-up ***	**Very High ***	I2C2_SCL	Cortex-M4	D2
	PF0	I2C2_SDA	Alternate Function Open Drain	**Pull-up ***	**Very High ***	I2C2_SDA	Cortex-M4	D2
I2C3	PH7	I2C3_SCL	Alternate Function Open Drain	**Pull-up ***	**Very High ***	I2C3_SCL	Cortex-M4	D2
	PH8	I2C3_SDA	Alternate Function Open Drain	**Pull-up ***	**Very High ***	I2C3_SDA	Cortex-M4	D2
I2C4	PF15	I2C4_SDA	Alternate Function Open Drain	**Pull-up ***	**Very High ***	I2C4_SDA	Cortex-M4	D3
	PF14	I2C4_SCL	Alternate Function Open Drain	**Pull-up ***	**Very High ***	I2C4_SCL	Cortex-M4	D3
RCC	PA8	RCC_MCO_1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	TP2	Cortex-M7* Cortex-M4	D3
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	**n/a**	OSS32_OUT	Cortex-M7* Cortex-M4	D3
	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	**n/a**	OS32_IN	Cortex-M7* Cortex-M4	D3
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	**n/a**	OSC_IN	Cortex-M7* Cortex-M4	D3
SPI1	PG11	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI1_SCLK	Cortex-M4	D2
	PG9	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI1_MISO	Cortex-M4	D2
	PD7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI1_MOSI	Cortex-M4	D2
	PG10	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI1_nSEL	Cortex-M4	D2
SPI2	PD3	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI2_SCLK	Cortex-M4	D2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PB9	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI2_nSEL	Cortex-M4	D2
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI2_MOSI	Cortex-M4	D2
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI2_MISO	Cortex-M4	D2
SPI3	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI3_MISO	Cortex-M4	D2
	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI3_SCLK	Cortex-M4	D2
	PD6	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI3_MOSI	Cortex-M4	D2
	PA4	SPI3_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SPI3_nSEL	Cortex-M4	D2
SPI5	PF8	SPI5_MISO	Alternate Function Push Pull	**Pull-down ***	**Very High ***	ETH_MISO	Cortex-M7	D2
	PF11	SPI5_MOSI	Alternate Function Push Pull	**Pull-up ***	**Very High ***	ETH_MOSI	Cortex-M7	D2
	PH6	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	ETH_SCLK	Cortex-M7	D2
SPI6	PB4 (NJTRST)	SPI6_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	EE_MISO	Cortex-M7	D3
	PG13	SPI6_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	EE_SCLK	Cortex-M7	D3
	PG14	SPI6_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	EE_MOSI	Cortex-M7	D3
TIM1	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MOT_PWM3	Cortex-M4	D2
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MOT_PWM2	Cortex-M4	D2
	PG4	TIM1_BKIN2	Alternate Function Open Drain	**Pull-up ***	Low	MOT_nFAULT	Cortex-M4	D2
	PE15	TIM1_BKIN	Alternate Function Open Drain	**Pull-down ***	Low	MOT_BREAK	Cortex-M4	D2
	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MOT_PWM1	Cortex-M4	D2
TIM4	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	**Very**	MOT_HALL3	Cortex-M4	D2

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
					High *			
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MOT_HALL2	Cortex-M4	D2
	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MOT_HALL1	Cortex-M4	D2
TIM5	PH11	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MOT_ENCB	Cortex-M4	D2
	PH10	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MOT_ENCA	Cortex-M4	D2
	PH12	TIM5_CH3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MOT_ENCZ	Cortex-M4	D2
USB_OTG_FS	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DP	Cortex-M7	D2
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USB_DM	Cortex-M7	D2
GPIO	PE0	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	**Pull-up ***	n/a	ETH_nPME	Cortex-M7	Cortex-M7
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	CAN2_STBY	Cortex-M7	Cortex-M7
	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TP4	Cortex-M4	Cortex-M4
	PE1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	**Pull-up ***	n/a	ETH_nIRQ	Cortex-M7	Cortex-M7
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	CAN1_STBY	Cortex-M7	Cortex-M7
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	CAN_SHDN	Cortex-M7	Cortex-M7
	PH13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	nLED1	Cortex-M4	Cortex-M4
	PG15	GPIO_Analog	Analog mode	No pull-up and no pull-down	**n/a**			
	PH15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	nLED2	Cortex-M4	Cortex-M4
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	MOT_EN3	Cortex-M4	Cortex-M4
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	MOT_EN2	Cortex-M4	Cortex-M4

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	MOT_EN4	Cortex-M4	Cortex-M4
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	MOT_EN1	Cortex-M4	Cortex-M4
	PG6	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	VER1	Cortex-M4	Cortex-M4
	PG5	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	VER0	Cortex-M4	Cortex-M4
	PF2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	**Pull-up ***	**n/a**	PWR_VCCOK	Cortex-M4	Cortex-M4
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	EE_nSEL	Cortex-M7	Cortex-M7
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	VER2	Cortex-M4	Cortex-M4
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	I2C3_XEN	Cortex-M4	Cortex-M4
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	ETH_nSEL	Cortex-M7	Cortex-M7
	PF4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	**Pull-up ***	**n/a**	PWR_VAUXOK	Cortex-M4	Cortex-M4
	PF5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PWR_VAUXEN	Cortex-M4	Cortex-M4
	PF3	GPIO_EXTI3	External Interrupt Mode with Rising edge trigger detection	**Pull-up ***	n/a	PWR_VCOREOK	Cortex-M4	Cortex-M4
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	I2C4_XEN	Cortex-M4	Cortex-M4
	PD15	GPIO_Analog	Analog mode	No pull-up and no pull-down	**n/a**			
	PH1-OSC_OUT (PH1)	GPIO_Analog	Analog mode	No pull-up and no pull-down	**n/a**			
	PF10	GPIO_Analog	Analog mode	No pull-up and no pull-down	**n/a**			
	PD9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI2_nXEN	Cortex-M4	Cortex-M4
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TP3	Cortex-M4	Cortex-M4
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI3_nXEN	Cortex-M4	Cortex-M4
	PD8	GPIO_Output	Output Push Pull	No pull-up and no pull-	Low	SPI1_nXEN	Cortex-M4	Cortex-M4

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
				down				
	PB13	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	**Medium ***	ETH_nRST	Cortex-M7	Cortex-M7
	PB1	GPIO_Analog	Analog mode	No pull-up and no pull-down	**n/a**			
	PH9	GPIO_Analog	Analog mode	No pull-up and no pull-down	**n/a**			
	PH2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	nLED3	Cortex-M4	Cortex-M4
	PA3	GPIO_Analog	Analog mode	No pull-up and no pull-down	**n/a**			
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	MOT_nRESET	Cortex-M4	Cortex-M4
	PG1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	I2C2_XEN	Cortex-M4	Cortex-M4
	PF13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	EE_nHOLD	Cortex-M7	Cortex-M7
	PH4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	nLED5	Cortex-M4	Cortex-M4
	PB2	GPIO_Analog	Analog mode	No pull-up and no pull-down	**n/a**	BOOT1	Cortex-M4	Cortex-M4
	PG0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	I2C1_XEN	Cortex-M4	Cortex-M4
	PE7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	MOT_nSLEEP	Cortex-M4	Cortex-M4
	PF12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	EE_nWP	Cortex-M7	Cortex-M7
	PH3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	nLED4	Cortex-M4	Cortex-M4
	PH5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	nLED6	Cortex-M4	Cortex-M4

* Initialized context

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	**High ***
ADC3	DMA1_Stream4	Peripheral To Memory	**Medium ***

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

ADC3: DMA1_Stream4 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

8.5.1. NVIC1

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream4 global interrupt	true	5	0
FDCAN1 interrupt 0	true	5	0
FDCAN2 interrupt 0	true	5	0
FDCAN1 interrupt 1	true	5	0
FDCAN2 interrupt 1	true	5	0
Ethernet global interrupt	true	5	0
Ethernet wake-up interrupt through EXTI line 86	true	5	0
SPI5 global interrupt	true	5	0
SPI6 global interrupt	true	5	0
USB On The Go FS End Point 1 Out global interrupt	true	5	0
USB On The Go FS End Point 1 In global interrupt	true	5	0
USB On The Go FS global interrupt	true	5	0
TIM17 global interrupt	true	15	0
HSEM1 global interrupt	true	5	0
ADC3 global interrupt	true	5	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line0 interrupt	unused		
EXTI line1 interrupt	unused		
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	unused		
FDCAN calibration unit interrupt	unused		
CM4 send event interrupt for CM7	unused		
HASH and RNG global interrupts	unused		
FPU global interrupt	unused		
RAM ECC diagnostic global interrupt	unused		
Hold core interrupt	unused		

8.5.2. NVIC1 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	true	false
DMA1 stream4 global interrupt	false	true	true
FDCAN1 interrupt 0	false	true	true
FDCAN2 interrupt 0	false	true	true
FDCAN1 interrupt 1	false	true	true
FDCAN2 interrupt 1	false	true	true
Ethernet global interrupt	false	true	true
Ethernet wake-up interrupt through EXTI line 86	false	true	true
SPI5 global interrupt	false	true	true
SPI6 global interrupt	false	true	true
USB On The Go FS End Point 1 Out global interrupt	false	true	true
USB On The Go FS End Point 1 In global interrupt	false	true	true
USB On The Go FS global interrupt	false	true	true
TIM17 global interrupt	false	true	true
HSEM1 global interrupt	false	true	true
ADC3 global interrupt	false	true	true

8.5.3. NVIC2

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0

Interrupt Table	Enable	Preenmption Priority	SubPriority
System tick timer	true	15	0
ADC1 and ADC2 global interrupts	true	5	0
TIM1 break interrupt	true	5	0
TIM1 update interrupt	true	5	0
TIM1 trigger and commutation interrupts	true	5	0
TIM1 capture compare interrupt	true	5	0
TIM4 global interrupt	true	5	0
I2C1 event interrupt	true	5	0
I2C1 error interrupt	true	5	0
I2C2 event interrupt	true	5	0
I2C2 error interrupt	true	5	0
SPI1 global interrupt	true	5	0
SPI2 global interrupt	true	5	0
TIM5 global interrupt	true	5	0
SPI3 global interrupt	true	5	0
DMA2 stream0 global interrupt	true	5	0
I2C3 event interrupt	true	5	0
I2C3 error interrupt	true	5	0
I2C4 event interrupt	true	5	0
I2C4 error interrupt	true	5	0
TIM16 global interrupt	true	15	0
HSEM2 global interrupt	true	5	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
EXTI line2 interrupt	unused		
EXTI line3 interrupt	unused		
EXTI line4 interrupt	unused		
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	unused		
CM7 send event interrupt for CM4	unused		
HASH and RNG global interrupts	unused		
FPU global interrupt	unused		
RAM ECC diagnostic global interrupt	unused		
Hold core interrupt	unused		

8.5.4. NVIC2 Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false

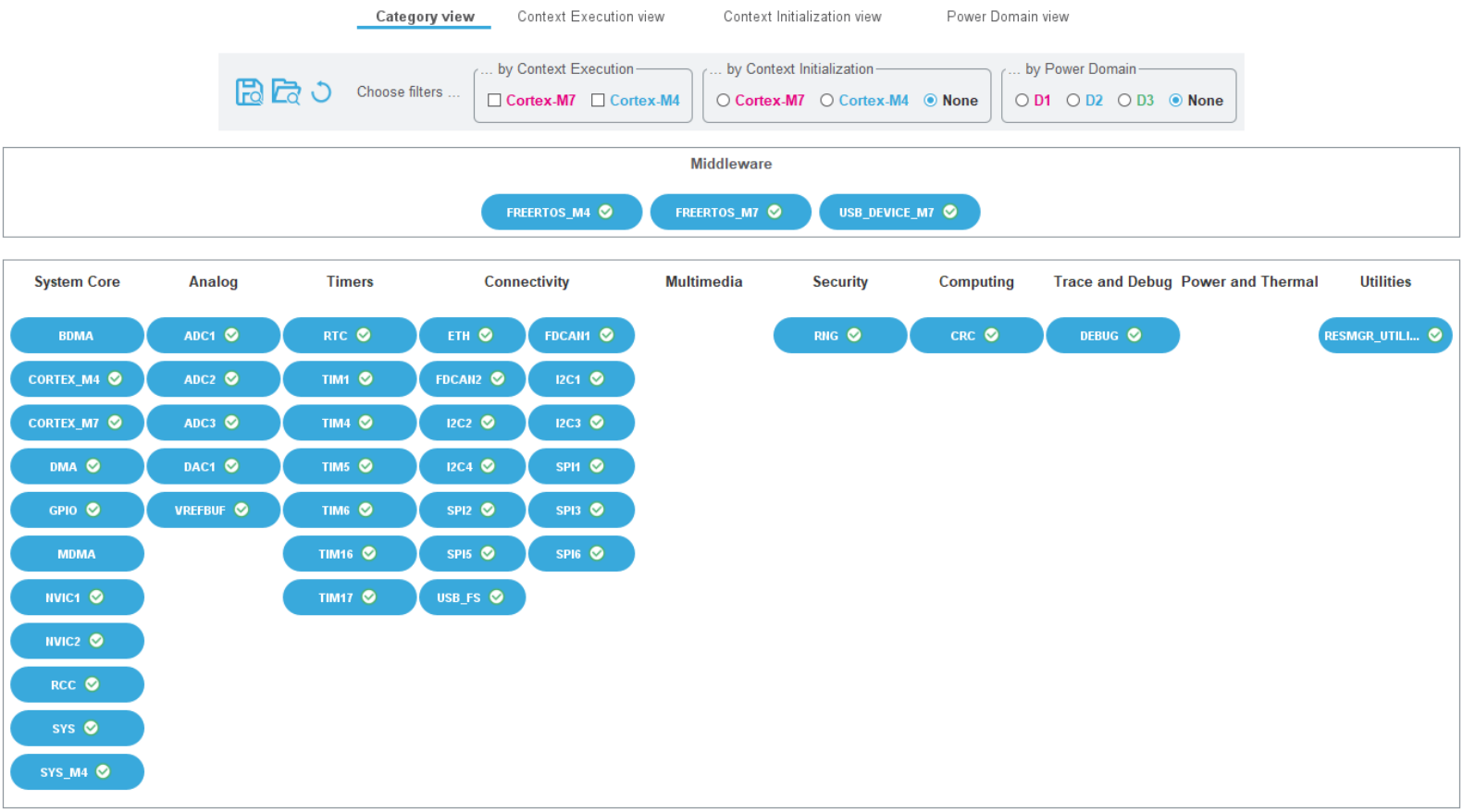
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	true	false
ADC1 and ADC2 global interrupts	false	true	true
TIM1 break interrupt	false	true	true
TIM1 update interrupt	false	true	true
TIM1 trigger and commutation interrupts	false	true	true
TIM1 capture compare interrupt	false	true	true
TIM4 global interrupt	false	true	true
I2C1 event interrupt	false	true	true
I2C1 error interrupt	false	true	true
I2C2 event interrupt	false	true	true
I2C2 error interrupt	false	true	true
SPI1 global interrupt	false	true	true
SPI2 global interrupt	false	true	true
TIM5 global interrupt	false	true	true
SPI3 global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true
I2C3 event interrupt	false	true	true
I2C3 error interrupt	false	true	true
I2C4 event interrupt	false	true	true
I2C4 error interrupt	false	true	true
TIM16 global interrupt	false	true	true
HSEM2 global interrupt	false	true	true

*** User modified value**

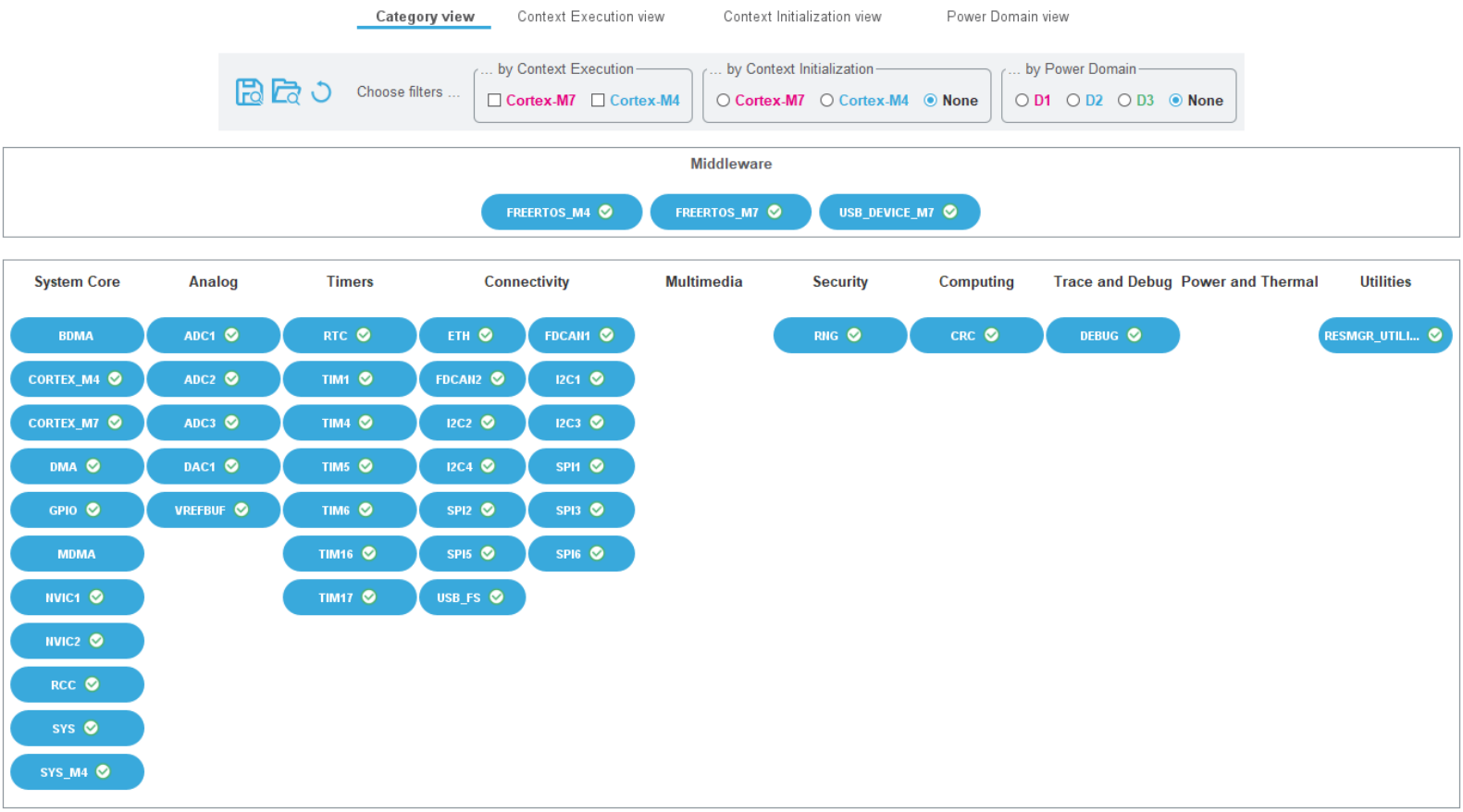
9. System Views

9.1. Category view

9.1.1. Current



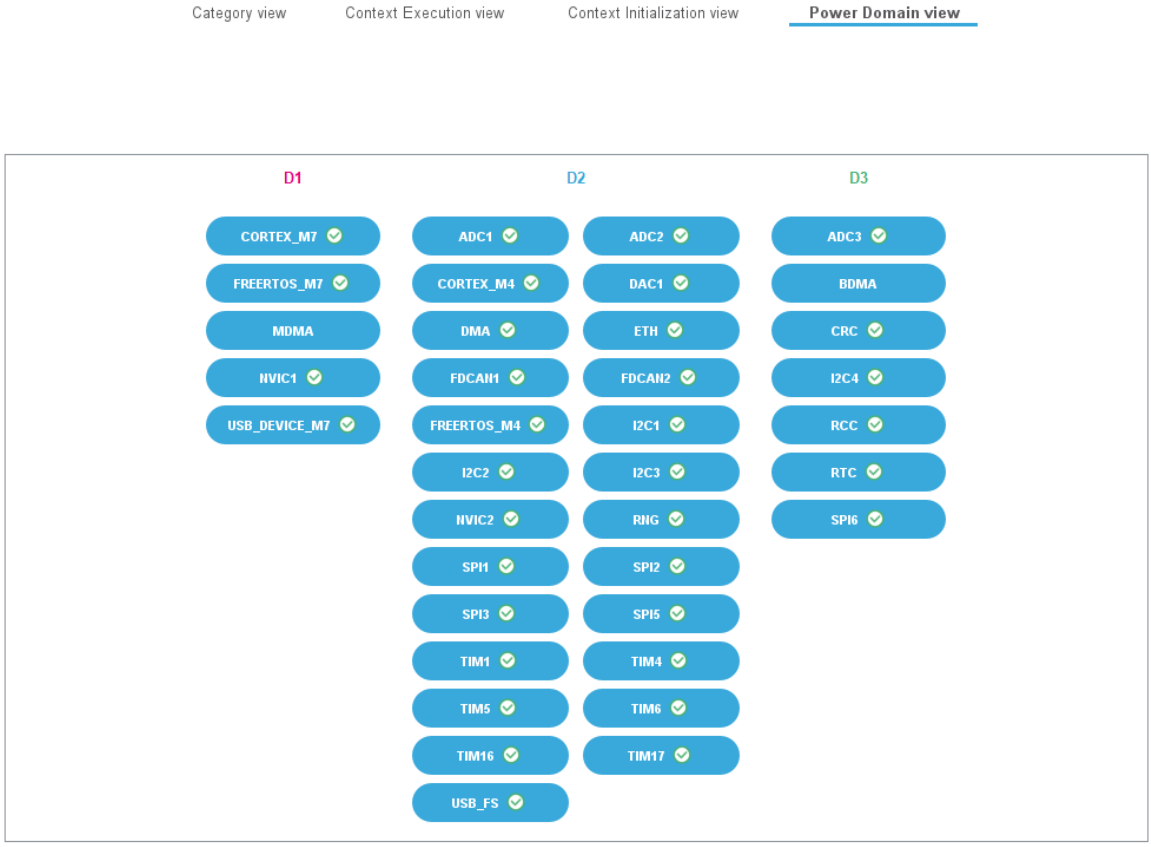
9.1.2. Without filters



9.2. Context Execution view

9.3. Context Initialization view

9.4. Power Domain view



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00600954.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00176879.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00530531.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00121475.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf

Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf
Application note	http://www.st.com/resource/en/application_note/DM00287603.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337873.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354333.pdf
Application note	http://www.st.com/resource/en/application_note/DM00356635.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00393275.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00525510.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00597308.pdf
Application note	http://www.st.com/resource/en/application_note/DM00622045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00623136.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00628458.pdf
Application note	http://www.st.com/resource/en/application_note/DM00660346.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf
Application note	http://www.st.com/resource/en/application_note/DM00733995.pdf