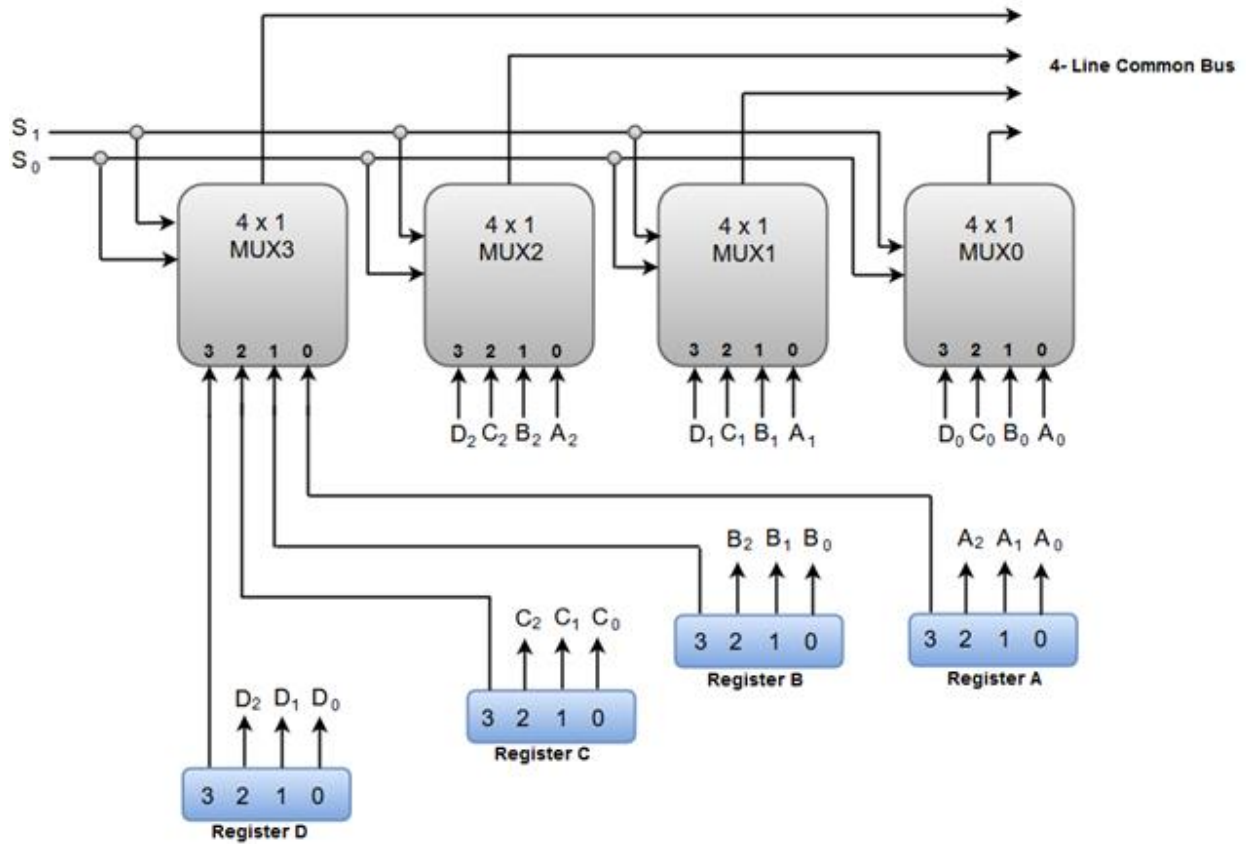


# Comman Bus System

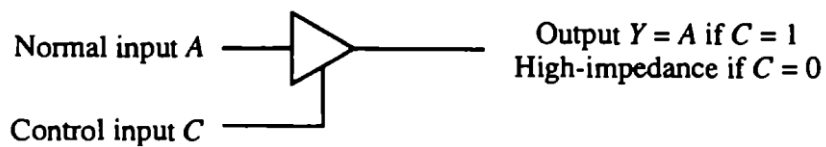
Bus System for 4 Registers:



$S_1$	$S_0$	Register selected
0	0	A
0	1	B
1	0	C
1	1	D

## Tri state Buffer

Figure 4-4 Graphic symbols for three-state buffer.



## Bus with Tri state Buffer

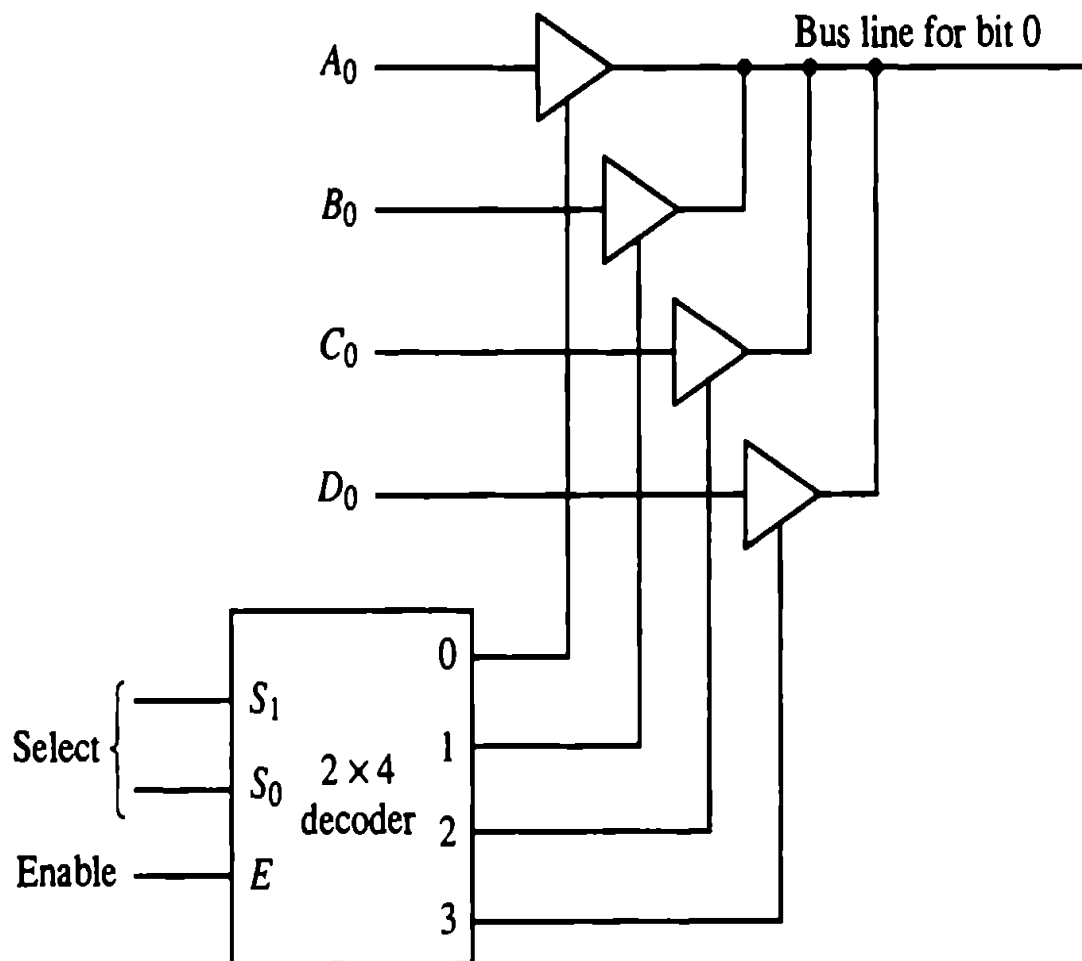


Figure 4-5 Bus line with three state-buffers.

## Binary Adder

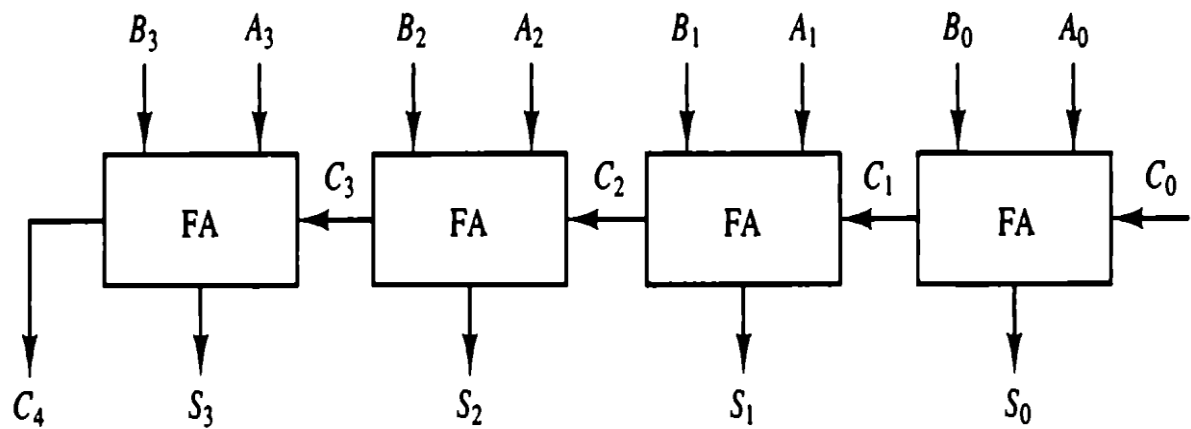


Figure 4-6 4-bit binary adder.

## Binary Subtractor

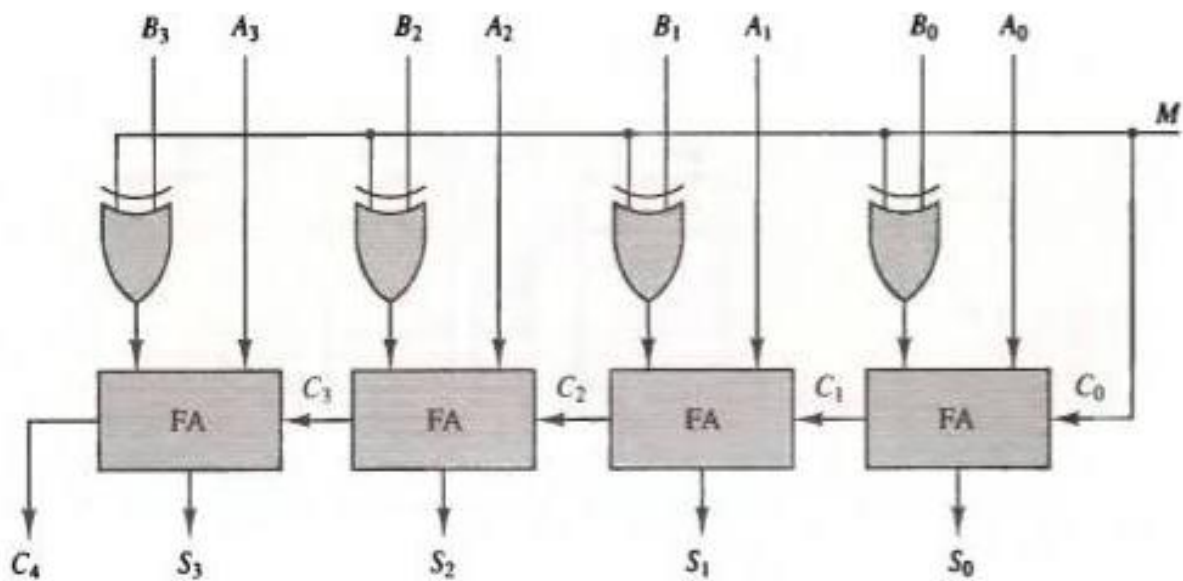


Figure 4-7 4-bit adder-subtractor.

## Binary Incrementer

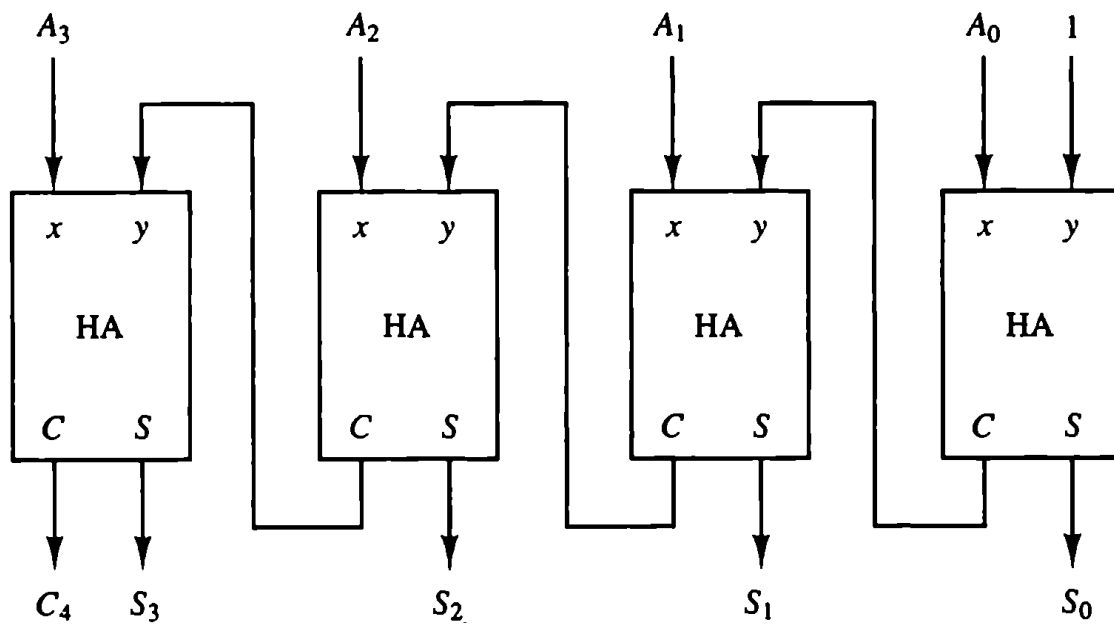


Figure 4-8 4-bit binary incrementer.

# Arithmetic Circuit

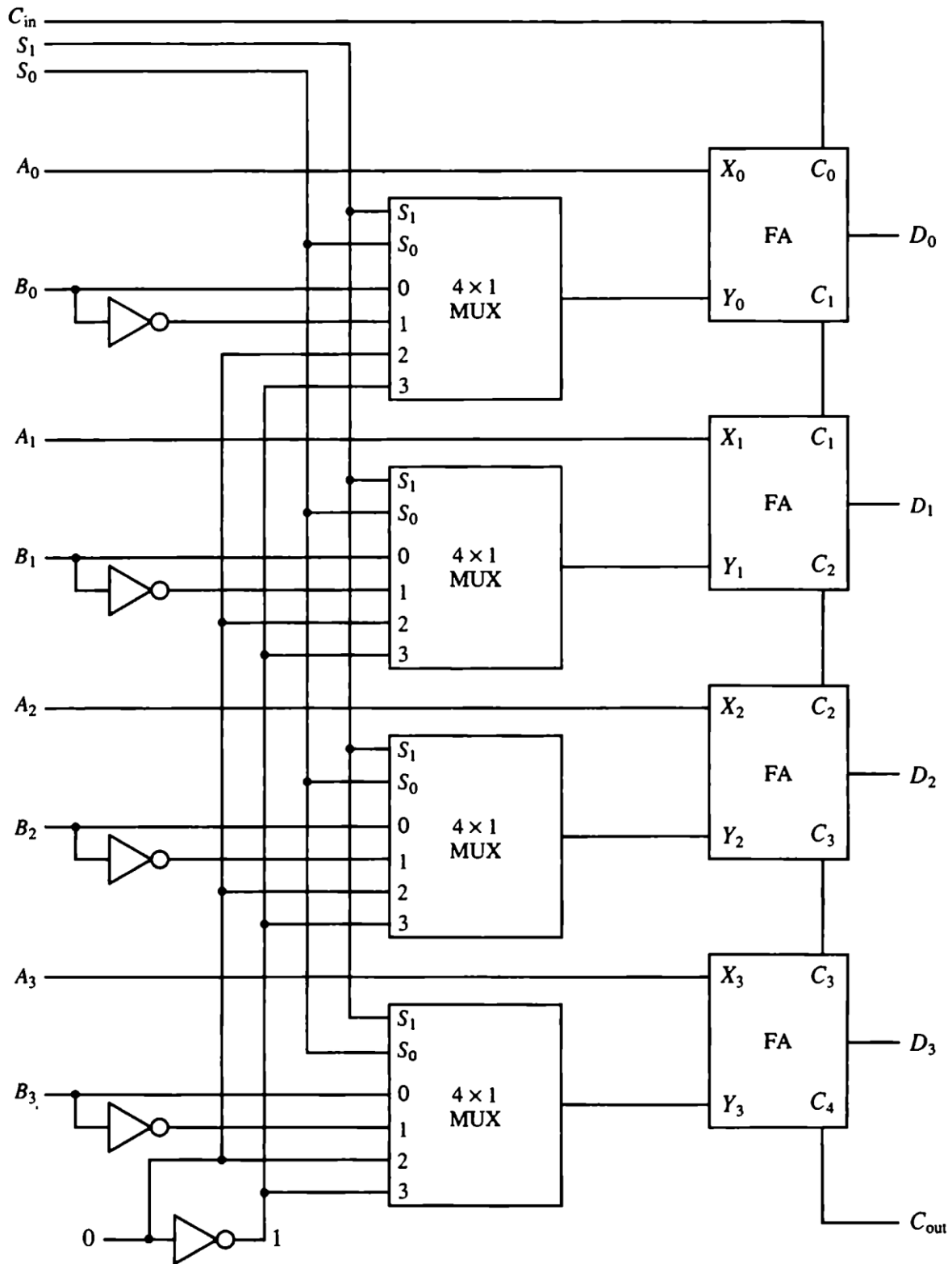


Figure 4-9 4-bit arithmetic circuit.

TABLE 4-4 Arithmetic Circuit Function Table

Select			Input $Y$	Output $D = A + Y + C_{in}$	Microoperation
$S_1$	$S_0$	$C_{in}$			
0	0	0	$B$	$D = A + B$	Add
0	0	1	$B$	$D = A + B + 1$	Add with carry
0	1	0	$\overline{B}$	$D = A + \overline{B}$	Subtract with borrow
0	1	1	$\overline{B}$	$D = A + \overline{B} + 1$	Subtract
1	0	0	0	$D = A$	Transfer $A$
1	0	1	0	$D = A + 1$	Increment $A$
1	1	0	1	$D = A - 1$	Decrement $A$
1	1	1	1	$D = A$	Transfer $A$

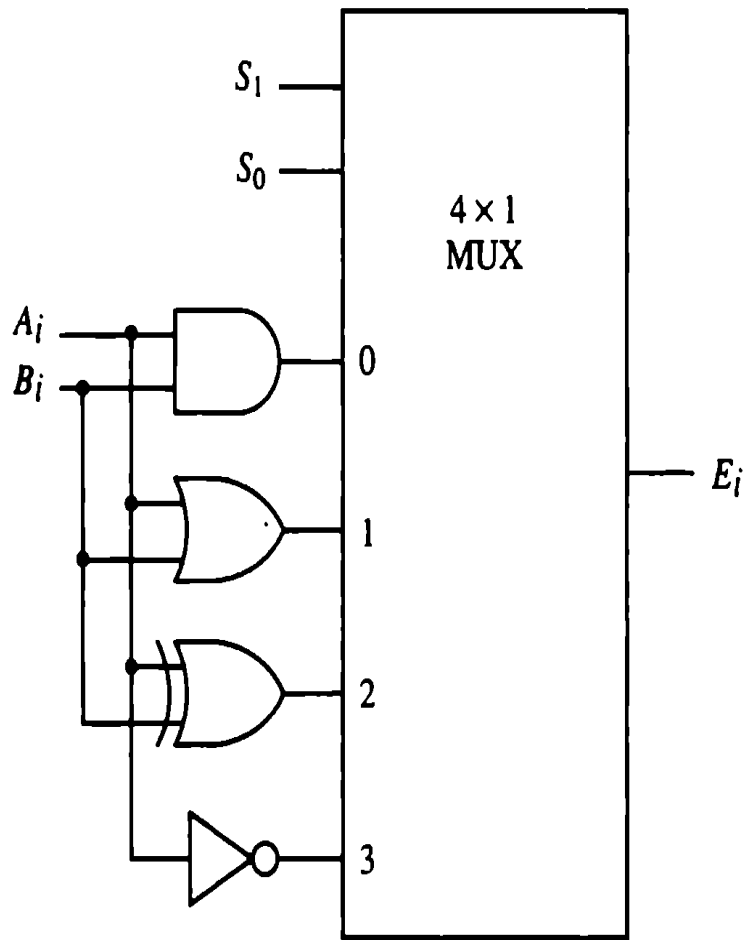
## List of 16 logic operation

TABLE 4-6 Sixteen Logic Microoperations

Boolean function	Microoperation	Name
$F_0 = 0$	$F \leftarrow 0$	Clear
$F_1 = xy$	$F \leftarrow A \wedge B$	AND
$F_2 = xy'$	$F \leftarrow A \wedge \overline{B}$	
$F_3 = x$	$F \leftarrow A$	Transfer $A$
$F_4 = x'y$	$F \leftarrow \overline{A} \wedge B$	
$F_5 = y$	$F \leftarrow B$	Transfer $B$
$F_6 = x \oplus y$	$F \leftarrow A \oplus B$	Exclusive-OR
$F_7 = x + y$	$F \leftarrow A \vee B$	OR
$F_8 = (x + y)'$	$F \leftarrow \overline{A \vee B}$	NOR
$F_9 = (x \oplus y)'$	$F \leftarrow \overline{A \oplus B}$	Exclusive-NOR
$F_{10} = y'$	$F \leftarrow \overline{B}$	Complement $B$
$F_{11} = x + y'$	$F \leftarrow A \vee \overline{B}$	
$F_{12} = x'$	$F \leftarrow \overline{A}$	Complement $A$
$F_{13} = x' + y$	$F \leftarrow \overline{A} \vee B$	
$F_{14} = (xy)'$	$F \leftarrow \overline{A \wedge B}$	NAND
$F_{15} = 1$	$F \leftarrow \text{all 1's}$	Set to all 1's

# Logic Circuit

Figure 4-10 One stage of logic circuit.

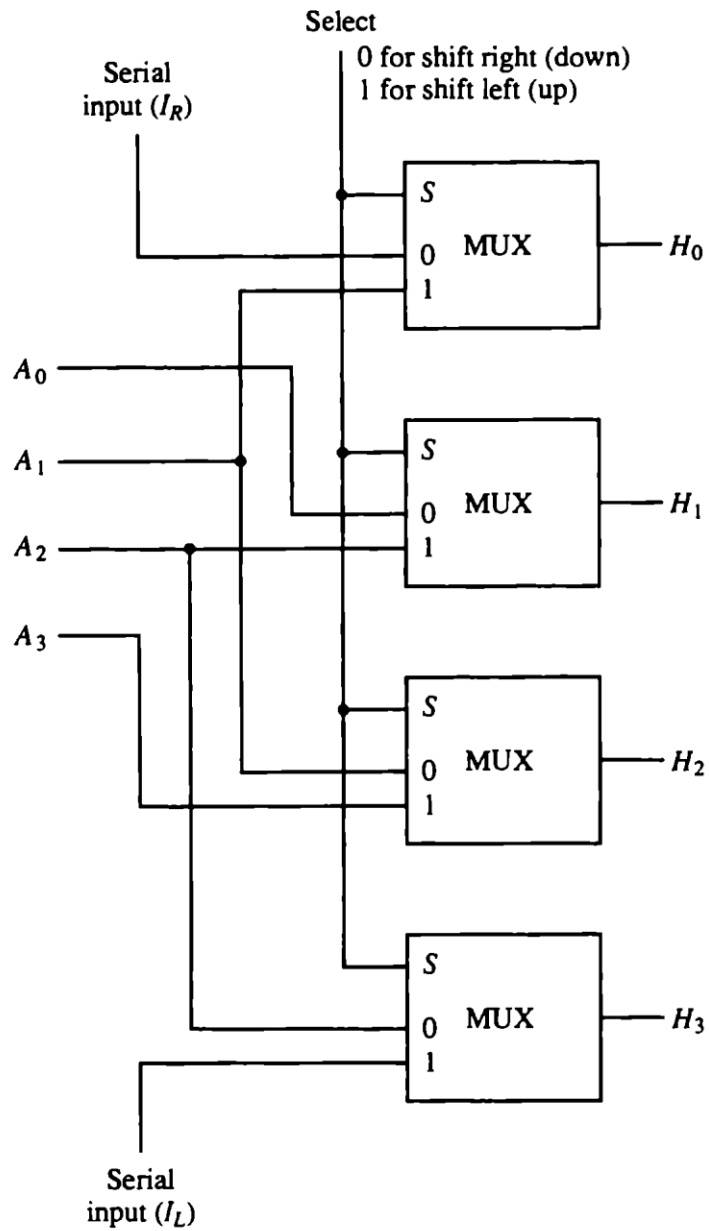


(a) Logic diagram

$S_1$	$S_0$	Output	Operation
0	0	$E = A \wedge B$	AND
0	1	$E = A \vee B$	OR
1	0	$E = A \oplus B$	XOR
1	1	$E = \bar{A}$	Complement

(b) Function table

# Shifter Circuit



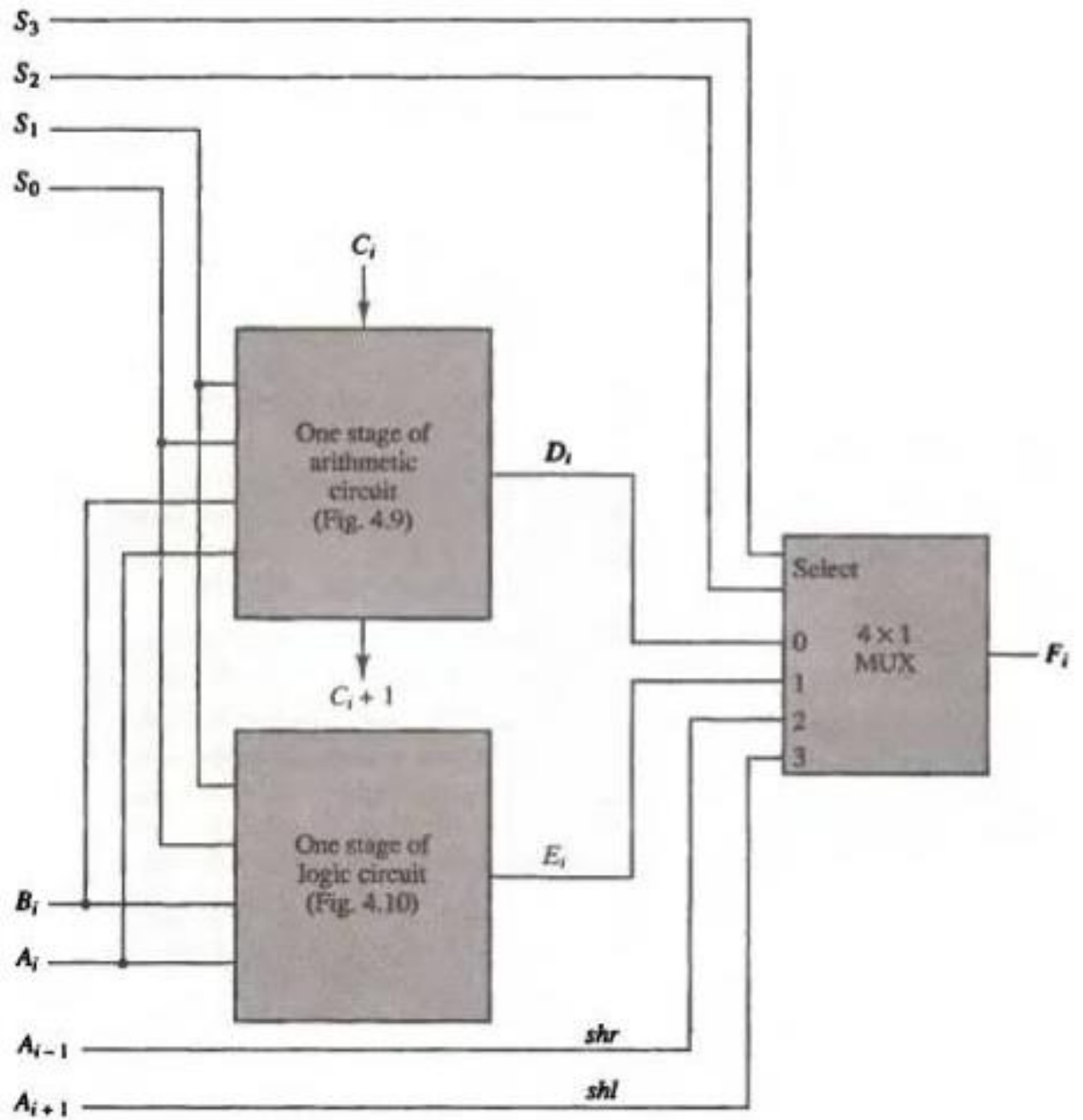
Function table				
Select	Output			
<i>S</i>	<i>H</i> <sub>0</sub>	<i>H</i> <sub>1</sub>	<i>H</i> <sub>2</sub>	<i>H</i> <sub>3</sub>
0	<i>I</i> <sub>R</sub>	<i>A</i> <sub>0</sub>	<i>A</i> <sub>1</sub>	<i>A</i> <sub>2</sub>
1	<i>A</i> <sub>1</sub>	<i>A</i> <sub>2</sub>	<i>A</i> <sub>3</sub>	<i>I</i> <sub>L</sub>

Figure 4-12 4-bit combinational circuit shifter.



## ALUS circuit

Figure 4-13 One stage of arithmetic logic shift unit.



**TABLE 4-8** Function Table for Arithmetic Logic Shift Unit

Operation select					Operation	Function
$S_3$	$S_2$	$S_1$	$S_0$	$C_{in}$		
0	0	0	0	0	$F = A$	Transfer $A$
0	0	0	0	1	$F = A + 1$	Increment $A$
0	0	0	1	0	$F = A + B$	Addition
0	0	0	1	1	$F = A + B + 1$	Add with carry
0	0	1	0	0	$F = A + \bar{B}$	Subtract with borrow
0	0	1	0	1	$F = A + \bar{B} + 1$	Subtraction
0	0	1	1	0	$F = A - 1$	Decrement $A$
0	0	1	1	1	$F = A$	Transfer $A$
0	1	0	0	$\times$	$F = A \wedge B$	AND
0	1	0	1	$\times$	$F = A \vee B$	OR
0	1	1	0	$\times$	$F = A \oplus B$	XOR
0	1	1	1	$\times$	$F = \bar{A}$	Complement $A$
1	0	$\times$	$\times$	$\times$	$F = \text{shr } A$	Shift right $A$ into $F$
1	1	$\times$	$\times$	$\times$	$F = \text{shl } A$	Shift left $A$ into $F$