Coa mcq - 3m xcgc 2

Computer System Architecture MCQ 01

1. RTL stands for:
a. Random transfer language
b. Register transfer language
c. Arithmetic transfer language
d. All of these

2. Which operations are used for addition, subtraction, increment, decrement and complement function:
a. Bus
b. Memory transfer
c. Arithmetic operation
d. All of these

3. Which language is termed as the symbolic depiction used for indicating the series:
a. Random transfer language
b. Register transfer language
c. Arithmetic transfer language
d. All of these

4. The method of writing symbol to indicate a provided computational process is called as a:
a. Programming language
b. Random transfer language
c. Register transfer language
d. Arithmetic transfer language

5. In which transfer the computer register are indicated in capital letters for depicting its function:
a. Memory transfer **b. Register transfer**
c. Bus transfer d. None of these

6. The register that includes the address of the memory unit is termed as the ____:
a. MAR b. PC
c. IR d. None of these

7. The register for the program counter is signified as_____:
a. MAR **b. PC**
c. IR d. None of these

8. In register transfer the instruction register as:
a. MAR b. PC
c. IR d. None of these

9. In register transfer the processor register as:
a. MAR b. PC
c. IR **d. RI**

10. How many types of micro operations:
a. 2 **b. 4**
c. 6 d. 8

11. Which are the operation that a computer performs on data that put in register:
a. Register transfer b. Arithmetic
c. Logical **d. All of these**

12. Which micro operations carry information from one register to another:
a. Register transfer b. Arithmetic
c. Logical d. All of these

13. Micro operation is shown as:
a. R1→R2 **b. R1←R2**
c. Both d. None

14. In memory transfer location address is supplied by____ that puts this on address bus:
a. ALU **b. CPU**
c. MAR d. MDR

15. How many types of memory transfer operation:
a. 1 **b. 2** c. 3 d. 4

16. Operation of memory transfer are:
a. Read b. Write
c. Both d. None

17. In memory read the operation puts memory address on to a register known as :
a. PC b. ALU
c. MAR d. All of these

18. Which operation puts memory address in memory address register and data in DR:
a. Memory read **b. Memory write**
c. Both d. None

19. Arithmetic operation are carried by such micro operation on stored numeric data available in_____:
a. Register b. Data
c. Both d. None

20. In arithmetic operation numbers of register and the circuits for addition at _____:
a. ALU b. MAR
c. Both d. None

21. Which operation are implemented using a binary counter or combinational circuit:
a. Register transfer **b. Arithmetic**
c. Logical d. All of these

22. Which operation is binary type, and are performed on bits string that is placed in register:
a. Logical micro operation
b. Arithmetic micro operation
c. Both
d. None

23. A micro operation every bit of a register is a:
a. Constant **b. Variable**
c. Both d. None

24. Which operation is extremely useful in serial transfer of data:
a. Logical micro operation
b. Arithmetic micro operation
c. Shift micro operation
d. None of these

25. Which language specifies a digital system which uses specified notation:
a. Register transfer b. Arithmetic
c. Logical d. All of these

26. IR stands for:
a. Input representation
b. Intermediate representation
c. Both d. None

27. HDL stands for:
a. Human description language
b. Hardware description language
c. Hardware description land
d. None of these

28. VPCC stands for:
a. Variable portable C compiler
b. Very portable C compiler
c. Both
d. None

29. In register transfer which system is a sequential logic system in which flip-flops and gates are constructed:
a. Digital system b. Register
c. Data d. None

30. High level language C supports register transfer technique for_____ application:
a. Executing b. Compiling
c. Both d. None

31. A counter is incremented by one and memory unit is considered as a collection of _____:
a. Transfer register **b. Storage register**
c. RTL d. All of these

32. Which is the straight forward register transfer the data from register to another register temporarily:
a. Digital system
b. Register
c. Data
d. Register transfer operations

33. In organization of a digital system register transfer of any digital system therefore it is called:
a. Digital system b. Register
c. Data **d. Register transfer level**

34. The binary information of source register chosen by:
a. Demultiplexer **b. Multiplexer**
c. Both d. None

35. Control transfer passes the function via control_____:
a. Logic b. Operation
c. Circuit d. All of these

36. Register are assumed to use positive-edge-triggered _____:
a. Flip-flop b. Logics
c. Circuit d. Operation

37. IDE stands for:
a. Input device electronics
b. Integrated device electronic
c. Both d. None

38. ATA stands for:
a. Advance technology attachment
b. Advance teach attachment
c. Both d. None

39. The memory bus is also referred as_____:
a. Data bus b. Address bus
c. Memory bus d. All of these

40. How many parts of memory bus:
a. 2 b. 3
c. 5 d. 6

41. A three state gate defined as:
a. Analog circuit b. Analog fundamentals
c. Both a&b **d. Digital circuit**

42. In 3 state gate two states act as signals equal to:
a. Logic 0 b. Logic 1
c. None of these **d. Both a & b**

43. In 3 state gate third position termed as high impedance state which acts as:
a. Open circuit b. Close circuit
c. None of these d. All of above

44. In every transfer, selection of register by bus is decided by:
a. Control signal b. No signal
c. All signal d. All of above

45. Every bit of register has:
a. 2 common line b. 3 common line
c. 1 common line d. none of these

46. DDR2 stands for:
a. Double data rate 2
b. Data double rate 2
c. Dynamic data rate 2
d. Dynamic double rate 2

47. SDRAM stands for:
a. System dynamic random access memory
b. Synchronous dynamic random access memory c. Both d. None

48. Which is referred as a sequential circuit which contains the number of register as per the protocol:
a. RTL **b. RAM**
c. MAR d. All of these

49. Which operation refer bitwise manipulation of contents of register:
a. Logical micro operation
b. Arithmetic micro operation
c. Shift micro operation
d. None of these

50. Which symbol will be used to denote an micro operation:
a. (^) **b. (v)**
c. Both d. None

51. which symbol will be denote an AND micro operation:
a. (^) b. (v)
c. Both d. None

52. Which operation are associated with serial transfer of data:
a. Logical micro operation
b. Arithmetic micro operation
c. Shift micro operation
d. None of these

53. The bits are shifted and the first flip-flop receives its binary information from the_____:
a. Serial output **b. Serial input**
c. Both d. None

54. How many types of shift micro operation:
a. 2 b. 4 **c. 6** d. 8

55. Which shift is a shift micro operation which is used to shift a signed binary number to the left or right:
a. Logical **b. Arithmetic**
c. Both d. None of these

56. Which shift is used for signed binary number:
a. Logical **b. Arithmetic**
c. Both d. None of these

57. Arithmetic left shift is used to multiply a signed number by_____:
a. One **b. Two**
c. Three d. All of these

58. The variable of_____ correspond to hardware register:
a. RAM **b. RTL**
c. ALU d. MAR

59. In which shift is used to divide a signed number by two:
a. Logical right-shift
b. Arithmetic right shift
c. Logical left shift
d. Arithmetic left shift

60. Shift left is equal to:
a. **multiply by two**
b. add by two
c. divide by two
d. subtract by two

Computer System Architecture MCQ 02

1. _____ is a command given to a computer to perform a specified operation on some given data:
a. An instruction b. Command
c. Code d. None of these

2. An instruction is guided by_____ to perform work according:
a. PC b. ALU c. Both a and b **d. CPU**

3. Two important fields of an instruction are:
a. Opcode b. Operand
c. Only a **d. Both a & b**

4. Each operation has its _____ opcode:
a. Unique b. Two
c. Three d. Four

5. which are of these examples of Intel 8086 opcodes:

a. MOV b. ADD c. SUB
d. All of these

6. _____specify where to get the source and destination operands for the operation specified by the _____:
a. Operand fields and opcode
b. Opcode and operand
c. Source and destination
d. CPU and memory

7. The source/destination of operands can be the_____ or one of the general-purpose register:
a. Memory b. One
c. both d. None of these

8. The complete set of op-codes for a particular microprocessor defines the_____ set for that processor:
a. Code b. Function
c. Module **d. Instruction**

9. Which is the method by which instructions are selected for execution:
a. Instruction selection
b. Selection control
c. Instruction sequencing
d. All of these

10. The simplest method of controlling sequence of instruction execution is to have each instruction explicitly specify:
a. The address of next instruction to be run
b. Address of previous instruction
c. Both a & b
d. None of these

11. As the instruction length increases _____ of instruction addresses in all the instruction is_____:
a. Implicit inclusion
b. Implicit and disadvantageous
c. Explicit and disadvantageous
d. Explicit and disadvantageous

12. _____is the sequence of operations performed by CPU in processing an instruction:
a. Execute cycle
b. Fetch cycle
c. Decode
d. Instruction cycle

13. The time required to complete one instruction is called:
a. Fetch time
b. Execution time
c. Control time
d. All of these

14. _____is the step during which a new instruction is read from the memory:
a. Decode
b. Fetch
c. Execute
d. None of these

15. _____is the step during which the operations specified by the instruction are executed:
a. Execute
b. Decode
c. Both a& b
d. None of these

16. Decode is the step during which instruction is_____:
a. Initialized
b. Incremented
c. Decoded
d. Both b & c

17. The instruction fetch operation is initiated by loading the contents of program counter into the_____ and sends_____ request to memory:
a. Memory register and read
b. Memory register and write
c. Data register and read
d. Address register and read

18. The contents of the program counter is the _____ of the instruction to be run:
a. Data
b. Address
c. Counter
d. None of these

19. The instruction read from memory is then placed in the_____ and contents of program counter is_____ so that it contains the address of_____ instruction in the program:
a. Program counter, incremented and next
b. Instruction register, incremented and previous
c. Instruction register, incremented and next
d. Address register, decremented and next

20. Execution of instruction specified by instruction to perform:
a. Operation
b. Operands
c. Both a & b
d. None of these

21. _____ is a symbolic representation of discrete elements of information:
a. Data
b. Code
c. Address
d. Control

22. Group of binary bits(0&1) is known as:
a. Binary code
b. Digit code
c. Symbolic representation
d. None of these

23. A group of 4 binary bits is called:
a. Nibble
b. Byte
c. Decimal
d. Digit

24. BCD uses binary number system to specify decimal numbers:
a. 1-10
b. 1-9
c. 0-9
d. 0-10

25. The _____ are assigned according to the position occupied by digits:
a. Volume
b. Weight
c. Mass
d. All of these

26. what is the BCD for a decimal number 559:
a. $[0101\ 0101\ 1001]_{BCD}$
b. [0101 0001 1010]
c. [0101 1001 1001]
d. [1001 1010 0101]

27. _____are the codes that represent alphabetic characters, punctuation marks and other special characters:
a. Alphanumeric codes
b. ASCII codes
c. EBCDIC codes
d. All of these

28. Abbreviation ASCII stands for:
a. American standard code for information interchange
b. Abbreviation standard code for information interchange
c. Both
d. None of these

29. How many bit of ASCII code:
a. 6
b. 7
c. 5
d. 8

30. Which code used in transferring coded information from keyboards and to computer display and printers:
a. ASCII
b. EBCDIC
c. Both
d. None of these

31. Which code used to represent numbers, letters, punctuation marks as well as control characters:
a. ASCII
b. EBCDIC
c. Both
d. None of these

32. abbreviation EBCDIC stand for:
a. Extended binary coded decimal interchange code
b. External binary coded decimal interchange code
c. Extra binary coded decimal interchange code
d. None of these

33. How many bit of EBCDIC code:
a. 7
b. 8
c. 5
d. 9

34. Which code the decimal digits are represented by the 8421 BCD code preceded by 1111:
a. ASCII
b. EBCDIC
c. Both
d. None of these

35. _____ has the property that corrupting or garbling a code word will likely produce a bit string that is not a code word:
a. Error deleting codes
b. Error detecting codes
c. Error string codes
d. None of these

36. Which is method used most simple and commonly:
a. Parity check method
b. Error detecting method
c. Both
d. None of these

37. Which is the method of parity:
a. Even parity method
b. Odd parity method
c. Both
d. None of these

38. The ability of a code to detect single errors can be stated in term of the _____:
a. Concept of distance
b. Even parity
c. Odd parity
d. None of these

39. The first n bit of a code word called _____ may be any of the 2^n n- bit string minimum error bit:
a. Information bits
b. String bits
c. Error bits
d. All of these

40. A code in which the total number of 1s in a valid (n+1) bit code word is even, this is called an _____:
a. Even parity code
b. Odd parity code
c. Both
d. None of these

41. A code in which the total number of 1s in a valid (n+1)bit code word is odd and this code is called an_____:
a. Error detecting code
b. Even parity code
c. Odd parity code
d. None of these

42. a code is simply a subset of the vertices of the _____:
a. n bit **b. n cube**
c. n single d. n double

43. Which method is used to detect double errors and pinpoint erroneous bits:
a. Even parity method
b. Odd parity method
c. Check sum method
d. All of these

44. A code that is used to correct error is called an _____:
a. Error detecting code
b. Error correcting code
c. Both
d. None of these

45. A received _____with a bit error will be closer to the originally transmitted code word than to any other code word:
a. Code word
b. Non code word
c. Decoding
d. All of these

46. Which code word was originally transmitted to produce a received word is called:
a. Non code word
b. Code word
c. Decoding
d. None of these

47. The hardware that does this is an _____:
a. Error detecting decoder
b. Error correcting decoder
c. Both
d. None of these

48. Hamming codes was developed in _____:
a. 1953
b. 1950
c. 1945
d. 1956

49. _____ between two code words is defined as the number of bits that must be changed for one code to another:
a. Hamming codes
b. Hamming distance
c. Both
d. None of these

50. It is actually a method for constructing codes with a minimum distance of ____:
a. 2
b. 4
c. 3
d. 5

51. The bit position in a _____ can be numbered from 1 through 2^i-1:
a. Hamming code word
b. Hamming distance word
c. Both
d. None of these

52. Each check bit is grouped with the information bits as specified by a_____:
a. Parity check code
b. Parity check matrix
c. Parity check bit
d. All of these

53. The pattern of groups that have odd parity called the _____must match one of the of columns in the parity check matrix:
a. Syndrome
b. Dynodes
c. Both
d. None of these

54. Which are designed to interpret a specified number of instruction code:
a. Programmer
b. Processors
c. Instruction
d. Opcode

55. Which code is a string of binary digits:
a. Op code
b. Instruction code
c. Parity code
d. Operand code

56. The list of specific instruction supported by the CPU is termed as its _____:
a. Instruction code
b. Parity set
c. Instruction set
d. None of these

57. _____is divided into a number of fields and is represented as a sequence of bits:
a. instruction
b. instruction set
c. instruction code
d. parity code

58. Which unit is necessary for the execution of instruction:
a. Timing
b. Control
c. Both
d. None of these

59. Which unit provide status , timing and control signal:
a. Timing and control unit
b. Memory unit
c. Chace unit
d. None of these

60. Which unit acts as the brain of the computer which control other peripherals and interfaces:
a. Memory unit
b. Cache unit
c. Timing and control unit
d. None of these

61. It contains the _____stack for PC storage during subroutine calls and input/output interrupt services:
a. Seven- level hardware
b. Eight- level hardware
c. One- level hardware
d. Three- level hardware

62. Which unit works as an interface between the processor and all the memories on chip or off- chip:
a. Timing unit
b. Control unit
c. Memory control unit
d. All of these

63. The maximum clock frequency is_____:
a. 45 MHZ
b. 50 MHZ
c. 52 MHZ
d. 68 MHZ

64. _____ is given an instruction in machine language this instruction is fetched from the memory by the CPU to execute:
a. ALU
b. CPU
c. MU
d. All of these

65. Which cycle refers to the time period during which one instruction is fetched and executed by the CPU:
a. Fetch cycle
b. Instruction cycle
c. Decode cycle
d. Execute cycle

66. How many stages of instruction cycle:
a. 5
b. 6
c. 4
d. 7

67. Which are stages of instruction cycle:
a. Fetch b. Decode
c. Execute
d. Derive effective address of the instruction
e. All of these

68. Which instruction are 32 bits long , with extra 16 bits:
a. Memory reference instruction
b. Memory reference format
c. Both d. None of these

69. Which is addressed by sign extending the 16-bit displacement to 32-bit:
a. Memory address**b. Effectivememory address**
c. Both a and b d. None of these

70. Which are instruction in which two machine cycle are required:
a. Instruction cycle
b. Memory reference instruction
c. Both d. None of these

71. Which instruction are used in multithreaded parallel processor architecture:
a. Memory reference instruction
b. Memory reference format
c. Both d. None of these

72. Which instruction are arranged as per the protocols of memory reference format of the input file in a simple ASCII sequence of integers between the range 0 to 99 separated by spaces without formatted text and symbols:
a. Memory reference instruction
b. Memory reference format
c. Both
d. None of these

73. _____ is an external hardware event which causes the CPU to interrupt the current instruction sequence:
a. Input interrupt b. Output interrupt
c. Both d. None of these

74. ISR stand for:
a. Interrupt save routine
b. Interrupt service routine
c. Input stages routine
d. All of these

75. Which interrupt services save all the register and flags:
a. Save interrupt
b. Input/output interrupt
c. Service interrupt
d. All of these

76. IRET stand for:
a. Interrupt enter
b. Interrupt return
c. Interrupt delete
d. None of these

77. Which are benefit of input/output interrupt:
a. It is an external analogy to exceptions
b. The processor initiates and perform all I/O operation
c. The data is transferred into the memory through interrupt handler
d. All of these

78. Which are the not causes of the interrupt:
a. In any single device
b. In processor poll devices
c. It is an external analogy to exception
d. None of these

79. Which are the causes of the interrupt:
a. In any single device
b. In processor poll devices
c. In a device whose ID number is stored on the address bus **d. All of these**

80. Which are the functioning of I/O interrupt:
a. The processor organizes all the I/O operation for smooth functioning
b. After completing the I/O operation the device interrupt the processor
c. Both d. None of these

81. _____with which computers perform is way beyond human capabilities:
a. Speed b. Accuracy
c. Storage d. Versatility

82. _____ of a computer is consistently:
a. Speed **b. Accuracy**
c. Storage d. Versatility

83. GIGO stand for:
a. Garbage-in-garbage-out
b. Garbage-in garbage-occur
c. Both d. None of these

84. How many basic operations of versatility:
a. 5 b. 6 **c. 4** d. 7

85. Which are the operation of versatility:
a. exchange of information with the outside world via I/O device
b. Transfer of data internally with in the central processing unit
c. Performs of the basic arithmetic operations
d. All of these

86. _____ of information in a human brain and a computer happens differently:
a. Intelligence **b. Storage**
c. Versatility d. Diligence

87. Which are the basic operation for converting:
a. Inputting b. Storing c. Processing
d. Outputting e. Controlling
f. All of these

88. The control unit and arithmetic logic unit are know as the _____:
a. Central program unit **b. CPU**
c. Central primary unit d. None

89. Which unit is comparable to the central nervous system in the human body:
a. Output unit **b. Control unit**
c. Input unit d. All of these

90. _____ of the primary memory of the computer is limited:
a. Storage capacity b. Magnetic disk
c. Both d. None of these

91. Information is handled in the computer by _____:
a. Electrical digit **b. Electrical component**
c. Electronic bit d. None of these

92. 0 and 1 are know as _____:
a. Byte **b. Bit** c. Digits d. Component

93. 0 and 1 abbreviation for:
a. Binary digit b. Octal digit
c. Both d. None of these

94. How many bit of nibble group:
a. 5 **b. 4** c. 7 d. 8

95. How many bit of bytes:
a. 3 b. 4 c. 6 **d. 8**

96. Which is the most important component of a digit computer that interprets the instruction and processes the data contained in computer programs:
a. MU b. ALU **c. CPU** d. PC

97. Which part work as a the brain of the computer and performs most of the calculation:
a. MU b. PC c. ALU **d. CPU**

98. Which is the main function of the computer:
a. Execute of programs
b. Execution of programs
c. Both
d. None of these

99. How many major component make up the CPU:
a. 4 **b. 3** c. 6 d. 8

100. Which register holds the current instruction to be executed:
a. Instruction register
b. Program register
c. Control register
d. None of these

101. Which register holds the next instruction to be executed:
a. Instruction register
b. Program register
c. Program control register
d. None of these

102. Each instruction is also accompanied by a_____:
a. Microprocessor
b. Microcode
c. Both
d. None of these

103. Which are microcomputers commonly used for commercial data processing, desktop publishing and engineering application:
a. Digital computer
b. Personal computer
c. Both
d. None of these

104. Which microprocessor has the control unit, memory unit and arithmetic and logic unit:
a. Pentium IV processor
b. Pentium V processor
c. Pentium III processor
d. None of these

105. The processing speed of a computer depends on the _____of the system:
a. Clock speed
b. Motorola
c. Cyrix
d. None of these

106. Which microprocessor is available with a clock speed of 1.6 GHZ:
a. Pentium III b. Pentium II
c. Pentium IV d. All of these

107. Which processor are used in the most personal computer:
a. Intel corporation's Pentium
b. Motorola corporation's
c. Both
d. None of these

Computer System Architecture MCQ 03

1. _____is the first step in the evolution of programming languages:
a. machine language
b. assembly language
c. code language
d. none of these

2. Mnemonic refers to:
a. Instructions
b. Code
c. Symbolic codes
d. Assembler

3. Mnemonic represent:
a. Operation codes
b. Strings
c. Address
d. None of these

4. To represent addresses in assembly language we use:
a. String characters
b. Arrays
c. Structure
d. Enum

5. Assembler works to convert assembly language program into machine language :
a. Before the computer can execute it
b. After the computer can execute it
c. In between execution
d. All of these

6. _____generation computers use assembly language:
a. First generation
b. Third generation
c. second generation
d. fourth generation

7. Assembly language program is called:
a. Object program
b. Source program
c. Oriented program
d. All of these

8. To invoke assembler following command are given at command line:
a. $ hello.s -o hello.o
b. $as hello.s –o o
c. $ as hello –o hello.o
d. $ as hello.s –o hello.o

9. By whom address of external function in the assembly source file supplied by _____ when activated:
a. Assembler
b. Linker
c. Machine
d. Code

10. An_____ -o option is used for:
a. Input file
b. External file
c. Output file
d. None of these

11. The assembler translates ismorphically_____ mapping from mnemonic in these statements to machine instructions:
a. 1:1
b. 2:1
c. 3:3
d. 4:1

12. Assembler works in_____ phases:
a. 1
b. 3
c. 2
d. 4

13. The assembler in first pass reads the program to collect symbols defined with offsets in a table_____:
a. Hash table
b. Symbol table
c. Both a& b
d. None of these

14. In second pass, assembler creates _____in binary format for every instruction in program and then refers to the symbol table to giving every symbol an_____ relating the segment.
a. Code and program
b. Program and instruction
c. Code and offset
d. All of these

15. which of the 2 files are created by the assembler:
a. List and object file
b. Link and object file
c. Both a & b
d. None of these

16. In which code is object file is coded:
a. Link code
b. Decimal code
c. Assembly code
d. Binary code

17. which type of errors are detected by the assembler:
a. syntax error
b. logical error
c. run time error
d. none of these

18. MOVE AX BX in this LINES OF CODE what type of error is declared:
a. Undeclared identifier MOVE
b. undeclared identifier AX
c. Accept as a command
d. Not look in symbol table

19. In given lines of code MOV AX,BL have different type of operands according to assembler for 8086 architecture these identifiers must be of:
a. Different type only in byte
b. Same type either in word or byte
c. Both a & b
d. None of these

20. What type of errors are not detected by assemblers:
a. Syntax error
b. Run time error
c. Logical error
d. All of these

21. _____serves as the purpose of documentation only:
a. List b. object
c. link d. code

22. An assembler is a utility program that performs:
a. Isometric translation
b. Isomorphic translation
c. Isochoric translation
d. None of these

23. Assemblers are of 2 types:
a. 1 pass
b. 2 pass
c. both a & b
d. none of these

24. CP/CMS assembly language was written in _____assembler:
a. S/340 b. S-350
c. S/320 **d. S/360**

25. ASM-H widely used _____assembler:
a. S/370
b. S/380
c. S/390
d. S/360

26. Assembler is a_____:
a. Interpreter
b. Translator
c. Exchanger
d. None of these

27. A_____ processor controls repetitious writing of sequence:
a. Macro
b. Micro
c. Nano
d. All of these

28. IBM-360 type language is example which supporting_____ language:
a. Micro
b. Macro
c. Both a & b
d. None of these

29. _____ is attached to using macro instruction definition:
a. Name
b. Definition
c. Identifier
d. All of these

30. END of macro definition by:
a. NAME
b. MEND
c. DATA
d. MEMORY

31. Process of replacing the sequence of lines of codes is known as:
a. Expanding die macro
b. Expanding tri macro
c. Tetra macro
d. None of these

32. A program that links several programs is called:
a. Linker
b. Loader
c. Translator
d. None of these

33. _____address is not assigned by linker:
a. Absolute
b. Relative
c. Both a & b
d. None of these

34. _____address is provided by linker to modules linked together that starting from_____:

a. Absolute and 0
b. Relative and 0
c. Relative and 1
d. Relative and 3

35. A linker is also known as:

a. Binder
b. Linkage editor
c. Both a & b
d. None of these

36. Loading is _____ with the task of storage management of operating system and mostly preformed after assembly:

a. Bound
b. Expanded
c. Overlaps
d. All of these

37. _____contain library program have to be indicated to the loader:

a. Externally defined
b. Internally defined
c. Executable file
d. All of these

38. It is the task of the _____to locate externally defined symbols in programs, load them in to memory by placing their _____of symbols in calling program:

a. Loader and name
b. Linker and values
c. Linker and name
d. Loader and values

39. Linker creates a link file containing binary codes and also produces_____ containing address information on linked files:

a. Link map
b. Map table
c. Symbol map
d. None of these

40. how many types of entities contained by assembler to handle program:
a. 4
b. 2
c. 3
d. 5

41. which of the following are types of assembler entities:

a. Absolute entities
b. Relative entities
c. Object program
d. All of these

42. _____have addresses where instructions are stored along with address of working storage:

a. Relative entities
b. Absolute entities
c. Both a & b
d. None of these

43. Absolute entities are _____whom value signify storage locations that are independent of resulting machine code:
a. Numeric constants
b. String constants
c. Fixed addresses
d. Operation codes
e. All of these

44. A module contains machine code with specification on_____:
a. Relative addresses
b. Absolute addresses
c. Object program
d. None of these

45. After actual locations for main storage are known, a _____adjusts relative addresses to these actual locations:
a. Relocating loader
b. Locating loader
c. Default loader
d. None of these

46. If there is a module from single source-language only that does not contain any external references, it doesn't need a linker to load it and is loaded_____:

a. Indirectly
b. Directly
c. Extending
d. None of these

47. Modern assemblers for RISC based architectures make optimization of instruction scheduling to make use of CPU _____efficiently:
a. Pipeline
b. Without pipeline
c. Both a & b
d. None of these

48. which are of the following modern assemblers:
a. MIPS
b. Sun SPARC
c. HP PA-RISC
d. x86(x64)
e. all of these

49. How many types of loop control structures in C language:

a. 4
b. 5
c. 2
d. 3

50. Types of loop control statements are:

a. For loop
b. While loop
c. Do-while loop
d. All of these

51. <Initial value> is_____ which initializes the value of variable:

a. Assignment expression
b. Condition value
c. Increment/decrement
d. None of these

52. The format "%8d" is used to print_____ values in a line:
a. 11
b. 10
c. 9
d. 12

53. <Condition> is a _____expression which will have value true or false:
a. Relational
b. Logical
c. Both a & b
d. None of these

54. <Increment> is the_____ value of variable which will be added every time:
a. Increment
b. Decrement
c. Expanding
d. None of these

55. _____is the statement block of for loop lies inside block of another for loop:
a. Nested for loop
b. Nested while loop
c. Nested do-while loop
d. None of these

56. SPARC stands for:
a. Scalable programmer architecture
b. Scalable processor architecture
c. Scalable point architecture
d. None of these

57. Full form of MIPS assembler is:
a. Microprocessor without interlocked pipeline stage
b. Microprocessor with interlocked pipeline stage
c. Both a & b
d. None of these

58. _____ statement block is executed atleast once for any value of the condition:
a. For statement
b. Do-while statement
c. While statement
d. None of these

59. _____statement is an unconditional transfer of control statement:
a. Goto
b. Continue
c. Switch
d. All of these

60. In Goto statement the place to which control is transferred is identified by a statement_____:
a. Label
b. Display
c. Break
d. None of these

61. The continue statement is used to transfer the control to the_____ of a statement block in a loop:
a. End
b. Beginning
c. Middle
d. None of these

62. The_____ statement is used to transfer the control to the end of statement block in a loop:

a. Continue
b. Break
c. Switch
d. Goto

63. _____function is used to transfer the control to end of a program which uses one argument( ) and takes value is zero for_____ termination and non-zero for _____termination:
a. Exit( ),normal, abnormal
b. Break, normal, abnormal
c. Both a & b
d. None of these

64. To design a program it requires_____:
a. Program specification
b. Code specification
c. Instruction specification
d. Problem specification

65. Testing helps to ensure _____of the program for use within a system:
a. Quality, accuracy and except
b. Quality, accuracy and acceptance
c. Design, assurance and acceptance
d. Quality, accuracy and development

66. An unstructured program uses a _____ approach to solve problems:

a. Linear
b. Top down
c. Both a & b
d. None of these

67. In a complex program, the _____overlaps:

a. Branching
b. Condition
c. Both a & b
d. None of these

68. How many structures structured programs are written:

a. 3
b. 2
c. 1
d. 6

69. following are structured programs written in simple structures:

a. Sequence
b. Selection
c. Iteration
d. All of these

70. Iteration also called:

a. Repetition
b. Straight
c. Selection
d. Sequence

71. In _____instructions are followed one after the other in the preset order in which they appear within program:
a. Sequence
b. Selection
c. Break
d. Iteration

72. _____means that one of two alternative sequences of instruction is chosen based on logical condition:
a. Sequence
b. Selection
c. Repetition
d. None of these

73. _____is sequence of instructions is executed and repeated any no. of times in loop until logical condition is true:

a. Iteration
b. Repetition
c. Both a & b
d. None of these

74. A _____is a small program tested separately before combining with final program:

a. Module
b. Block
c. selection
d. none of these

75. _____uses various symbols to represent function within program and is _____representation:

a. Flowchart, pictorial
b. Algorithm, pictorial
c. Pictorial, flowchart
d. None of these

76. _____Avoid crossing flow lines:

a. Flowchart
b. Algorithm
c. Both a & b
d. None of these

77. A flow chart is drawn from top to bottom and_____:

a. Right to left
b. Only right
c. Left to right
d. Only left

78. Flowchart that exceed page should be properly linked using _____to portions of flowchart on different pages:
a. Connectors
b. Interconnections
c. Connections
d. None of these

79. _____is useful to prepare detailed program documentation:

a. Flowchart
b. Algorithm
c. Both a & b
d. None of these

80. Pseudo means:

a. Imitation
b. Imitate
c. In imitation
d. None of these

81. Preparing the pseudocode requires _____time than drawing flowchart:

a. Less
b. More
c. Optimum
d. None of these

82. There is _____standard for preparing pseudocode instructions:

a. No
b. 4
c. 2
d. 6

83. _____are used to translate high level language instructions to a machine code:

a. Translators
b. Interpreters
c. Compilers
d. None of these

84. The compiler _____translate a program code with any syntax error:

a. Can
b. Cannot
c. Without
d. None of these

85. Before checking the program for errors in translating code into machine language the high level language code is loaded into_____:

a. Register
b. Memory
c. Data
d. CPU

86. After compilation of the program ,the operating system of computer activates:

a. Loader
b. Linker
c. Compiler
d. None of these

87. The linker has utilities needed for _____within the translated program:

a. Input
b. Output
c. Processing
d. All of these

88. Flowchart is a_____ representation of an algorithm:

a. Symbolic
b. Diagrammatic
c. Both a & b
d. None of these

89. In flow chart symbols the _____operation represents the direction of flow:
a. Connector
b. Looping
c. Arrows
d. Decision making

90. Which register is memory pointer:
a. Program counter
b. Instruction register
c. Stack pointer
d. Source index

91. How many approaches are used to design control unit:
a. 2
b. 3
c. 4
d. 5

92. Which are the following approaches used to design control unit:
a. Hardwired control
b. Microprogrammed control
c. Both a & b
d. None of these

93. Cache memory is located between main memory and_____:
a. CPU
b. Memory
c. Both a & b
d. None of these

94. _____arrow represents the value obtained by evaluating right side expression/variable to the left side variable:

a. Forth
b. Inbetween
c. Back
d. None of these

95. A _____ is written as separate unit, apart from main and called whenever necessary:
a. Subroutine
b. Code
c. Block
d. None of these

96. _____uses the stack to store return address of subroutine:

a. CPU
b. Microprocessor
c. register
d. memory

97. A subroutine is implemented with 2 associated instructions:

a. CALL
b. RETURN
c. Both a & b
d. None of these

98. Call instruction is written in the _____program:

a. Main
b. Procedures
c. Program
d. Memory

99. Return instruction is written in_____ to written to main program:

a. Subroutine
b. Main program
c. Both a & b
d. None of these

100. When subroutine is called contents of program counter is location address of _____instruction following call instruction is stored on _____and program execution is transferred to_____ address:
a. Non executable, pointer and subroutine
b. Executable, Stack and Main program
c. Executable, Queue and Subroutine
d. Executable, Stack and Subroutine

101. A subroutine called by another subroutine is called:
a. Nested
b. For loop
c. Break
d. Continue

102. The extent nesting in subroutine is limited only by:
a. Number of available Stack locations
b. Number of available Addressing locations
c. Number of available CPU locations
d. Number of available Memory locations

103. Which are of the following instructions of hardware subroutines:
a. SCAL
b. SXIT
c. Both a & b
d. None of these

104. Importance in local variable and index registers in subroutine does_____:
a. Alter
b. Not alter
c. Both a & b
d. None of these

105. Markers in subroutine cannot be accepted as limits whereas this markers stands for:

a. Top of stack
b. Bottom of stack
c. Middle of stack
d. All of these

106. Subroutines are placed in identical section to caller so that SCAL and SXIT _____overpass divison limits:
a. Don't
b. Does
c. Cross
d. By

107. _____subroutine declaration come after procedure announcement:
a. Global b. Local
c. Both a & b d. None of these

108. subroutines are invoked by using their_____ in a subroutine call statement and replacing formal parameters with_____ parameters:
a. Identifier and formal
b. Identifier and actual
c. Expression and arguments
d. None of these

109. Parameters can be stacked by _____just as with procedures:

a. Asterisk(*)
b. Arrow
c. Line
d. Pipeline

110. The subroutines are determined by functioning of _____instructions:

a. SCAL and SXIT
b. only SCAL
c. only SXIT
d. none of these

111. Call is_____ subroutine call:

a. Conditional
b. Unconditional
c. Both a & b
d. None of these

112. A flag is a _____that keep track of a changing condition during computer run:

a. Memory
b. Register
c. Controller
d. None of these

113. When a subroutine is _____the parameters are loaded onto the stack and SCAL is executed:

a. Executed
b. Invoked
c. Ended
d. Started

114. Subroutine is called _____:

a. In Same program
b. In external program
c. Both a & b
d. None of these

115. If internal subroutine is called global data is used to pass values defining parameters between _____program and defined _____:

a. Main and subroutine
b. Local and subroutine
c. Global and subroutine
d. Global and main

116. In what type of subroutine actual parameters are passed through the main program to formal parameters in the related subroutine:

a. Internal
b. External
c. Both a & b
d. None of these

117. By defining the _____register as last in first out stack the sequence can handle nested subroutines:
a. S
b. J
c. R
d. T

118. The _____stack can be 4-word memory addressed by 2 bits from an up/down counter known as the stack pointer:
a. FIFO
b. PIPO
c. SISO
d. LIFO

119. getchar :: IO char in this given function what is indicated by IO char:
a. when getchar is invoked it returns a character
b. when getchar is executed it returns a character
c. both a & b
d. none of these

120. If we define putchar function in putchar :: char -> IO ( ) syntax than character input as an argument and returns_____:
a. Useful value
b. Get output
c. Get no output
d. None of these

121. The front panel display provides lights as green LED represent _____ and red LED represent _____for device programmer who writes input/output basic:
a. Busy and Error
b. Error and Busy
c. Busy and Busy
d. Error and Error

122. The input data for processing uses the standard input device which by default is a _____:
a. Mouse
b. Scanner
c. Keyboard
d. Monitor

123. The processed data is sent for output to standard _____device which by default is computer screen:

a. Input
b. Output
c. Both a & b
d. None of these

124. Each instruction is executed by set of micro operations termed as:

a. Micro instructions
b. Mini instructions
c. Both a & b
d. None of these

125. For each micro operation the control unit generates set of_____ signals:

a. Control
b. Address
c. Data
d. None of these

126. Sequence of microinstructions is termed as micro program or_____:

a. Hardware
b. Software
c. Firmware
d. None of these

127. The micro program is an _____written in microcode and stored in firmware which is also referred as_____:
a. Interpreter and control memory
b. Translator and control store
c. Translator and control memory
d. Interpreter and Translator

128. Compared to hardware, firmware is _____to design micro programmed organization:

a. Difficult
b. Easier
c. Both a& b
d. None of these

129. Compared to software, firmware is _____to write:

a. Easier
b. Difficult
c. Mediator
d. Optimum

130. _____program converts machine instructions into control signals:
a. Control memory program
b. Control store program
c. Both a & b
d. Only memory

131. who coined the term micro program in 1951:

a. T.V. Wilkes
b. M.V. Wilkes
c. S.V. Wilkes
d. D.V. Wilkes

132. what is full form of EDSAC:
a. Electronic delay source accumulator calculator
b. Electronic delay storage automatic code
c. Electronic destination source automatic calculator
d. Electronic delay storage automatic calculator

133. Who led to development of read –only magnetic core matrix for use in control unit of small computer at IBM's laboratory:

a. John Fairclough's
b. Johny fairclough
c. Mr. Redcliff
d. M.V. Wilkes

134. From1961-1964 John fairclough's research played an important role to pursue full range of compatible computers as system:

a. System/360
b. System/460
c. System/560
d. System/780

135. Each microinstructions cycle is made of 2 parts:

a. Fetch
b. Execute
c. Code
d. Both a & b

136. One of use of microprogramming to implement _____ of processor in Intel 80x86 and Motorola 680x0 processors whose instruction set are evolved from 360 original:
a. Control structure
b. Without control
c. Control unit
d. Only control

137. The function of these microinstructions is to issue the micro orders to_____:
a. CPU
b. Memory
c. Register
d. Accumulator

138. Micro-orders generate the_____ address of operand and execute instruction and prepare for fetching next instruction from the main memory:
a. Physical
b. Effective
c. Logical
d. all of above

139. Which of the following 2 task are performed to execute an instruction by MCU:
a. Microinstruction execution
b. Microinstruction sequencing
c. Both a & b d. None of these

140. What is the purpose of microinstruction executions:
a. Generate a control signal
b. Generate a control signal to compile
c. Generate a control signal to execute
d. All of these

141. Which microinstruction provide next instruction from control memory:
a. Microinstruction execution
b. Microinstruction Buffer
c. Microinstruction decoder
d. Microinstruction Sequencing

142. Which are the following components of microprogramed units to implement control process:
a. Instruction register
b. Microinstruction address generation
c. Control store microprogram memory
d. Microinstruction Buffer
e. Microinstruction decoder
f. All of these

143. Microcodes are stored as firmware in _____:
a. Memory chips b. Registers
c. accumulators d. none of these

144. A control memory is_____ stored in some area of memory:
a. Control instruction
b. Memory instruction
c. Register instruction
d. None of these

145. A computer having writable control memory is known as_____:
a. Static micro programmable
b. Dynamic micro programmable
c. Both a & b
d. None of these

146. The control memory contains a set of words where each word is:

a. Microinstruction
b. Program
c. Sets
d. All of these

147. During program execution content of main memory undergo changes and, but control memory has_____ microprogram:

a. Static
b. Dynamic
c. Compile time
d. Fixed

148. What happens if computer is started :
a. It executes "CPU" microprogram which is sequence of microinstructions stored in ROM
b. It executes "code" microprogram which is sequence of microinstructions stored in ROM
c. **It executes "boot" microprogram which is sequence of microinstructions stored in ROM**
d. It executes "strap loader" microprogram which is sequence of microinstructions stored in ROM

149. Control memory is part of _____ that has addressable storage registers and used as temporary storage for data:

a. ROM
b. RAM
c. CPU
d. Memory

150. How many modes the address in control memory are divided:

a. 2
b. 3
c. 5
d. 7

151. which of the following is interrupt mode:

a. Task mode
b. Executive mode
c. Both a & b
d. None of these

152. Mode of addresses in control memory are:
a. Executive mode
b. Task mode
c. Both a & b
d. None of these

153. Addresses in control memory is made by____ for each register group:
a. Address select logic
b. Data select logic
c. Control select logic
d. All of these

154. There are how many register groups in control memory:
a. 3
b. 5
c. 6
d. 8

155. What type of circuit is used by control memory to interconnect registers:
a. Data routing circuit
b. Address routing circuit
c. Control routing circuit
d. None of the these

156. Which memory is used to copy instructions or data currently used by CPU:

a. Main memory
b. Secondary memory
c. Cache memory
d. None of these

157. Copy of instruction in cache memory is known as:

a. Execution cache
b. Data cache
c. Instruction cache
d. All of these

158. Copy of data in cache memory is called:
a. Data cache
b. Execution cache
c. Address cache
d. Control cache

159. What are 2 advantages of cache memory:
a. Reduction of average access time for CPU memory
b. Reduction of bandwidth of available memory of CPU
c. Both a & b
d. None of these

160. On what method search in cache memory used by the system:

a. Cache directing
b. Cache mapping
c. Cache controlling
d. Cache invalidation

161. _____process starts when a cpu with cache refers to a memory:

a. Main memory
b. External memory
c. Cache
d. All of these

162. When cache process starts hit and miss rate defines in cache directory:

a. during search reads
b. during search writes
c. during replace writes
d. during finding writes

163. In cache memory hit rate indicates:
a. Data from requested address is not available
b. Data from requested address is available
c. Control from requested address is available
d. Address from requested address is not available

164. In cache memory miss rate indicates:
a. Availability of requested data
b. Availability of requested address
c. Non-Availability of requested data
d. Non-Availability of requested address

165. Which 3 areas are used by cache process:
a. Search, updating, invalidation
b. Write, updating, invalidation
c. Search, read, updating
d. Invalidation, updating, requesting

166. Updating writes to cache data and also to _____:

a. Directories
b. Memory
c. Registers
d. Folders

167. Invalidation writes only to_____ and erases previously residing address in memory:
a. Folders
b. Memory
c. Directory
d. Files

168. _____machine instruction creates branching to some specified location in main memory if result of last ALU operation is Zero or Zero flag is set:
a. Branch on One
b. Branch on Three
c. Branch on Nine
d. Branch on Zero

169. Full form of CAR:
a. Control address register
b. Content address register
c. Condition accumulator resource
d. Code address register

170. Two types of microinstructions are:
a. Branching
b. Non-branching
c. Both a & b
d. None of these

171. Which are 3 ways to determine address of next micro instruction to be executed:
a. Next sequential address
b. Branching
c. Interrupt testing
d. All of these

172. Branching can be_____:
a. Conditional
b. Unconditional
c. Both a & b
d. None of these

173. In which branching condition is tested which is determined by status bit of ALU:
a. Unconditional
b. Conditional
c. Both a & b
d. None of these

174. which branch is achieved by fixing status bit that output of multiplexer is always one:
a. Unconditional
b. Conditional
c. Looping
d. All of these

175. Which register is used to store addresses of control memory from where instruction is fetched:
a. MAR
b. BAR
c. CAR
d. DAR

176. Control ROM is the control memory that holds:

a. Control words
b. Memory words
c. Multiplexers
d. Decoders

177. Opcode is the machine instruction obtained from decoding instruction stored in:

a. Stack pointer
b. Address pointer
c. Instruction register
d. Incrementer

178. Branch logic determines which should be adopted to select the next_____ value among possibilities:
a. CAR
b. GAR
c. HAR
d. TAR

179. _____ generates CAR+1 as possibility of next CAR value:
a. Decrementer
b. Incrementer
c. Postfix
d. Prefix

180. _____used to hold return address for operations of subroutine call branch:
a. TBR
b. HDR
c. SDR
d. SBR

181. Which of following 2 types of computer system considered by micro programmed unit:
a. Micro level computers
b. Machine level computers
c. Both a & b
d. None of these

182. Following are the components of micro programmed control unit:
a. Subroutine register
b. Control address register
c. Memory Of 128 words with 20 bits per words
d. All of these

183. Various machine level components are:
a. Address register b. Program counter
c. Data register d. Accumulator register
e. Memory of 2K,16 bits/word RAM
f. Multiplexers **g. All of these**

184. Data transfers are done using:
a. Multiplexer switching
b. Demultiplexer switching
c. Adder switching
d. Subtractor switching

185. PC can be loaded from_____:
a. BR
b. CR
c. AR
d. TR

186. Which functions are performed by CU:
a. Data exchange b/w CPU and memory or I/O modules
b. External operations
c. Internal operations inside CPU
d. Both a & c

187. Which are internal operations inside CPU:
a. Data transfer b/w registers
b. Instructing ALU to operate data
c. Regulation of other internal operations
d. All of these

188. How many paths taken by movement of data in CU:
a. 3
b. 4
c. 5
d. 2

189. 2 data paths in CU are:
a. Internal data paths
b. External data paths
c. Both a & b
d. None of these

190. _____is the data paths link CPU registers with memory or I/O modules:
a. External data paths
b. Internal data paths
c. Boreal data paths
d. Exchange data paths

191. _____is data paths there is movement of data from one register to another or b/w ALU and a register:
a. External b. Boreal
c. Internal d. Exchange

192. Which is the input of control unit:
a. Master clock signal
b. Instruction register c. Flags
d. Control signals from bus
e. All of these

193. If _____flag is set then control unit issues control signals that causes program counter to be incremented by 1:

a. Zero
b. One
c. Three
d. Eight

194. Which control unit is implemented as combinational circuit in the hardware:
a. Microprogrammed control unit
b. Hardwired control unit
c. Blockprogrammed control unit
d. Macroprogrammed control unit

195. Microprograms are usually stored in:
a. ROM
b. RAM
c. SAM
d. SAN

196. Among them which is the faster control unit:
a. Hardwired
b. Microprogrammed
c. Both a & b
d. None of these

197. For CISC architecture_____ controllers are better:
a. Microprogrammed
b. Hardwired
c. Betterwired
d. None of these

198. Full form of FSM is:
a. Finite state machine
b. Fix state machine
c. Fun source metal
d. All of these

199. Rules of FSM are encoded in:
a. ROM
b. Random logic
c. Programmable logic array
d. All of these

200. In RISC architecture access to registers is made as a block and register file in a particular register can be selected by using:
a. Multiplexer
b. Decoder
c. Subtractor
d. Adder

201. Outputs of instruction/data path in CU are:
a. Reg R/W b. Load/Reg-Reg
c. ALU function select d. Load control
e. Read control f. IR Latch
g. JUMP/Branch/Next PC **h. All of these**

202. One last bit of control output is for control of_____ state:
a. Minor **b. Major**
c. Mixer d. None of these

203. Following are 4 major states for 'load' are:
a. Fetch b. Decode c. Memory
d. Write back **e. All of these**

204. Jump has 3 major states are:
a. Fetch b.Decode c.Complete**d.All of these**

205. _____ state keeps track of position related to execution of an instruction:
a. Major b. Minor c. Both a & b
d. None of these

206. An instruction always starts with state___:

a. 1 b. 2 c. 3 **d. 0**

207. Decoding of an instruction in RISC architecture means decision on working of control unit for:
a. Remainder of instructions
b. Divisor of instructions
c. Dividend of instructions d. None

208. Which control is used during starting of instruction cycle:
a. Write **b. Read** c. R/W
d. None of these

209. _____function select takes op code in IR translating to function of ALU and it may be compact binary code or one line per ALU:
a. ALU b. CPU c.Memory d. Cache

210. _____is dependent on instruction type in CU:
a. Jump b. Branch
c. NextPC **d. All of these**

211. _____dependent on instruction and major state and also comes in starting of data fetch state as well as write back stage in CU:
a. Register read b. Register write
c. Register R/W d. All of these

212. _____dependence over op-code in C:
a. Load register
b. Load Reg/Reg
c. Only Load
d. None of these

213. Full form of PLA in CU:
a. Progrmmable Logic Array
b. Programs Load Array
c. Programmable Logic Accumulator
d. all of these

214. Which are tasks for execution of CU or MCU:
a. Microinstruction execution
b. Microinstruction sequencing
c. Both a & b d. None of these

215. Branching is implemented by depending on output of:
a. CD b. RG c. CC d. CR

216. Who determine under what conditions the branching will occur and when:
a. By combination of CD and BT
b. By combination of CD and BR
c. By combination of CD and CR
d. By combination of TD and BR

217. The character U is used to indicate:
a. Undefined transfers
b. Unfair transfers
c. Unconditional transfers
d. All of these

218. Which field is used to requests for branching:
a. DR b. CR
c. TR **d. BR**

219. which field is used to determine what type of transfer occurs:
a. CR b. SR
c. BR d. MR

220. Source statements consist of 5fields in microinstruction source code are:
a. Lable
b. Micro-ops
c. CD-spec
d. BR-spec
e. Address
f. All of these

Computer System Architecture MCQ 04

1. Which is a type of microprocessor that is designed with limited number of instructions:
a. CPU
b. RISC
c. ALU
d. MUX

2. Which unit is a pipeline system helps in speeding up processing over a non pipeline system:
a. CPU
b. RISC
c. ALU
d. MUX

3. The group of binary bits assigned to perform a specified operation is known as:
a. Stack register
b. Control word
c. Both
d. None

4. How many binary selection inputs in the control word:
a. 1
b. 7
c. 14
d. 28

5. In control word three fields contain how many bits:
a. 1
b. 2
c. 3
d. 4

6. Three fields contains three bits each so one filed has how many bits in control word:
a. 2
b. 4
c. 5
d. 6

7. How is selects the register that receives the information from the output bus:
a. Decoder
b. Encoder
c. MUX
d. All of these

8. A bus organization for seven _____register:
a. ALU
b. RISC
c. CPU
d. MUX

9. How many source register propagate through the multiplexers:

a. 1
b. 2
c. 3
d. 4

10. How many bits of OPR select one of the operations in the ALU:

a. 2
b. 3
c. 4
d. 5

11. five bits of OPR select one of the operation in the ____ in control register:

a. CPU
b. RISC
c. ALU
d. MUX

12. The OPR field has how many bits:

a. 2
b. 3
c. 4
d. 5

13. In stack organization the insertion operation is known as ____:

a. Pop
b. Push
c. Both
d. None

14. In stack organization the deletion operation is known as ____:
a. Pop
b. Push
c. Both
d. None

15. A stack in a digital computer is a part of the_____:

a. ALU
b. CPU
c. Memory unit
d. None of these

16. In stack organization address register is known as the:

a. Memory stack
b. Stack pointer
c. Push operation
d. Pop operation

17. In register stack a stack can be organized by a _____number of register:

a. Infinite number
b. Finite number
c. Both
d. None

18. Which operation are done by increment or decrement the stack pointer:

a. Push
b. Pop
c. Both
d. None

19. In register stack a stack can be a finite number of_____:

a. Control word
b. Memory word
c. Transfer word
d. All of these

20. The stack pointer contains the address of the word that is currently on____:

a. Top of the stack
b. Down of the stack
c. Top and Down both
d. None

21. In register stack items are removed from the stack by using the ____operation:

a. Push
b. Pop
c. Both
d. None

22. Which register holds the item that is to be written into the stack or read out of the stack:

a. SR
b. IR
c. RR
d. DR

23. In register stack the top item is read from the stack into:

a. SR
b. IR
c. RR
d. DR

24. In conversion to reverse polish notation the ____and____ operations are performed at the end:

a. Add and subtract
b. Subtract and multiplication
c. Multiplication and subtract
d. All of these

25. RPN stands for:

a. Reverse polish notation
b. Read polish notation
c. Random polish notation
d. None of these

26. Instruction formats contains the memory address of the_____:

a. Memory data
b. Main memory
c. CPU
d. ALU

27. In instruction formats instruction is represent by a_____ of bits:

a. Sequence
b. Parallel
c. Both
d. None

28. In instruction formats the information required by the _____ for execution:

a. ALU
b. CPU
c. RISC
d. DATA

29. The operation is specified by a binary code known as the_____:

a. Operand code
b. Opcode
c. Source code
d. All of these

30. Which are contains one or more register that may be referenced by machine instruction:

a. Input
b. Output
c. CPU
d. ALU

31. Memory –mapped ___is used this is just another memory address:

a. Input
b. Output
c. Both
d. None

32. Which operation use one operand or unary operations:

a. Arithmetic
b. Logical
c. Both
d. None

33. 3-Address format can be represented as :
a. dst <-[src1][src2]
b. dst ->[src1][src2]
c. dst <->[src1][src2]
d. All of these

34. 2- Address format can be represented as:
a. dst ->[dst]*[src]
b. dst<-[dst]*[src]
c. dst<->[dst]*[src]
d. All of these

35. In 1-address format how many address is used both as source as well as destination:

a. 1
b. 2
c. 3
d. 4

36. The stack pointer is maintained in a____:

a. Data
b. Register
c. Address
d. None of these

37. ___ mode of addressing is a form of implied addressing:
a. Stack
b. Array
c. Queue
d. Binary

38. Stack uses RPN to solve _____expression:

a. Logical
b. Arithmetic
c. Both
d. None

39. In the RPN scheme the numbers and operators are listed_____:

a. One after another
b. One before another
c. Another after one
d. Another before one

40. In addressing modes instruction has primarily how many components:
a. 1
b. 2
c. 3
d. 4

41. EA stands for:

a. Effective add
b. Effective absolute
c. Effective address
d. End address

42. In which addressing the operand is actually present in instruction:

a. Immediate addressing
b. Direct addressing
c. Register addressing
d. None of these

43. In which addressing the simplest addressing mode where an operand is fetched from memory is_____:

a. Immediate addressing
b. Direct addressing
c. Register addressing
d. None of these

44. which addressing is a way of direct addressing:

a. Immediate addressing
b. Direct addressing
c. Register addressing
d. None of these

45. In which mode the main memory location holds the EA of the operand:

a. Immediate addressing
b. Direct addressing
c. Register addressing
d. Indirect addressing

46. Which addressing is an extremely influential way of addressing:

a. Displacement addressing
b. Immediate addressing
c. Direct addressing
d. Register addressing

47. In the base –register addressing the register reference may be _____:

a. Implicit
b. Explicit
c. Both
d. None

48. In post –indexing the indexing is performed_____

a. Before the indirection
b. After the indirection
c. Same time indirection
d. All of these

49. In post-indexing the contents of the address field are used to access a memory location containing a___ address:

a. Immediate addressing
b. Direct addressing
c. Register addressing
d. None of these

50. In pre –indexing the indexing is performed_____

a. Before the indirection
b. After the indirection
c. Same time indirection
d. All of these

51. The final addressing mode that we consider is_____:

a. Immediate addressing
b. Direct addressing
c. Register addressing
d. Stack addressing

52. In data transfer manipulation designing as instruction set for a system is a complex_____ :

a. Art
b. System
c. Computer
d. None of these

53. Which addressing is an extremely influential way of addressing:

a. Immediate addressing
b. Direct addressing
c. Register addressing
d. Displacement addressing

54. Which addressing offset can be the content of PC and also can be negative:
a. Relative addressing
b. Immediate addressing
c. Direct addressing
d. Register addressing

55. The length of instruction set depends on:
a. Data size
b. Memory size
c. Both
d. None

56. In length instruction some programs wants a complex instruction set containing more instruction, more addressing modes and greater address rang, as in case of_____:

a. RISC
b. CISC
c. Both
d. None

57. In length instruction other programs on the other hand, want a small and fixed-size instruction set that contains only a limited number of opcodes, as in case of_____:

a. RISC
b. CISC
c. Both
d. None

58. The instruction set can have variable-length instruction format primarily due to:
a. Varying number of operands
b. Varying length of opcodes in some CPU
c. Both
d. None

59. An instruction code must specify the address of the____:

a. Opecode
b. Operand
c. Both
d. None

60. A simple ____ differs widely from a Turing machine:

a. CISC
b. RISC
c. CPU
d. ALU

61. How many types of basically Data manipulation:

a. 1
b. 2
c. 3
d. 4

62. Which is data manipulation types are:
a. Arithmetic instruction
b. Shift instruction
c. Logical and bit manipulation instructions
d. All of these

63. Arithmetic instruction are used to perform operation on:
a. Numerical data
b. Non-numerical data
c. Both
d. None

64. How many basic arithmetic operation:
a. 1
b. 2
c. 3
d. 4

65. which are arithmetic operation are:

a. Addition
b. Subtraction
c. Multiplication
d. Division
e. All of these
f. None of these

66. In which instruction are used to perform Boolean operation on non-numerical data:
a. Logical and bit manipulation
b. Shift manipulation
c. Circular manipulation
d. None of these

67. Which operation is used to shift the content of an operand to one or more bits to provide necessary variation:
a. Logical and bit manipulation
b. Shift manipulation
c. Circular manipulation
d. None of these

68. _____is just like a circular array:
a. Data
b. Register
c. ALU
d. CPU

69. Which control refers to the track of the address of instructions:

a. Data control
b. Register control
c. Program control
d. None of these

70. In program control the instruction is set for the statement in a:
a. Parallel
b. Sequence
c. Both
d. None

71. How many types of unconditional jumps used in program control are follows:

a. 1
b. 2
c. 3
d. 4

72. Which are unconditional jumps used in program control are follows:

a. Short jump
b. Near jump
c. Far jump
d. All of these

73. Which instruction is used in program control and used to decrement CX and conditional jump:

a. Loop
b. Shift manipulation
c. Circular manipulation
d. None of these

74. Which is always considered as short jumps:

a. Conditional jump
b. Short jump
c. Near jump
d. Far jump

75. Who change the address in the program counter and cause the flow of control to be altered:

a. Shift manipulation
b. Circular manipulation
c. Program control instruction
d. All of these

76. Which is the common program control instructions are:

a. Branch
b. Jump
c. Call a subroutine
d. Return
e. All of these
f. None of these

77. Which is a type of microprocessor that is designed with limited number of instructions:
a. CISC
b. RISC
c. Both
d. None

78. SMP Stands for:
a. System multiprocessor
b. Symmetric multiprocessor
c. Both
d. None

79. UMA stands for:
a. Uniform memory access
b. Unit memory access
c. Both
d. None

80. NUMA stands for:
a. Number Uniform memory access
b. Not Uniform memory access
c. Non Uniform memory access
d. All of these

81. SIMD stands for:
a. System instruction multiple data
b. Single instruction multiple data
c. Symmetric instruction multiple data
d. Scale instruction multiple data

82. MIMD stands for:
a. Multiple input multiple data
b. Memory input multiple data
c. Multiple instruction multiple data
d. Memory instruction multiple data

83. HLL stands for:
a. High level languages
b. High level line
c. High level logic
d. High level limit

84. Which is a method of decomposing a sequential process into sub operations:
a. Pipeline b. CISC
c. RISC d. Database

85. How many types of array processor:
a. 1 **b. 2**
c. 3 d. 4

86. Which are the types of array processor:
a. Attached array processor
b. SIMD array processor
c. Both d. None

87. Which are the application of vector processing:
a. Weather forecasting
b. Artificial intelligence
c. Experts system d. Images processing
e. Seismology f. Gene mapping
g. Aerodynamics **h. All of these**
i. None of these

88. Which types of jump keeps a 2_byte instruction that holds the range from- 128to127 bytes in the memory location:
a. Far jump b. Near jump
c. Short jump d. All of these

89. Which types of register holds a single vector containing at least two read ports and one write ports:
a. Data system
b. Data base
c. Memory
d. Vector register

90. Parallel computing means doing several takes simultaneously thus improving the performance of the_____:
a. Data system
b. Computer system
c. Memory
d. Vector register

91. Which is used to speed-up the processing:

a. Pipeline
b. Vector processing
c. Both
d. None

92. Which processor is a peripheral device attached to a computer so that the performance of a computer can be improved for numerical computations:

a. Attached array processor
b. SIMD array processor
c. Both
d. None

93. Which processor has a single instruction multiple data stream organization that manipulates the common instruction by means of multiple functional units:
a. Attached array processor
b. SIMD array processor
c. Both
d. None

94. Which carry is similar to rotate without carry operations:

a. Rotate carry
b. Rotate through carry
c. Both
d. None

95. In the case of a left arithmetic shift , zeros are Shifted to the _____:

a. Left
b. Right
c. Up
d. Down

96. In the case of a right arithmetic shift the sign bit values are shifted to the_____:

a. Left
b. Right
c. Up
d. Down

Computer System Architecture MCQ 05

1. A number system that uses only two digits, 0 and 1 is called the_____:
a. Octal number system
b. Binary number system
c. Decimal number system
d. Hexadecimal number system

2. In which computers, the binary number are represented by a set of binary storage device such as flip flop:
a. Microcomputer
b. Personal computer
c. Digital computer
d. All of these

3. A binary number can be converted into _____:
a. Binary number
b. Octal number
c. Decimal number
d. Hexadecimal number

4. Which system is used to refer amount of things:
a. Number system
b. Number words
c. Number symbols
d. All of these

5. _____are made with some part of body, usually the hands:

a. Number words
b. Number symbols
c. Number gestures
d. All of these

6. _____are marked or written down:
a. Number system
b. Number words
c. Number symbols
d. Number gestures

7. A number symbol is called a _____:

a. Arabic numerals
b. Numerals
c. Both
d. None of these

8. 0,1,2 ,3 ,4,5,6 ,7,8 and 9 numerals are called:
a. Arabic numerals
b. String numerals
c. Digit numerals
d. None of these

9. How many system of arithmetic, which are often used in digital system:

a. 5
b. 6
c. 3
d. 4

10. Which are the system of arithmetic, which are often used in digital system:
a. Binary digit
b. Decimal digit
c. Hexadecimal digit
d. Octal digit
e. All of these

11. In any system, there is an ordered set of symbols also known as_____:
a. Digital
b. Digit
c. Both
d. None of these

12. Which is general has two parts in number system:
a. Integer
b. Fraction
c. Both
d. None of these

13. MSD stand for:

a. Most significant digit
b. Many significant digit
c. Both a and b
d. None of these

14. LSD stand for:
a. Less significant digit
b. Least significant digit
c. Loss significant digit
d. None of these

15. The _____ and _____ of a number is defined as the number of different digits which can occur in eachposition in the system:
a. Base
b. Radix
c. Both
d. None of these

16. Which system has a base or radix of 10:
a. Binary digit
b. Hexadecimal digit
c. Decimal digit
d. Octal digit

17. Each of the ten decimal digits_____:
a. 1 through 10
b. 0 through 9
c. 2 through 11
d. All of these

18. The binary number system is also called a _____:
a. Base one system
b. Base two system
c. Base system
d. Binary system

19. The two symbols 0 and 1 are known as:
a. Bytes
b. Bits
c. Digit
d. All of these

20. In which counting, single digit are used for none and one:
a. Decimal counting
b. Octal counting
c. Hexadecimal counting
d. Binary counting

21. In which numeral every position has a value 2 times the value f the position to its right:
a. Decimal
b. Octal
c. Hexadecimal
d. Binary

22. A binary number with 4 bits is called a_____:
a. Bit
b. Bytes
c. Nibble
d. None of these

23. A binary number with 8 bits is called as a_____:
a. Bytes
b. Bits
c. Nibble
d. All of these

24. In which digit the value increases in power of two starting with 0 to left of the binary point and decreases to the right of the binary point starting with power -1:
a. Hexadecimal
b. Decimal
c. Binary
d. Octal

25. Which system is used in digital computers because all electrical and electronic circuits can be made to respond to the states concept:

a. Hexadecimal number
b. Binary number
c. Octal number
d. Decimal number

26. Which addition is performed in the same manner as decimal addition:

a. Binary
b. Decimal
c. Both
d. None of these

27. _____in all digital systems actually performs addition that can handle only two number at a time:

a. Register
b. circuit
c. digital
d. All of these

28. Which machine can perform addition operation in less than 1 ms:

a. Digital machine
b. Electronic machine
c. Both
d. None of these

29. _____is the inverse operation of addition:

a. Addition
b. Multiply
c. Subtraction
d. Divide

30. _____of a number from another can be accomplished by adding the complement of the subtrahend to the minuend:

a. Subtraction
b. Multiply
c. Divide
d. All of these

31. Complement the subtrahend by converting all _____and all _____:

a. 1's to 0's
b. 0's to 1's
c. Both
d. None of these

32. Each device represent :
a. 1 bit
b. 2 bit
c. 3 bit
d. 4 bit

33. A 0 in the sign bit represents a _____ and a 1 in the sign bit represents a _____:
a. Positive number
b. Negative number
c. Both
d. None of these

34. How many main sign number binary codes are used:
a. 4 b. 5 **c. 3** d. 6

35. Which are the types of binary codes number:
a. Sign magnitude
b. 1's complement code
c. 2's complement code
d. All of these

36. How many types of addition in the 2's complement system:
a. 3
b. 4
c. 5
d. 6

37. Which are the types of addition in the 2's complement system:
a. Both number positive
b. A Positive number and a smaller negative number
c. A negative number and a smaller positive number
d. Both number negative
e. All of these

38. How many important ideas to notice about these odometer readings:
a. 1 **b. 2** c. 3 d. 4

39. Which are the types of important ideas to notice about these odometer readings:
a. The MSB is the sign bit :0 for a +sign and 1 for a – sign
b. The negative number represent the 2's complement of the positive number
c. Both d. All of these

40. Which is an algorithm or techniques used to multiply two numbers:
a. Addition algorithm
b. Subtraction algorithm
c. Multiplication algorithm
d. All of these

41. Which algorithm are used depending on the size of the numbers:
a. Simple algorithm
b. Specific algorithm
c. Both
d. None of these

42. Which algorithm is named after Volker Strassen:
a. Strassen algorithm
b. Matrix algorithm
c. Both
d. None of these

43. Strassen algorithm was published in _____:
a. 1967
b. 1969
c. 1987
d. 1980

44. Which algorithm is used for matrix multiplication:
a. Simple algorithm
b. Specific algorithm
c. Strassen algorithm
d. Addition algorithm

45. Which algorithm is a divided and conquer algorithm that is asymptotically faster:
a. Simple algorithm
b. Specific algorithm
c. Strassen algorithm
d. Addition algorithm

46. Which method required 8 multiplication and 4 addition:
a. Multiplication
b. Usual multiplication
c. Both d. None of these

47. Which algorithm is a multiplication algorithm which multiplies two signed binary numbers in 2's complement notation:
a. Usual multiplication
b. Booth's multiplication
c. Both d. None of these

4. Which algorithm includes repeated addition of two predetermined values A and S to a product P and then performs a rightward arithmetic shift on P:
a. Booth's algorithm
b. Usual algorithm
c. Multiplication algorithm
d. None of these

49. Which algorithm in mathematics expresses the outcome of the process of division of integers by another:
a. Addition algorithm
b. Multiplication algorithm
c. Division algorithm
d. None of these

50. Which algorithm is used to find GCD of two integers:
a. Multiplication algorithm
b. Division algorithm
c. Addition algorithm
d. Simple algorithm

51. Which algorithm is used as a general variant of a theorems, in the domain of integral numbers:
a. Multiplication algorithm
b. Division algorithm
c. Addition algorithm
d. Simple algorithm

52. How many main approaches to algorithm for division:
a. 2 b. 3
c. 4 d. 5

53. How many algorithm based on add/subtract and shift category:
a. 2 b. 4
c. 3 d. 6

54. Which are the algorithm based on add/subtract and shift category:
a. Restoring division
b. Non-restoring division
c. SRT division
d. All of these

55. Several methods for converting a _____:
a. Decimal number to a binary number
b. Binary number to a decimal number
c. Octal number to a decimal number
d. Hexadecimal number to a binary number

56. A popular method knows as double-dabble method also knows as _____:
a. Divided-by-one method
b. Divided-by-two method
c. Both d. None of these

57. Which method is used to convert a large decimal number into its binary equivalent:
a. Double dabble method
b. Divided-by-two-method
c. Both
d. None of these

58. In this method, the decimal number is _____:
a. Repeatedly divided by 4
b. Repeatedly divided by 2
c. Repeatedly divided by 1
d. None of these

59. The conversion of decimal fraction to binary fraction may be accomplished by using _____:
a. Several techniques
b. Simple techniques
c. Both d. None of these

60. Which system was used extensively by early mini computers:
a. Decimal number **b. Octal number**
c. Hexadecimal number d. Binary number

61. 3 bit binary numbers can be represented by _____:
a. Binary number b. Decimal number
c. Hexadecimal number
d. Octal number

62. A number system that uses eight digits,0,1,2,3,4,5,6, and 7 is called an _____:
a. Binary number system
b. Decimal number system
c. Octal number system
d. None of these

63. Which system each digit has a weight corresponding to its position:
a. Hexadecimal number system
b. Binary number system
c. Decimal number system
d. Octal number system

64. Which odometer is a hypothetical device similar to the odometer of a car:
a. Binary b. Decimal
c. Hexadecimal **d. Octal**

65. An _____can be easily converted to its decimal equivalent by multiplying each octal digit by positional weight:
a. Binary number **b. Octal number**
c. Hexadecimal number
d. Decimal number

66. The simple procedure is to use _____ :
a. Binary-triplet method
b. Decimal-triplet method
c. Octal-triplet method
d. All of these

67. Which system groups number by sixteen and power of sixteen:
a. Binary **b. Hexadecimal**
c. Octal d. None of these

68. Which number are used extensively in microprocessor work:
a. Octal **b. Hexadecimal**
c. Both d. None of these

69. Which number is formed from a binary number by grouping bits in groups of 4-bit each starting at the binary point:
a. Binary b. Octal
c. Decimal **d. Hexadecimal**

70. Which number system has a base of 16 :
a. Binary number system
b. Octal number system
c. Decimal number system
d. Hexadecimal number system

71. Counting in hex, each digit can be increment from_____:
a. 0 to F b. 0 to G
c. 0 to H d. 0 to J

72. Which number can be converted into binary numbers by converted each hexadecimal digit to 4 bits binary equivalent using the code:
a. Binary number b. Decimal number
c. Octal number **d. Hexadecimal number**

73. One way to convert from decimal to hexadecimal is the _____:
a. Double dabble method
b. Hex dabble method
c. Binary dabble method
d. All of these

74. Binary numbers can also be expressed in this same notation by _____representation:
a. Floating point
b. Binary point
c. Decimal point
d. All of these

75. How many parts of floating point representation of a number consists:
a. 4 **b. 2** c. 3 d. 5

76. The first part of floating point represents a signed fixed point number called:
a. Exponent
b. Digit
c. Number
d. Mantissa

77. The second part of floating point designates the position of the decimal point and is called:
a. Mantissa b. Binomial
c. Octal **d. Exponent**

78. The fixed point mantissa may be _____or_____:
a. Fraction b. Integer
c. Both d. None of these

79. The number of bit required to express_____ and _____ are determined by the accuracy desired from the computing system :
a. Exponent b. Mantissa
c. Both d. None f these

80. Which part is not physically indicated in the register:
a. Binary **b. Decimal**
c. Octal d. None of these

81. The exponent contains the decimal number :
a. +05 b. +03
c. +04 d. +07

82. The first or the integer part is known as_____:
a. Exponent b. Integer
c. Binomial **d. None of these**

83. How many bits of mantissa :
a. 4 b. 8
c. 10 d. 16

84. How many bit of exponent:
a. 4 **b. 6**
c. 8 d. 10

85. Which number is said to be normalized if the more significant position of the mantissa contains a non zero digit:
a. Binary point number
b. Mantissa point number
c. Floating point number
d. None of these

86. Which operation with floating point numbers are more complicated then arithmetic operation with fixed point number :
a. Logical operation
b. Arithmetic operation
c. Both
d. None of these

Computer System Architecture MCQ 06

1. Which is an important data transfer technique :
a. CPU
b. **DMA**
c. CAD
d. None of these

2. Which device can be thought of as transducers which can sense physical effects and convert them into machine-tractable data:

a. Storage devices
b. **Peripheral devices**
c. Both
d. None

3. Which devices are usually designed on the complex electromechanical principle:

a. Storage devices
b. Peripheral devices
c. **Input devices**
d. All of these

4. Which disk is one of the important I/O devices and its most commonly used as permanent storage devices in any processor:

a. **Hard disk**
b. Optical disk
c. Magneto disk
d. Magneto Optical disk

5. In storage devices PC have hard disk having capacities in the range of _____:

a. 12GB to 15GB
b. 15GB to 20GB
c. **20GB to 80GB**
d. 80GB to 85GB

6. Which disk is a 3.5-inch diskette with a capacity of 1.44MB:

a. Soft disk
b. Floppy disk
c. **Both**
d. None

7. Which has a large storage capacity of 2 to8GB:

a. **Magnetic tape**
b. Magnetic disk
c. Soft disk
d. Floppy disk

8. Which disk read the data by reflecting pulses of laser beams on the surface:

a. Magnetic disk
b. Soft disk
c. Floppy disk
d. **Optical disk**

9. Data access time of optical disk varies from 200 to 350minutes with transfer rate of _____:
a. 130KB/s to 400KB/s
b. 130KB/s to 500KB/s
c. 150KB/s to 600KB/s
d. **150KB/s to 800KB/s**

10. NAND type flash memory data storage devices integrated with a _____ interface:
a. ATM
b. LAN
c. **USB**
d. DBMS

11. Which disk is based on the same principle as the optical disk:
a. Optical disk
b. Magnetic disk
c. **Magneto-optical disk**
d. All of these

12. WAN stands for:
a. **Wide area network**
b. Word area network
c. World area network
d. Window area network

13. The human-interactive I/O devices can be further categorized as____:
a. Direct
b. Indirect
c. **Both**
d. None

14. I/O devices are categorized in 2 parts are:
a. Character devices
b. Block devices
c. Numeral devices
d. **Both a & b**

15. UART stands for:
a. Universal asynchronization receiver/transmitter
b. **Universal asynchronous receiver/transmitter**
c. United asynchronous receiver/transmitter
d. Universal automatic receiver/transmitter

16. Which are following pointing devices:
a. Light pen
b. Joystick
c. Mouse
d. **All of these**

17. Full form of LED:
a. **Light emitting diode**
b. Light encounter destination
c. Live emitting diode
d. None of these

18. In_____ mouse we use pair of LED:
a. **Optical**
b. Digital
c. Analog
d. All of these

19. _____is device that is designed for gaming purposes and based on principle of electricity:
a. Joy
b. Stick
c. **Joystick**
d. None of these

20. Joystick uses shaft potentiometers for:
a. **X-Y DIRECTION**
b. Only X direction
c. Only Y direction
d. All of these

21. Full form of ADC:
a. **Analog to digital converter**
b. Digital to analog converter
c. Accumulator digital converter
d. All of these

22. A system that enables computer to recognize human voice called:
a. Voice system
b. **Voice input system**
c. Input system
d. None of these

23. 2 commonly used voice input systems are:
a. Micro
b. Microphone
c. Voice recognition software
d. **Both b & c**

24. Optical scanner devices are:
a. MICR
b. OMR
c. OCR
d. **All of these**

25. MICR stands for:
a. **Magnetic ink character recognition**
b. Magnetic initiate character recognition
c. Both a & b
d. None of these

26. _____technique is used in evaluating objective answer sheets:

a. **Optical Mark Reader**
b. Optical Marker Reader
c. Optical Marker Reading
d. All of these

27. _____technique help in banking sector:

a. OCR
b. OMR
c. **MICR**
d. None of these

28. _____camera records image, converts it into digital format via ADC and stores it on a frame buffer:

a. **Video**
b. Without video
c. Audio
d. None of these

29. Sensors are_____ type of devices:

a. Interactive
b. **Non-interactive**
c. Interaction
d. Intermediate

30. Output devices commonly referred as:

a. **Terminals**
b. Host
c. Receivers
d. Senders

31. Terminals classified in to 2 types are:

a. Hard copy
b. Soft copy
c. **Both a & b**
d. None of these

32. VDU stands for:

a. Video display unit
b. **Visual display unit**
c. Visual data unit
d. None of these

33. A monitor consists of :
a. ARU
b. BRT
c. **CRT**
d. ARU

34. LCD stands for:
a. **Liquid crystal display**
b. Liquid catalog display
c. Liquid crystal data
d. Liquid code display

35. The size of monitor ranges from:

a. 12-12 inch
b. **12-21 inch**
c. 21-12 inch
d. 21-11 inch

36. Range of color depends on:
a. Number of bits code lines with each pixel
b. **Number of bits associated with each pixel**
c. Number of instructions associated with each pixel
d. Number of code associated with each pixel

37. Which parameter defines number of times electron beam scans screen in a second:
a. **Refresh rate**
b. Data transfer rate
c. Pitch rate
d. All of these

38. Refresh rate refresh screen up to:
a. **30 Hz per frame**
b. 33 Hz per frame
c. 44 Hz per frame
d. 20 Hz per frame

39 Printer speed is _____pages per minute:
a. 13
b. **12**
c. 11
d. 10

40. Printer is a:
a. **Hardcopy**
b. Softcopy
c. Both a & b
d. None of these

41. Laser printer is type of:
a. Impact printer
b. **Non-impact printer**
c. Both a & b
d. None of these

42. _____printer print 120 to 200 characters per second:
a. **Dot-matrix**
b. Laser
c. Line
d. None of these

43. In_____ printing, each character is printed on the paper by striking a pin or hammer against an inked ribbon:

a. Non-impact printing
b. **Impact printing**
c. Both a & b
d. None of these

44. Dot matrix printer is 2 types is:

a. Daisy wheels
b. Matrix printer
c. High quality matrix printer
d. **Both a & c**

45. In daisy wheel printer can print 40 character/second and bold characters are achieved by overprinting the text:

a. Four times
b. Double
c. **Once**
d. Thrice

46. _____printers spray tiny droplets of coloured inks on the paper and pattern depends on how nozzle sprays the ink:

a. **Inkjet printer**
b. Laser printer
c. Daisy wheel
d. Dot matrix printer

47. Laser printer is a type of :

a. Impact printing
b. **Non-impact printing**
c. Both a & b
d. None of these

48. _____are used for printing big charts, drawings, maps and 3 dimensional illustrations specially for architectural and designing purposes:
a. Printers
b. **Plotters**
c. Speakers
d. Mouse

49. DAC stands for:
a. **Digital to analog converter**
b. Analog to digital converter
c. Only digital converter
d. Only analog converter

50. In text to speech, speech is synthesized using lookup table of_____ and these clubbed together to form_____:

a. **Phonemes, Words**
b. Phonemes, Sentences
c. Character, Phonemes
d. Word, Character

51. _____interface is an entity that controls data transfer from external device, main memory and or CPU registers:

a. **I/O interface**
b. CPU interface
c. Input interface
d. Output interface

52. The operating mode of I/O devices is_____ for different device:

a. Same
b. **Different**
c. Optimum
d. Medium

53. To resolve problems of I/O devices there is a special hardware component between CPU and_____ to supervise and synchronize all input output transfers:

a. Software
b. Hardware
c. **Peripheral**
d. None of these

54. I/O modules are designed with aims to:
a. Achieve device independence
b. Handle errors
c. Speed up transfer of data
d. Handle deadlocks
e. Enable multi-user systems to use dedicated device
f. **All of these**

55. IDE is a_____ controller:

a. **Disk**
b. Floppy
c. Hard
d. None of these

56. In devices, controller is used for_____:
a **Buffering the data**
b. Manipulate the data
c. Calculate the data
d. Input the data

57. By which signal flow of traffic between internal and external devices is done:
a. Only control signal
b. Only timing signal
c. **Control and timing signal**
d. None of these

58. In devices 2 status reporting signals are:

a. BUSY
b. READY
c. **Both a & b**
d. None of these

59. I/O module must recognize a_____ address for each peripheral it controls:

a. Long
b. Same
c. **Unique**
d. Bigger

60. Each interaction b/w CPU and I/O module involves:

a. **Bus arbitration**
b. Bus revolution
c. Data bus
d. Control signals

61. Which are 4 types of commands received by an interface:
a. **Control, status, data output, data input**
b. Only data input
c. Control, flag, data output, address arbitration
d. Data input, data output, status bit, decoder

62. Two ways in which computer buses can communicate with memory in case of I/O devices by using:
a. Separate buses for memory and I/O device
b. Common bus for memory and I/O device
c. **both a & b**
d. none of these

63. There are 2 ways in which addressing can be done in memory and I/O device:
a. Isolated I/O
b. Memory-mapped I/O
c. **Both a & b**
d. None of these

64. Advantages of isolated I/O are:
a. Commonly usable
b. Small number of I/O instructions
c. **Both a & b**
d. None of these

65. In _____ addressing technique separate address space is used for both memory and I/O device:
a. Memory-mapped I/O
b. **Isolated I/O**
c. Both a & b
d. None of these

66. _____is a single address space for storing both memory and I/O devices:
a. **Memory-mapped I/O**
b. Isolated I/O
c. Separate I/O
d. Optimum I/O

67. Following are the disadvantages of memory-mapped I/O are:
a. Valuable memory address space used up
b. I/O module register treated as memory addresses
c. Same machine intersection used to access both memory and I/O device
d. **All of these**

68. Who determine the address of I/O interface:
a. Register select
b. Chip select
c. **Both a & b**
d. None of these

69. 2 control lines in I/O interface is:
a. **RD, WR**
b. RD,DATA
c. WR, DATA
d. RD, MEMORY

70. In I/O interface RS1 and RS0 are used for selecting:
a. Memory
b. **Register**
c. CPU
d. Buffer

71. If CPU and I/O interface share a common bus than transfer of data b/w 2 units is said to be:
a. **Synchronous**
b. Asynchronous
c. Clock dependent
d. Decoder independent

72. All the operations in a digital system are synchronized by a clock that is generated by:
a. Clock
b. Pulse
c. **Pulse generator**
d. Bus

73. Asynchronous means:
a. Not in step with the elapse of address
b. Not in step with the elapse of control
c. Not in step with the elapse of data
d. **Not in step with the elapse of time**

74. _____is a single control line that informs destination unit that a valid is available on the bus:
a. **Strobe**
b. Handshaking
c. Synchronous
d. Asynchronous

75. What is disadvantage of strobe scheme:
a. No surety that destination received data before source removes it
b. Destination unit transfer without knowing whether source placed data on data bus
c. Can't said
d. **Both a & b**

76. In_____ technique has 1 or more control signal for acknowledgement that is used for intimation:
a. **Handshaking**
b. Strobe
c. Both a & b
d. None of these

77. The keyboard has a_____ asynchronous transfer mode:
a. Parallel
b. **Serial**
c. Optimum
d. None

78. In _____transfer each bit is sent one after the another in a sequence of event and requires just one line:
a. **Serial** b. Parallel
c. Both a & b d. None of these

79. Modes of transfer b/w computer and I/O device are:
a. Programmed I/O
b. Interrupt-initiated I/O
c. DMA
d. Dedicated processor such as IOP and DCP
e. **All of these**

80. _____operations are the results of I/O operations that are written in the computer program:
a. **Programmed I/O**
b. DMA
c. Handshaking
d. Strobe

81. _____is a dedicated processor that combines interface unit and DMA as one unit:
a. **Input-Output Processor**
b. Only input processor
c. Only output processor
d. None of these

82. _____is a special purpose dedicated processor that is designed specially designed for data transfer in network:
a. Data Processor
b. **Data Communication Processor**
c. DMA Processor
d. Interrupt Processor

83. _____processor has to check continuously till device becomes ready for transferring the data:
a. **Interrupt-initiated I/O**
b. DMA
c. IOP
d. DCP

84. Interrupt-driven I/O data transfer technique is based on_____ concept:
a. **On demand processing**
b. Off demand processing
c. Both a & b
d. None of these

85. Which technique helps processor to run a program concurrently with I/O operations:
a. **Interrupt driven I/O**
b. DMA
c. IOP
d. DCP

86. 3 types of exceptions are:
a. Interrupts
b. Traps
c. System calls
d. **All of these**

87. Which exception is also called software interrupt:
a. Interrupt
b. **System calls**
c. Traps
d. All of these

88. User programs interact with I/O devices through:

a. **Operating system**
b. Hardware
c. Cpu
d. Microprocessor

89. Which table handle store address of interrupt handling subroutine:

a. **Interrupt vector table**
b. Vector table
c. Symbol link table
d. None of these

90. Which technique is used that identifies the highest priority resource by means of software:

a. Daisy chaining
b. **Polling**
c. Priority
d. Chaining

91. _____interrupt establishes a priority over the various sources to determine which request should be entertained first:

a. **Priority interrupt**
b. Polling
c. Daisy chaining
d. None of these

92. _____method is used to establish priority by serially connecting all devices that request an interrupt:

a. Polling
b. **Daisy chaining**
c. Priority
d. None of these

93. In daisy chaining device 0 will pass signal only if it has:

a. Interrupt request
b. **No interrupt request**
c. Both a & b
d. None of these

94. VAD stands for:

a. **Vector address**
b. Symbol address
c. Link address
d. None of these

95. _____interrupt method uses a register whose bits are set separately by interrupt signal for each device:
a. **Parallel priority interrupt**
b. Serial priority interrupt
c. Both a & b
d. None of these
96. _____register is used whose purpose is to control status of each interrupt request in parallel priority interrupt:

a. Mass
b. Mark
c. Make
d. **Mask**

97. The ANDed output of bits of interrupt register and mask register are set as input of:

a. Priority decoder
b. **Priority encoder**
c. Priority decoder
d. Multiplexer

98. Which 2 output bits of priority encoder are the part of vector address for each interrupt source in parallel priority interrupt:

a. **A0 and A1**
b. A0 and A2
c. A0 and A3
d. A1 and A2
99. What is the purpose

100. of A0 and A1 output bits of priority encoder in parallel priority:
a. Tell data bus which device is to entertained and stored in VAD
b. **Tell subroutine which device is to entertained and stored in VAD**
c. Tell subroutine which device is to entertained and stored in SAD
d. Tell program which device is to entertained and stored in VAD
101. When CPU invokes a subroutine it performs following functions:
a. Pushes updated PC content(return address) on stack
b. Loads PC with starting address of subroutine
c. Loads PC with starting address of ALU
d. **Both a & b**
102. DMAC stands for:
a. **Direct memory access controller**
b. Direct memory accumulator controller
c. Direct memory access content
d. Direct main access controller
103. IOP stands for:
a. **Input output processor**
104. DCP stands for:
a. **Data communication processor**
105. Which may be classified as a processor with the direct memory access capability that communicates with I/O devices:

a. DCP
b. **IOP**
c. Both
d. None

106. The processor that communicates with remote terminals like telephone or any other serial communication media in serial fashion is called _____:

a. **DCP**
b. IOP
c. Both
d. None

107. Instruction that are used for reading from memory by an IOP called _____:

a. **Commands**
b. Block diagram
c. Interrupt
d. None of these

108. Data communication with a remote device a special data communication is used_____:

a. Multiprocessor
b. **Serial communication**
c. DCP
d. IOP

109. CRC stands for:
a. **Cyclic redundancy check**
110. Which is used for synchronous data, PID is process ID, followed by message, CRC code and EOP indicating end of block:

a. DCP
b. CRC
c. IOP
d. **SYNC**

111. Which is commonly used in high –speed devices to realize full efficiency of communication link:
a. Transmission
b. **Synchronous communication**
c. Multiprocessor
d. All of these

112. Multiprocessor use _____ than two CPUs assembled in single system unit:
a. One or More
b. **Two or More**
c. One or One
d. Two or Two

113. Which refers the execution of various software process concurrently:
a. **Multiprocessor**
b. Serial communication
c. DCP
d. IOP

114. Which is used for this and known as high speed buffer exist with almost each process?

a. Primary
b. RAM
c. **Cache**
d. None of these

115. Data and instructions are accessed from local memory and global memory that is used by_____:
a. **Internetworking facilities**
b. Interconnection facilities
c. Both a & b
d. None of these

116. Multiprocessor uses large caches but limited process that shares_____
a. Memory bus
b. **Single memory bus**
c. Double memory bus
d. None of these

117. Distributed are shares also referred to as tightly coupled and loosely coupled multiprocessor respectively and hence called _____
a. **Coupled multiprocessor**
b. Shared multiprocessor
c. Distributed multiprocessor
d. None of these

118. Which consist if a numbers of processor can be accessed among various shared memory modules?
a. Coupled memory multiprocessor
b. **Shared memory multiprocessor**
c. Distributed memory multiprocessor
d. None of these

119. Which keeps a number of processors in which virtual storage space is assigned for redundant execution:
a. Coupled memory multiprocessor
b. Shared memory multiprocessor
c. **Distributed memory multiprocessor**
d. None of these

120. The memory capacity in system is considered because the connecting processors are used_____:

a. **Network**
b. Internet
c. Intranet
d. None of these

121. Intercrosses arbitration system for multiprocessor shares a _____:

a. Primary bus
b. **Common bus**
c. Domain bus
d. All of these

122. Which is used to decentralize the decision to avail greater flexibility to the system that makes processor or microprocessor in a very short:

a. **Arbitration**
b. Centralized
c. Both a & b
d. None of these

123. Which is signal tells that an arbitration of the access bus is possible during interprocessing:

a. DBA
b. **BAP**
c. BNA
d. None of these

124. Which signal bus request :

a. BAP
b. BNA
c. BAL
d. **DBA**

125. Which signal on the bus indicates that request from process arbitration is to be processed:

a. BAL
b. **BREQ**
c. BM4
d. DBA

126. Which signal is exchange information by bus:
a. **BECH**
b. BM4
c. BAL
d. All of these

127. Which signal on bus applies +1 to the priority of resolution circuits of the arbitration designate a new arbitration:
a. BM4
b. BAL
c. **BNA**
d. DBA

128. Which signal create 3 lines of bus in which signals from the encoded number of processors:
a. **BM1 to BM3**
b. BAL
c. Both
d. None of these

129. Which signal request the validation signal make active if its logic level is 0 and validate signals from BM1 to BM3:

a. BAL
b. **BM4**
c. BNA
d. All of these

130. Which signal represents synchronization signal decided by interprocess arbitration with a certain delay or signal DMA:

a. **BAL**
b. BNA
c. Both
d. None of these

131. In which condition only one process holds a resource at a given time:

a. **Mutual exclusion**
b. Hold and wait
c. Both
d. None of these

132. In which condition one process holds the allocated resources and other waits for it:

a. No preemption
b. **Hold and wait**
c. Mutual exclusion
d. All of these

133. In which condition resource is not removed from a process holding:

a. Synchronization problem
b. **No preemption**
c. Hold and wait
d. None of these

134. In which condition busy waiting, programmer error, deadlock or circular wait occurs in interprocessing:

a. **Synchronization problem**
b. No preemption
c. Hold and wait
d. None of these

135. Mechanism can be referred to as adding a new facility to the system hence known as _____:

a. Process
b. **Arbitration**
c. Both a & b
d. None of these

136. Which is a mechanism used by the OS to ensure a systematic sharing of resources amongst concurrent resources:

a. Process synchronous
b. Process system
c. **Process synchronization**
d. All of these

137. _____ is basically sequence of instructions with a clear indication of beginning and end for updating shared variables

a. **Critical section**
b. Entry section
c. Remainder section
d. All of these

138. Which provides a direct hardware support to mutual exclusion

a. **Test-and-set(TS)**
b. Swap instruction
c. Wait instruction
d. Signal instruction

139. A process waiting to enter its critical section may have to wait for unduly_____:
a. Short time or may have to wait forever
b. **Long time or may have to wait forever**
c. Short time or may have to wait for long time
d. Long time or may have to wait for short time

140. Which is a modified version of the TS instruction which is designed to remove busy-waiting:
a. Swap instruction
b. Wait instruction
c. Signal instruction
d. **Both b & c**

141. PCB stands for:
a. **Process control block**

142. ____ gets activated whenever the process encounters a busy condition code:
a. **Wait instruction**
b. Signal instruction
c. Both a & b
d. None of these

143. _____ are new and mutually exclusive operation:
a. Wait instruction
b. Signal instruction
c. **Both a & b**
d. None of these

144. _____ gets activated whenever a process leaves the critical region and the flag is set to false:
a. Wait instruction
b. **Signal instruction**
c. Both a & b
d. None of these

145. Which represent an abstraction of many important ideas in mutual exclusion:
a. Process synchronous
b. Process system
c. **Semaphores**
d. All of these

146. A semaphore is a _____ integer variable upon which two atomic operations wait and signal are defined:
a. Negative integer
b. **Non- Negative integer**
c. Positive integer
d. None of these

147. Which operation is executed as soon as a process exits from a critical section:

a. Wait
b. **Signal**
c. Both a & b
d. None of these

148. CCR stands for:
a. **Conditional critical region**

149. _____ is a control structure in a high-level programming language:
a. CPU
b. ALU
c. DDR
d. **CCR**

150. The exclusion between processes is ensured by a third semaphore called_____:
a. **Mutex**
b. Mutual
c. Memory
d. All of these

151. _____ semaphore provides mutual exclusion for accesses to the buffer pool and is initialized to the value:

a. **Mutex**
b. Mutual
c. Memory
d. All of these

152. Which processes access and manipulate the shared data concurrently:

a. Micro processes
b. **Several processes**
c. Both
d. None of these

153. Which section is basically a sequence of instruction with a clear indication of beginning and end for updating shared variables:

a. Racing section
b. **Critical section**
c. Both
d. None of these

154. In which section only one process is allowed to access the shared variable and all other have to wait:

a. **Critical section**
b. Racing section
c. Entry section
d. Remainder section

155. Which are the problem of critical section:

a. Mutual exclusion
b. Progress
c. Bounded wait
d. **All of these**

156. Which section refer to the code segment of a process that is executed when the process intends to enter its critical section:
a. Critical section
b. **Entry section**
c. Reminder section
d. None of these

157. Which section refer to the code segment where a shared resource is accessed by the process:
a. Reminder section
b. Entry section
c. Both
d. **None of these**

158. Which section is the remaining part of a process's code:
a. Racing section
b. Critical section
c. Entry section
d. **Reminder section**

159. How many conditions for controlling access to critical section:

a. 2
b. 4
c. **3**
d. 5

160. Which instruction provides a direct hardware support to mutual exclusion:

a. SP instruction
b. **TS instruction**
c. Both
d. None of these

161. Which instruction also improves the efficiency of the system:

a. Swap instruction
b. **TS instruction**
c. Both
d. None of these

162. Which instruction allows only one concurrent process to enter the critical section:

a. RP instruction
b. SP instruction
c. **TS instruction**
d. None of these

163. Which section problem can be solved simply in a uniprocessor environment if the we are able to prevent the occurrence of interrupt during the modification of a shared variable:

a. Entry section
b. **Critical section**
c. Non-critical section
d. None of these

164. The problem of readers and writers was first formulated by _____:

a. P.J. Courtois
b. F.Heymans
c. D.L. Parnas
d. **All of these**

165. Which is a situation in which some process wait for each other's actions indefinitely:

a. Operating system
b. **Deadlock**
c. Mutex
d. None of these

166. _____system handles only deadlocks caused by sharing of resources in the system:

a. **Operating system**
b. Deadlock
c. Mutex
d. None of these

167. A deadlocks occurs when the how many conditions are met:
a. 1
b. 2
c. 3
d. **4**

168. Which are the characteristics of deadlocks:

a. Mutual exclusion
b. Hold and wait
c. No pre-emption
d. Circular wait
e. **All of these**

169. RAG stands for:
a. **Resource allocation graph**

170. How many events concerning RAG can occur in a system:
a. 1
b. 2
c. **3**
d. 4

171. Which are the events concerning RAG can occur in a system:
a. Request for a resource
b. Allocation of a resource
c. Release of resource
d. **All of these**

172. How many methods for handling deadlocks:
a. 1 b. 2
c. **3** d. 4

173. Which are the method for handling deadlocks:

a. Deadlock prevention
b. Deadlock avoidance
c. Deadlock detection
d. **All of these**

174. How many condition that should be met in order to produce a deadlock:

a. 2 b. **4**
c. 6 d. 8

175. Which are the condition that should be met in order to produce a deadlock:

a. Mutual exclusion b. Hold and Wait
c. No preemption
d. Circular wait e. **All of these**

176. In protocol each process can make a request only in an _____:

a. **Increasing order** b. Decreasing order
c. Both a & b d. None of these

177. In protocol above mentioned _____protocol are used then the circular wait-condition can not hold:

a. 1 b. **2**
c. 3 d. 4

178. Which state refers to a state that is not safe not necessarily a deadlocked state:

a. Safe state b. **Unsafe state**
c. Both a & b d. None of these

179. _____ a direct arrow is drawn from the process to the resource rectangle to represent each pending resource request:
a. TS b. SP
c. CCR d. **RAG**

180. The attributes of a file are:
a. Name b. Identifier
c. Types d. Location
e. Size f. Protection
g. Time, date and user identification
h. **All of these**

181. The various file operation are:
a. Crating a file b. Writing a file
c. Reading a file
d. Repositioning within a file
e. Deleting a file truncating a file
f. **All of these**

182. Which operations are to be performed on a directory are:
a. Search for a file b. Create a file
c. Delete a file d. List a directory
e. Rename a file
f. Traverse the file system
g. **All of these**

183. Which memory is assembled between main memory and CPU:
a. Primary memory b. **Cache memory**
c. Both a & b d. None of these

184. Which is considered as semi-conductor memory , which is made up of static RAM:
a. Primary memory b. **Cache memory**
c. Both a & b d. None of these

185. Which is one of the important I/O devices and is most commonly used as permanent storage device in any processor:
a. Soft disk b. **Hard disk**
c. Both a & b d. None of these

186. _____ can read any printed character by comparing the pattern that is stored in the computer:
a. SP b. CCR
c. RAG d. **OCR**

187. Which system is a typical example of the readers and writers problem:
a. **Airline reservation system**
b. Airport reservation system
c. Both
d. None of these

188. Which lock can arise when two processes wait for phone calls from one another:

a. Spine lock b. **Dead lock**
c. Both d. None of these

189. Which lock is more serious than indefinite postponement or starvation because it affect more than one job:

a. **Deadlock** b. Spinelock
c. Both d. None of these