6.15 PROGRAMMABLE DEVICES :

6.15.1 Application specific integrated circuit- ASIC:

Different types of standard ICs like decoder, encoder, code converter, multiplexer, de multiplexer, comparator, parity generator, checker etc. are manufactured by various manufacturers for the design and application. All these ICs are called the fixed function ICs because each type of IC is developed for certain definite function. For example, binary to Gray code converter IC can convert the binary code in to the Gray code only. When the digital circuit is not much complicated, the circuit can be designed by making use of some fixed function ICs.

But when the circuit is more complicated, large numbers (hundreds or thousands) of such fixed functions are to be used.

Disadvantages of fixed function ICs :

1. More space is required.
2. Power consumption increases.
3. Cost increases.
4. There is no security as the design can be copied.

To overcome the above problems, application specific integrated circuits (ASIC) are developed. In this the user (circuit designer) gives the design to the manufacturer and the manufacturer fabricates the IC as per the design.

Advantages of ASIC :

1. Space occupied is reduced.
2. Power consumption is reduced.
3. Cost can be reduced if large numbers of ICs are manufactured.
4. The design cannot be copied.
5. Overall size is reduced.

Disadvantages of ASIC :

1. Initial cost is high.
2. Cost also increases as the testing methods are to be developed.

6.15.2 Programmable logic devices-PLDs :

ASICs were developed to overcome the difficulties experienced in realizing the design of the complicated logic circuit. These difficulties can be overcome by making use of the programmable logic design (PLD) also.

Programmable logic device is a LSI chip, which contains numbers of logic gates, flip-flops, registers. These are interconnected and kept on the chip. The connections are made through the fusible links. User retains the links which are required and fuse the remaining links (this is called programming the PLD).

Advantages of PLD :

1. Space occupied is less.
2. Power consumption is less.
3. Reliability is more.
4. Development cost is less.
5. Design can be done quickly.
6. Operation is quick.
7. Amendments can be made in the circuit.
8. Security of design increases.
9. Circuit testing is simple.

The following devices are used as PLD.

1. Programmable read only memory (PROM)
2. Programmable array logic (PAL)
3. Programmable logic array (PLA)
4. Simple programmable logic devices (SPLD)
5. Complex programmable logic devices (CPLD)
6. Field programmable gate array (FPGA)

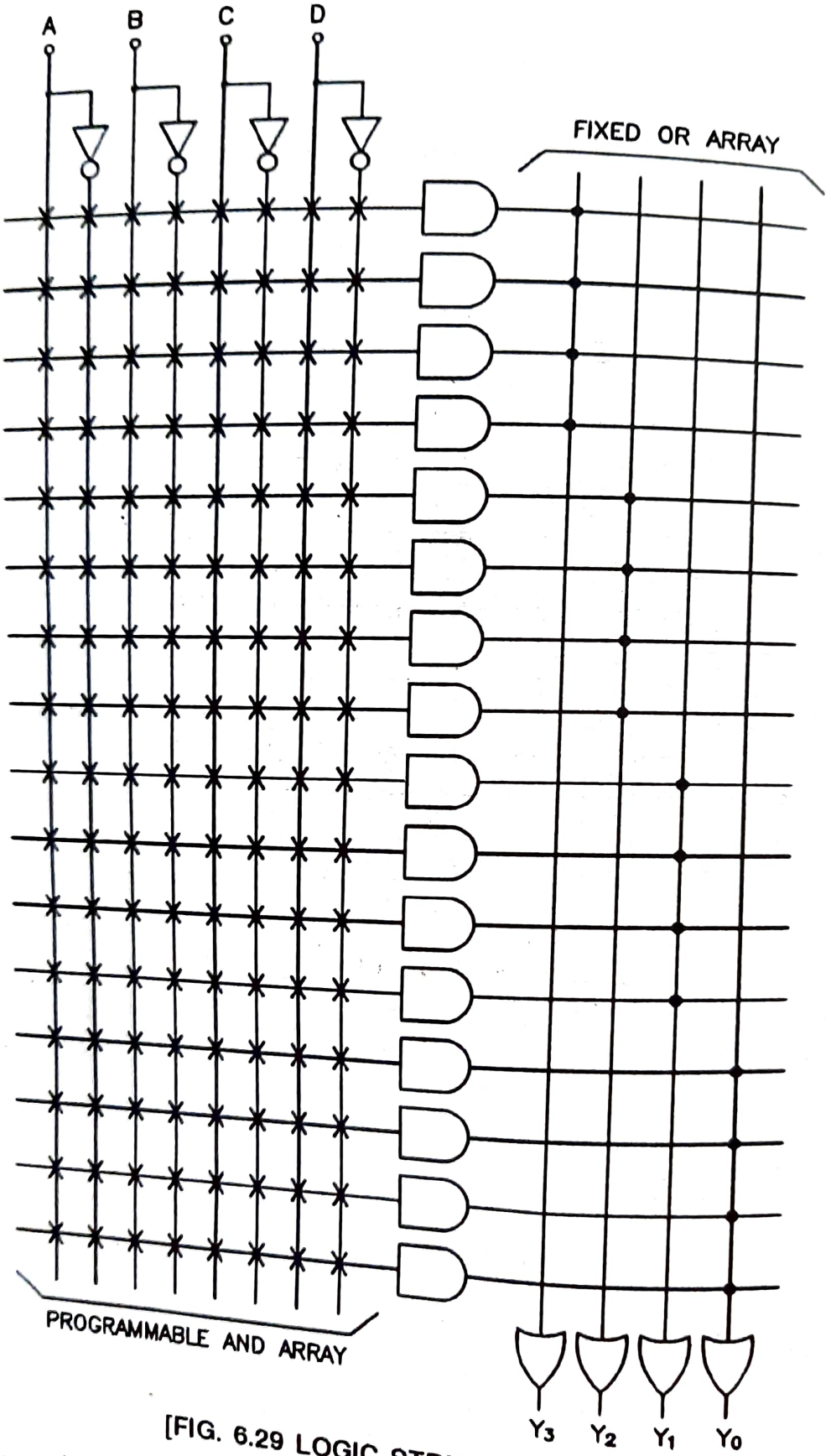
6.15.3 Use of ROM/PROM as PLD :

ROM is basically the memory device in which data is stored permanently. The data stored is not wiped off when the power supply fails. It is used to store fixed type of storage like tables etc.

ROM can also be used for the design of the combinational logic, but in this the users themselves cannot program the device. The user gives the design to the manufacturer and the manufacturer makes suitable arrangement of connection of diodes or gates in ROM IC.

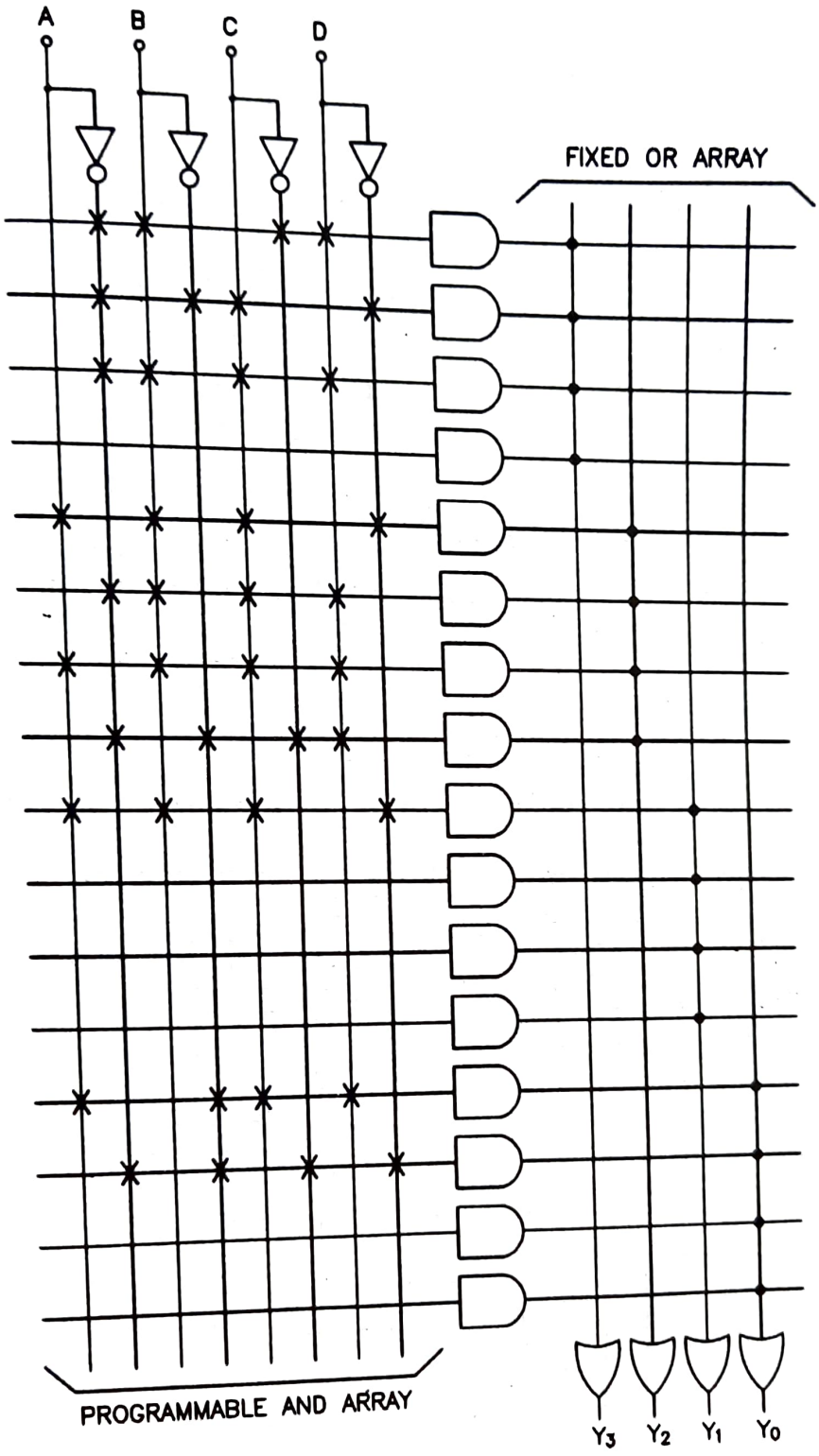
PROM means programmable read only memory. PROM is used to generate Boolean function

6.15.4 Programmable array logic-PAL :



[FIG. 6.29 LOGIC STRUCTURE OF PAL]

The arrangement in PAL is reverse than that of PROM. In this the AND gates on th input side are programmable while the OR gates on the output side are fixed. PAL can also b used to obtain the SOP function. Arrangement of PAL is shown in figure 6.29.



[FIG. 6.30 PROGRAMMING OF PAL]

In this there are four inputs A, B, C, D and four outputs Y_0 through Y_3. There are four inverters and 16 nos. of 8-input AND gates which are programmable. There are 16-input-four nos. of OR gates which cannot be programmed.

Let us suppose we require the following SOP functions.

$$Y_3 = \overline{A}B\overline{C}D + \overline{A}\overline{B}C\overline{D} + \overline{A}BCD$$

$$Y_2 = ABC\overline{D} + \overline{A}BCD + ABCD + \overline{A}\overline{B}\overline{C}D$$

$$Y_1 = ABC\overline{D}$$

$$Y_0 = A\overline{B}CD + \overline{A}\overline{B}\overline{C}\overline{D}$$

Let us consider Y_3.

The first min term is $\overline{A}B\overline{C}D$. So, we have to retain the link nos. second, third, sixth and seventh in the first row and all other links have to be fused.

The second min term is $\overline{A}\overline{B}C\overline{D}$. So, we have to retain the link nos. second, fourth, fifth and eighth in the second row and All other links have to be fused.

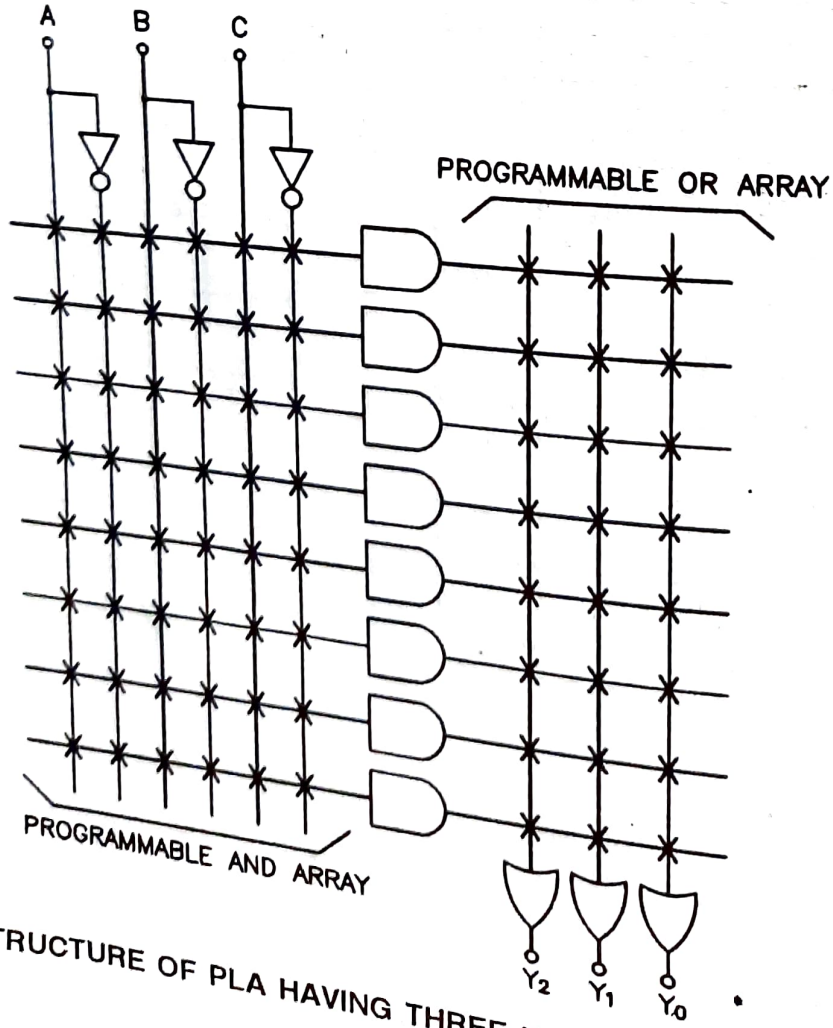
The third min term is $\overline{A}BCD$. So, we have to retain the link nos. second, third, fifth and seventh in the third row and fuse all other links.

There is no fourth min term. So, we shall have to fuse all the eight links in the fourth row.

Similarly we can program for Y_2, Y_1 and Y_0.

Programmed PAL is shown in figure 6.30.

6.15.5 PROGRAMMABLE LOGIC ARRAY – PLA :



[FIG. 6.31 STRUCTURE OF PLA HAVING THREE INPUTS AND THREE OUTPUTS]

The programmable logic array (PLA) includes the characteristics of both the PROM and PAL. In this the AND gates on the input side are programmable and OR gates on the output side are also programmable. Moreover, EX-OR gate is supplied for the controlled inversion. It is either masked programmable type or field programmable type like PLA. In figure 6.31, PLA structure of three inputs and three outputs is shown.

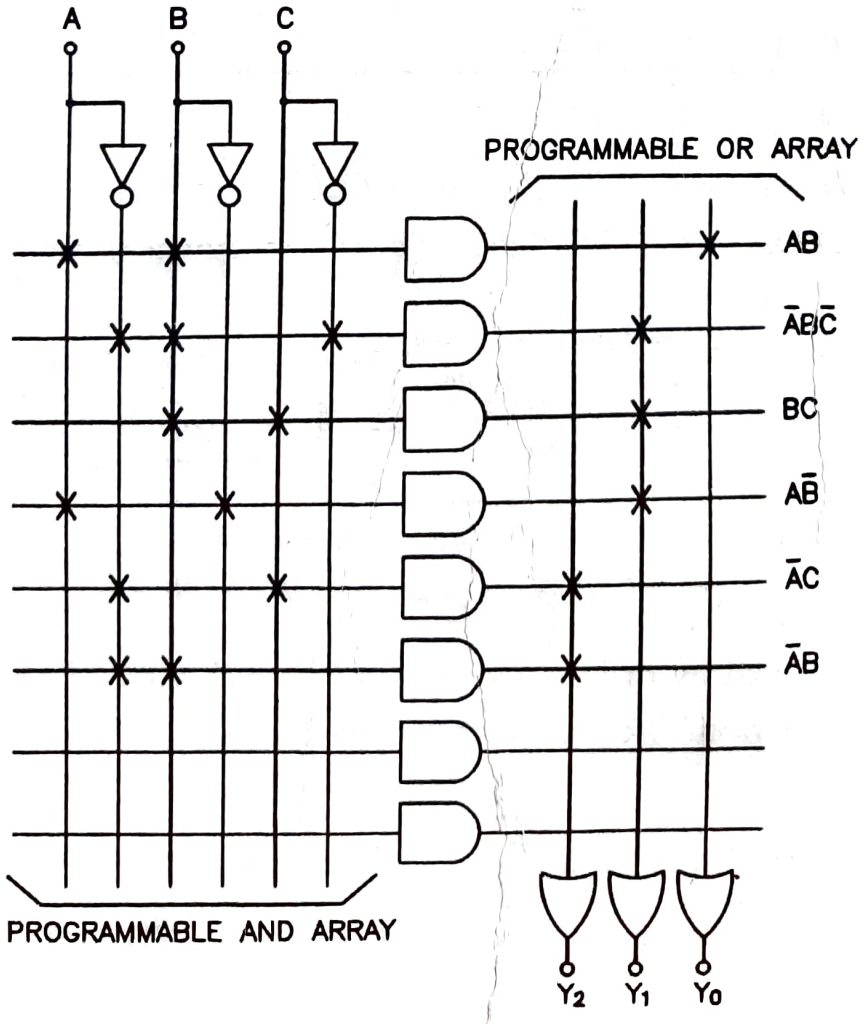
Let us suppose we have to obtain the following Boolean functions.

$$Y_0 = AB$$

$$Y_1 = \overline{A}B\overline{C} + BC + A\overline{B}$$

$$Y_2 = \overline{A}C + \overline{A}B$$

The programmed PLA programmed like PROM and PAL is shown in figure 6.32.



[Fig. 6.32 Programming of PLA]

6.15.6 Comparison of PROM, PAL and PLA :

PROM	PAL	PAL
1. AND array is fixed and OR array is programmable.	1. OR array is fixed and AND array is programmable.	1. Both the AND array and OR array are programmable.
2. Cost is less and easy to use.	2. Cheap and easy to use.	2. Costly and complex.
3. All min terms are decoded.	3. AND array is programmed for required min terms.	3. AND array can be programmed for necessary min terms.
4. Only the standard SOP form of Boolean function can be implemented.	4. Boolean function in SOP form can be implemented.	4. Boolean function in SOP form can be implemented.