Sequential logic circuit

Digital Electronics (DE)

Information and Communication Technology

Prepared by Prof.jaydip siyara

Outline

- Ripple/Asynchronous Counters
  - Ripple up-down, Modulo or Modulus counter
- Synchronous Counters
  - Up counter, Down counter using different FFs
- Decade and BCD counter
- Presettable Counters
- Decoding a Counter
- Designing Counters with Arbitrary Sequences
- Registers
  - Buffer, Shift, Bidirectional, Universal
  - applications of shift registers,
    - serial to parallel converter, parallel to serial converter
    - ring counter, sequence generator,

Registers

Section - 2

Registers

- As a flip-flop (FF) can store only one bit of data, a 0 or a 1, it is referred to as a single-bit register.
- A register is a group of FFs used to store binary data.
- The storage capacity of a register is the number of bits (1s and 0s) of digital data it **can retain.**
- Loading a register means setting or resetting the individual FFs, i.e. inputting data into the register so that their states correspond to the bits of data to be stored.
- To store **n bit n D/SR/JK FF** are connected together.
- Loading may be serial or parallel.
- In serial loading, data is transferred into the register in serial form i.e. one bit at a time.
- In parallel loading, the data is transferred into the register in parallel form meaning that all the FFs are triggered into their new states at the same time.
- Types of registers are:
  1. Shift register,
  2. Bidirectional shift register,
  3. Universal shift register

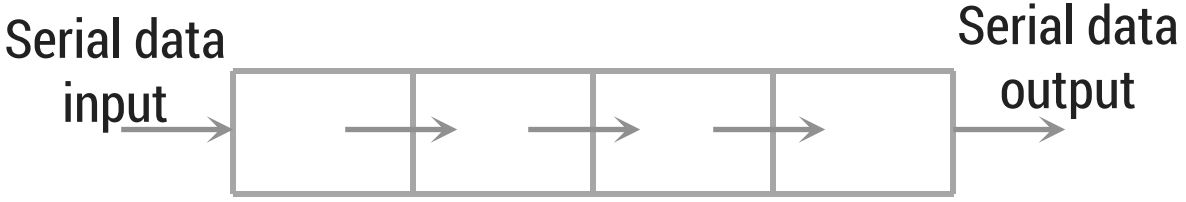
Shift Register

- A number of FFs connected together such that data may be shifted into and shifted out of them is called a shift register.
- Data may be shifted into or out of the register either in serial form or in parallel form.
- So, there are four basic types of shift registers:
  1. serial-in, serial-out (SISO)
  2. serial-in, parallel-out (SIPO)
  3. parallel-in, serial-out(PISO)
  4. parallel-in, parallel-out(PIPO) (Buffer register)

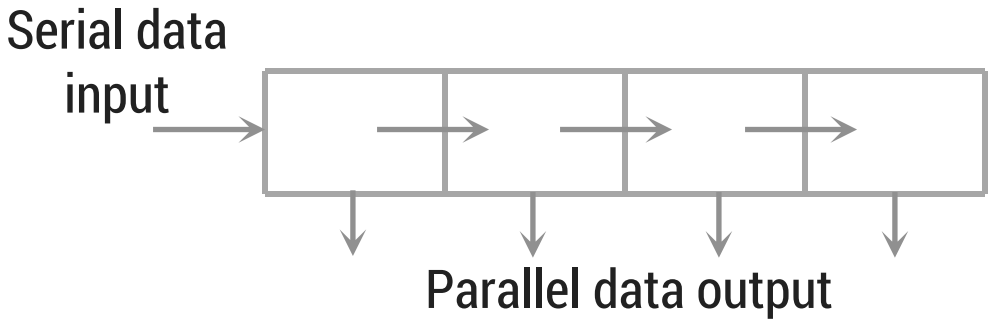
Find-out IC name

- Data may be rotated left or right. Data may be shifted from left to right or right to left at will, i.e. in a bidirectional way.
- Also, data may be shifted in serially (in either way) or in parallel and shifted out serially (in either way) or in parallel.

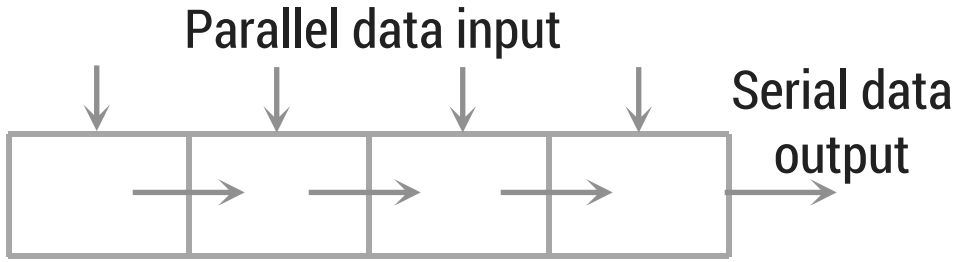
Data transmission in shift register



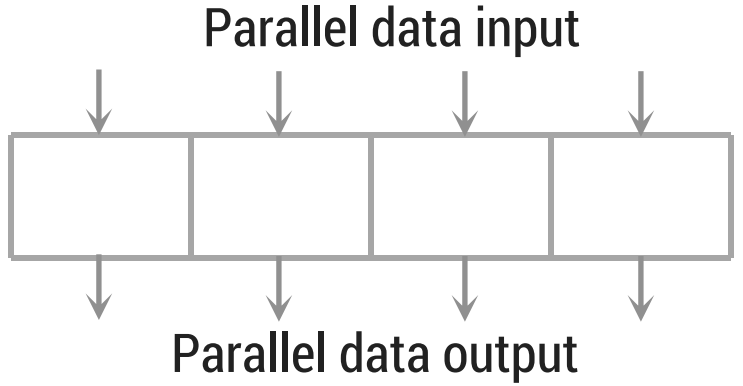
Serial-in, serial-out shift-right, shift register



Serial-in, parallel-out, shift register



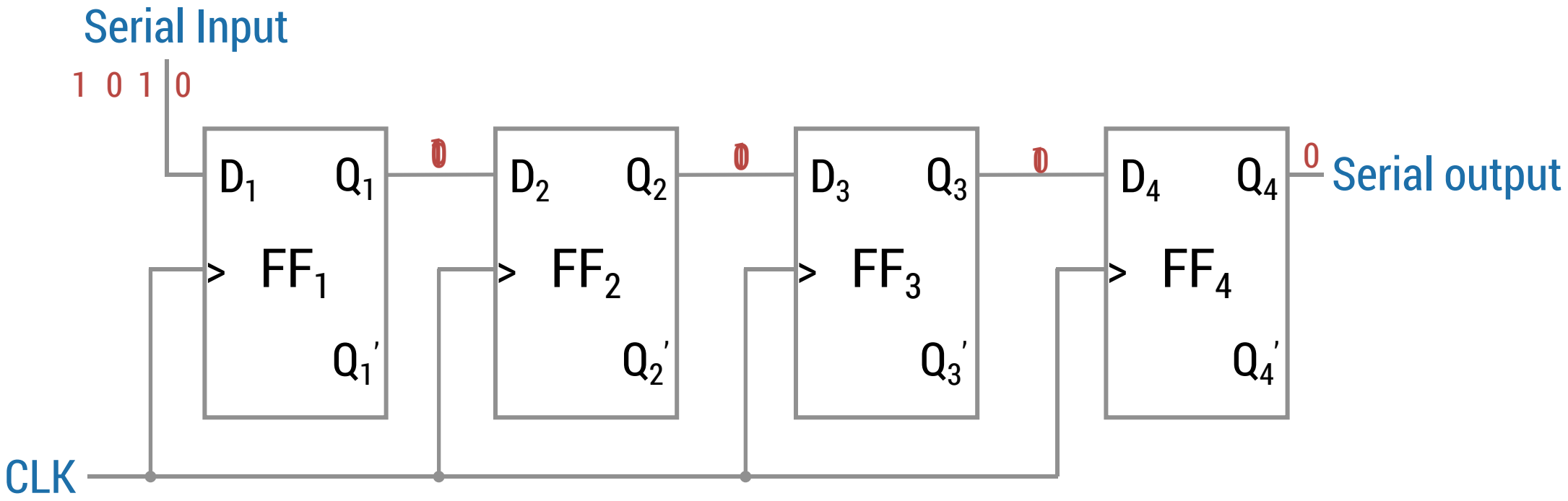
Parallel-in, serial-out, shift register



Parallel-in, parallel-out, shift register

Serial-in, Serial-out, Shift-right, Shift register

To store 4bit 4 D Flip-flops are connected.



Data = 1010

In SISO n number of clock pulses are required to store n bit word.

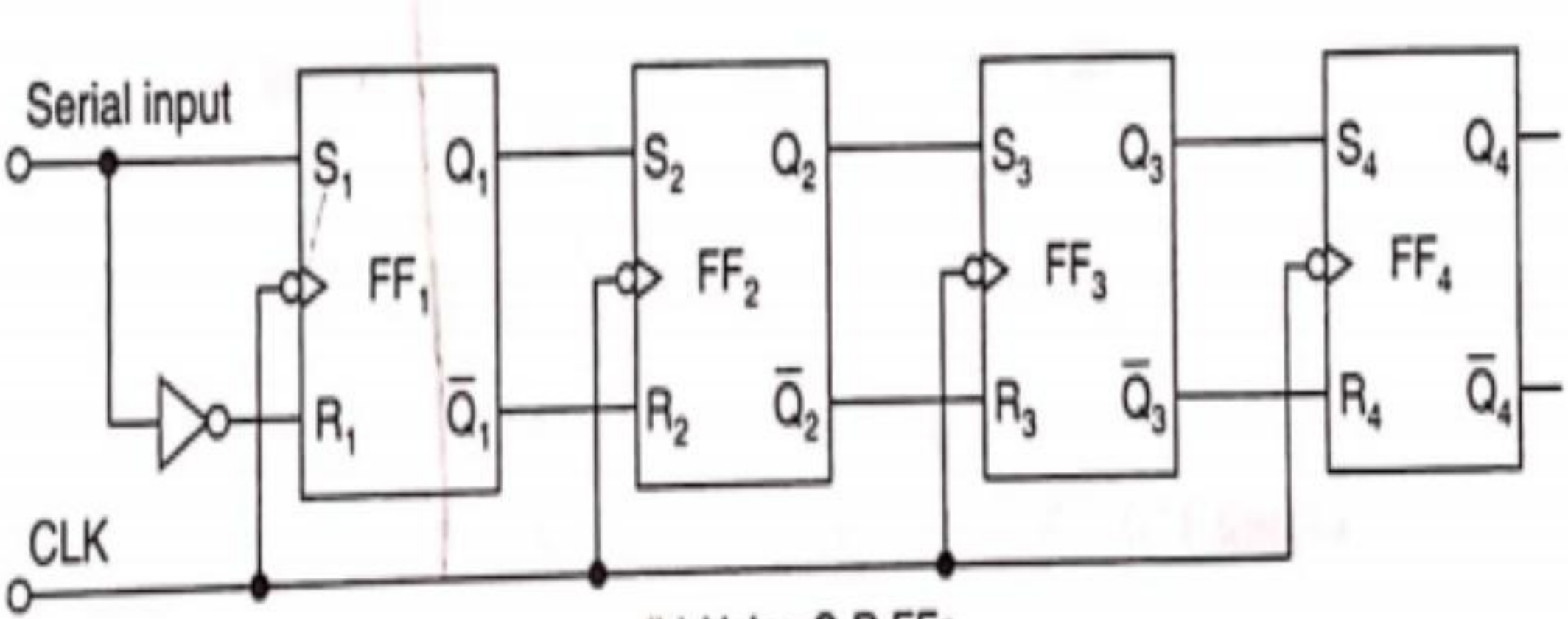
For description refer this site: http://studytronics.weebly.com/shift-registers.html

If data is 1011.Truth table is as below,

Timing pulse	Q_A	Q_B	Q_C	Q_D
Initial value	0	0	0	0
After 1st clock pulse	1	0	0	0
After 2nd clock pulse	1	1	0	0
After 3rd clock pulse	0	1	1	0
After 4th clock pulse	1	0	1	1

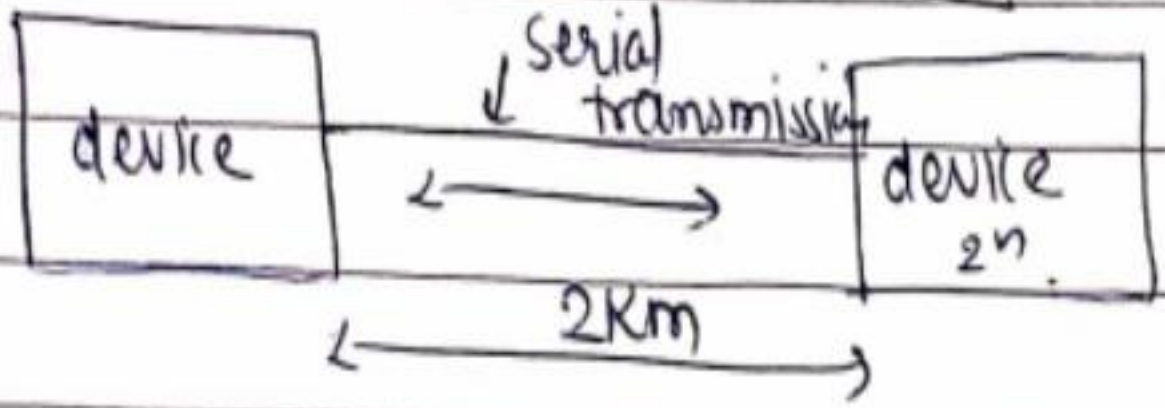
To the waveform see this you tube video: https://www.youtube.com/watch?v=zazz_LH1Sxo

SISO using SR FF



(b) Using S-R FFs

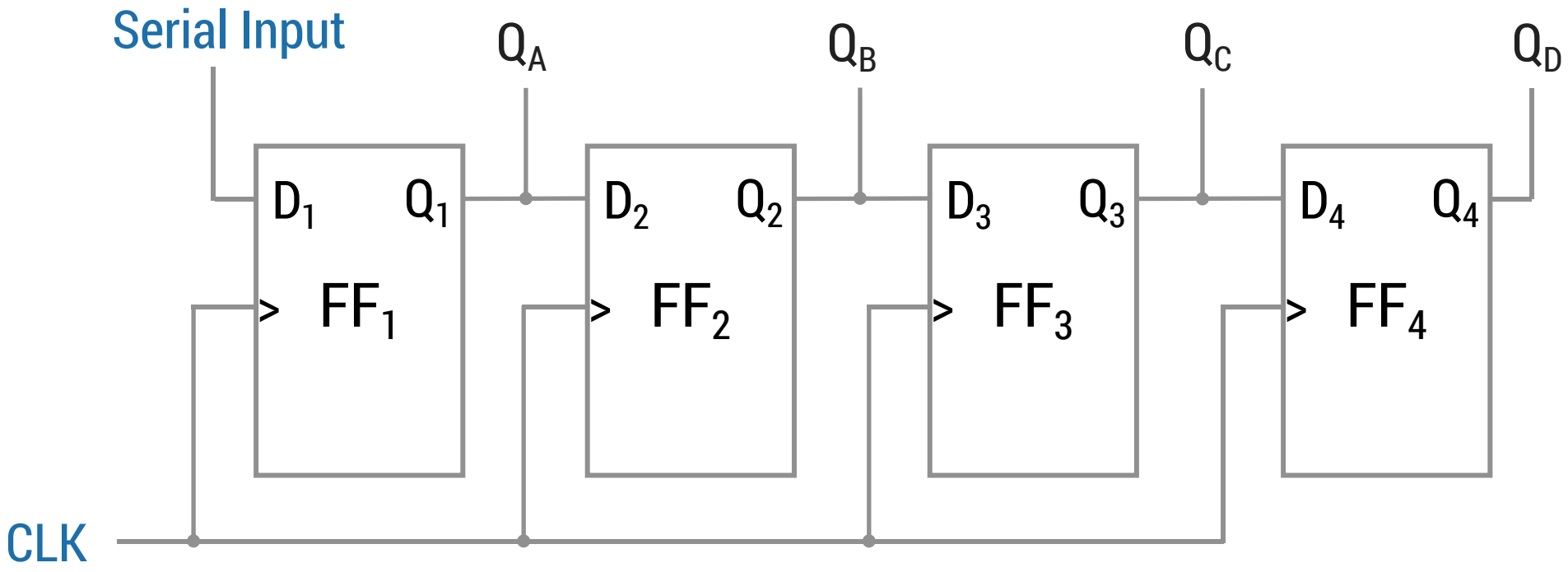
* Application of serial operation :-



a) 1 bit will be transmitted in 1 clock pulse. ⇒ Speed ↓

b) when distance is large only one conductor will be required.

Serial In Parallel Out using DFF(SIPO)

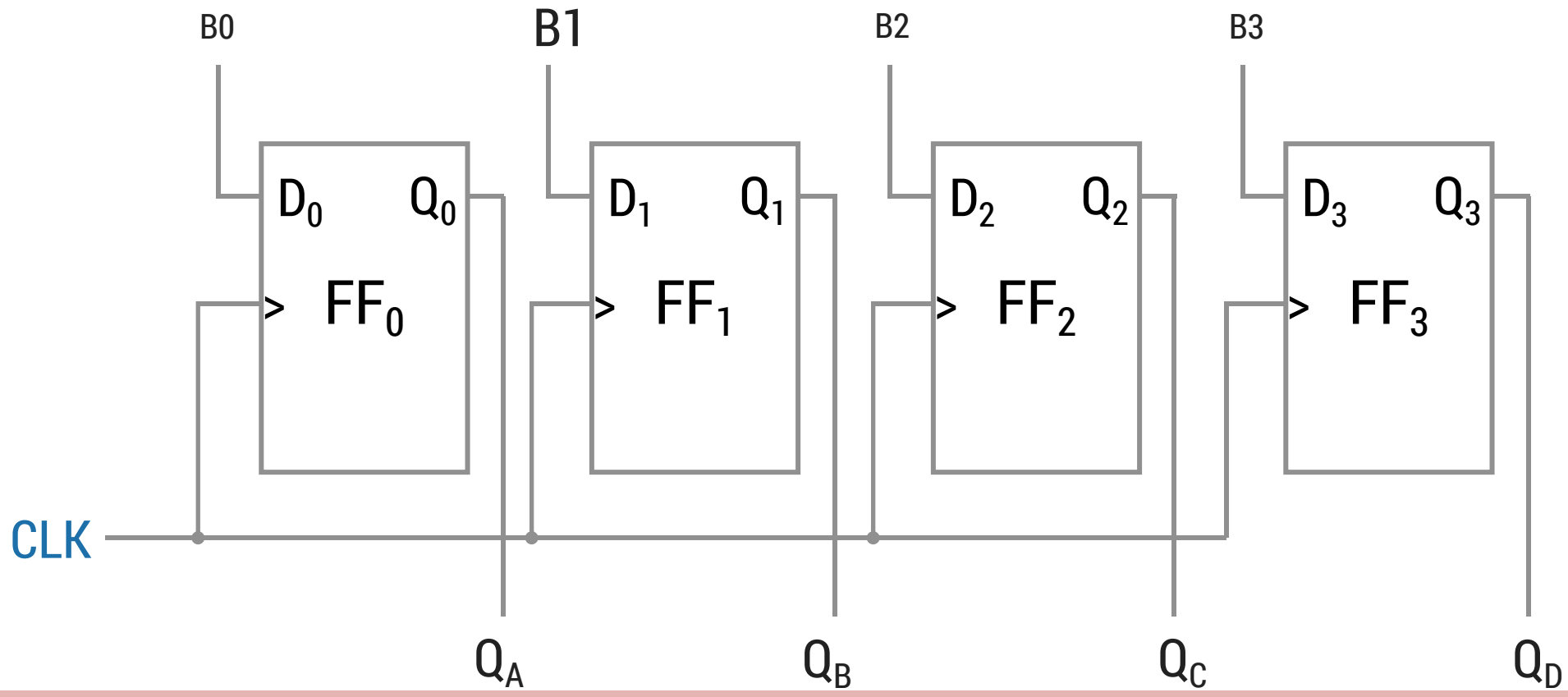


For description refer this site:
http://studytronics.weebly.com/shift-registers.html .

Serial In Parallel Out using DFF(SIPO)

1. In such types of operations, the data is entered serially and taken out in parallel fashion.
2. Data is loaded bit by bit. The outputs are disabled as long as the data is loading.
3. As soon as the data loading gets completed, all the flip-flops contain their required data, the outputs are enabled so that all the loaded data is made available over all the output lines at the same time.
4. 4 clock cycles are required to load a four bit word. Hence the speed of operation of SIPO mode is same as that of SISO mode.

Parallel-in, Parallel-out, Shift register(PIPO)



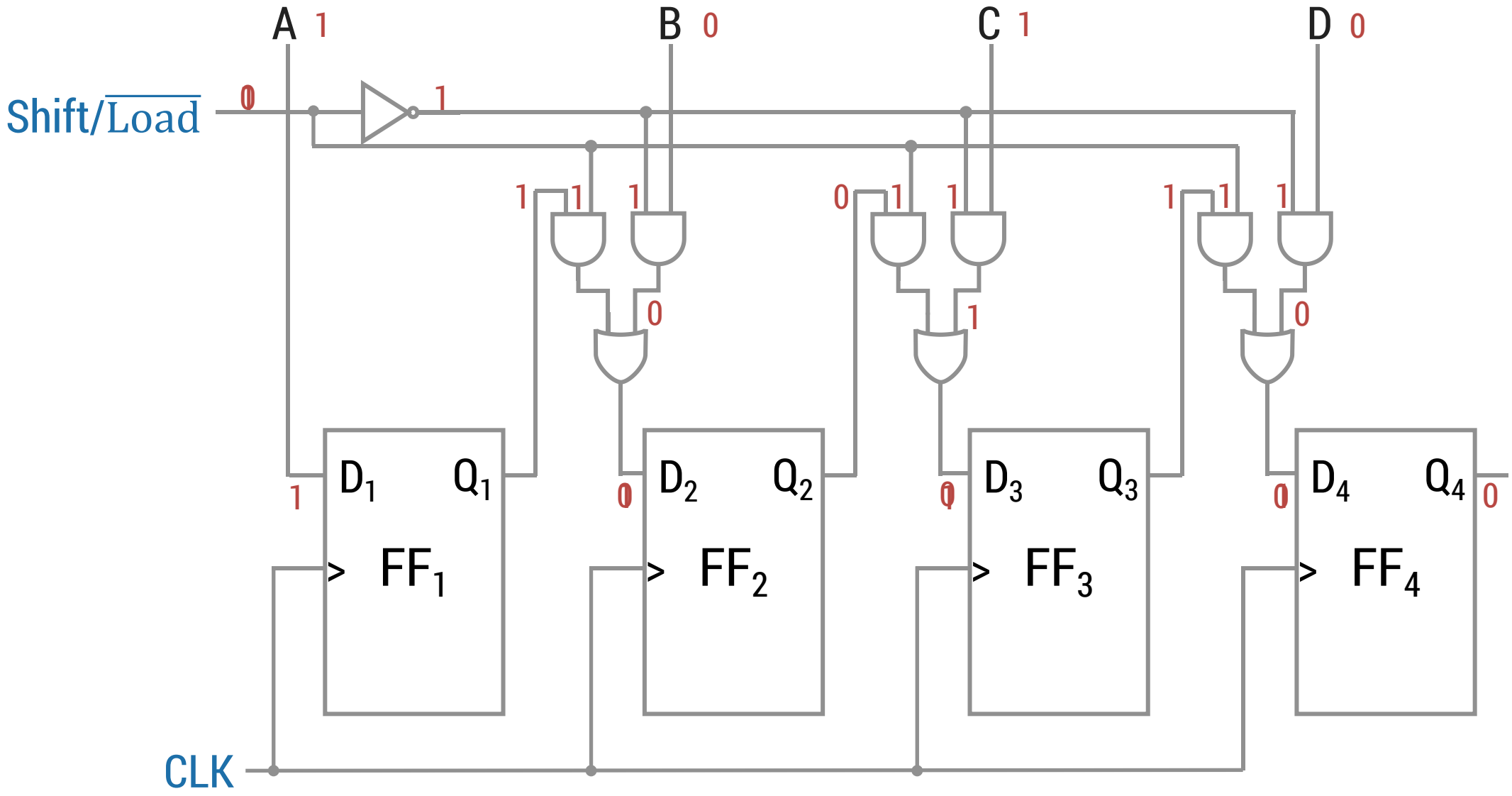
- It is called Buffer register.
- In one clock pulse all bits are stored simultaneously . Only one clock pulse is required.

For description refer this site: http://studytronics.weebly.com/shift-registers.html

Parallel-in, Parallel-out, Shift register(PIPO)

In this mode, the 4 bit binary input B0, B1, B2, B3is applied to the data inputs D0, D1, D2, D3respectively of the four flip-flops. As soon as a negative clock edge is applied, the input binary bits will be loaded into the flip-flops simultaneously. The loaded bits will appear simultaneously to the output side. Only clock pulse is essential to load all the bits.

Parallel-in, Serial-out, Shift register



Parallel-in, Serial-out, Shift register

- The input data will enter in parallel that means at a time to all flip flop and output will get serially.

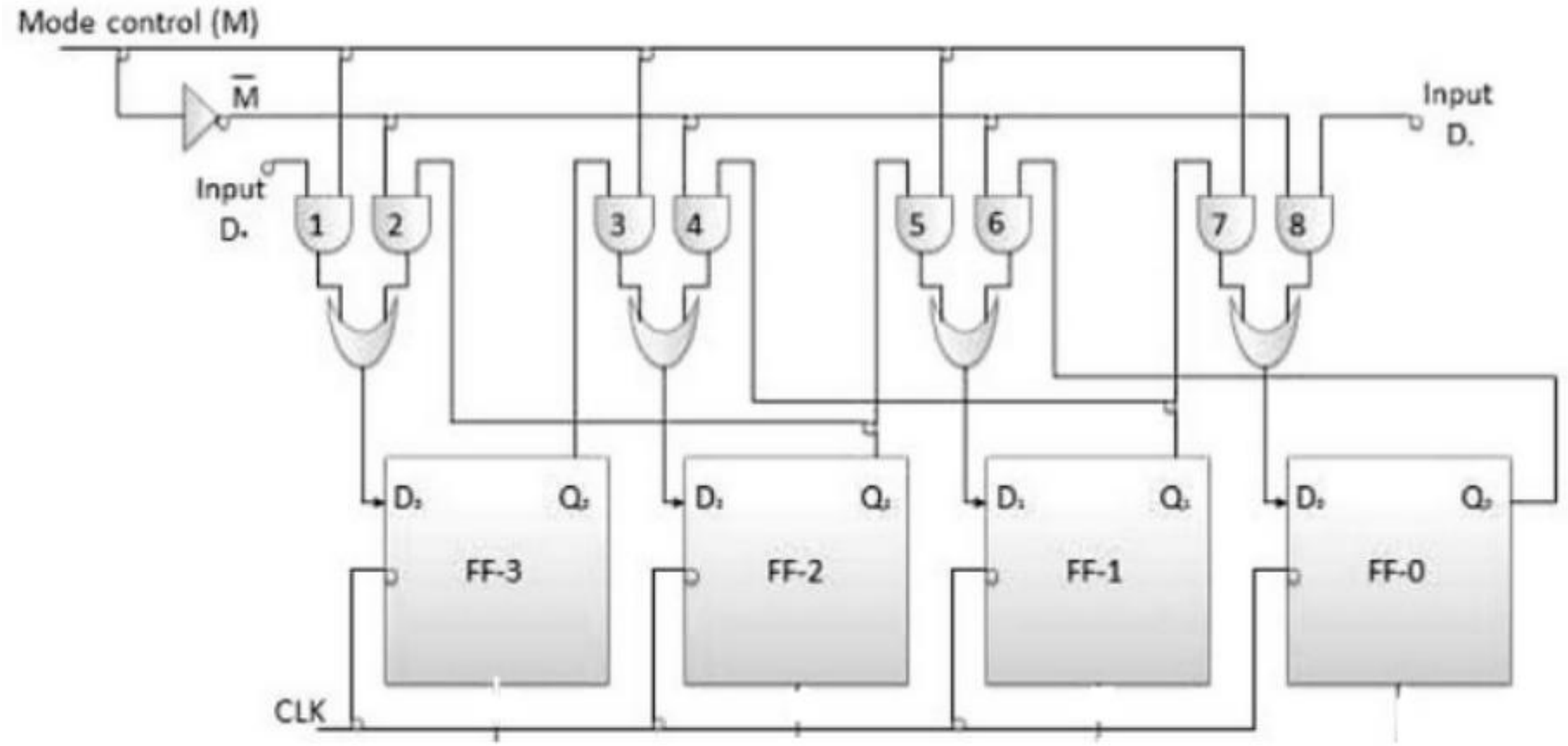
- Then all input are feed the inputs of different 4 number of flip flop. With single clock pulse all data are enter to all 4 **flip flops.**

- 4 bit parallel in serial out shift register, A, B, C, and D are the four parallel data input lines and SHIFT / LOAD (SH / LD) is a **control input** that allows the four bits of data at A, B, C, and D inputs to enter into the register in parallel or shift the data in serial.
- if SHIFT / LOAD = 0 then data will be stored and
  if SHIFT / LOAD = 1 then data will be shifted.
-

4 bit Bidirectional shift register

- **It is the registers which are capable of shifting the data either right or left depending on the mode selected.**
- If the **mode = 1**, the data will be shifted towards the right direction
- if the **mode = 0**, the data will be shifted towards the left direction.
- 4- D flip-flops which are connected.
- The input data is connected at two ends of the circuit and depending on the mode selected only one and gate is in the active state.

4 bit Bidirectional shift register



Application of Register

- Temporary data storage i.e. Microprocessor.
- Data transfer and data manipulation .i.e. multiplication and division by 2.
- Produce time delay to digital circuits.
- Used in communication lines where demultiplexing of a data line into several parallel line is required.
- Data Converter.
- Ring counter.
- Johnson or Twisted ring counter

https://learn.circuitverse.org/docs/seq-msi/registers.html#serial-in-serial-out

Counters

Introduction

- A counter – a group of flip-flops connected together to perform counting operations (flip-flops are used to construct counters)

- Two categories:
  1) Asynchronous counter
  2) Synchronous counter

- Classification of counters
  - UP counter
  - DOWN counter
  - UP/DOWN counter

https://learn.circuitverse.org/docs/seq-msi/counters.html

Introduction- Counters

- Primary purpose is to produce a **specified output pattern sequence**.
- The total number of **states** is called its **modulus.**
- *An n-bit counter that counts through all its natural states and does not skip any of the states has a modulus of 2^n.*

- If a counter has **m distinct states** then it is called a **mod-m counter.**
-

- n bit counter has n flip flops and it has 2^n distinct states with maximum count of $2^n - 1$.

Asynchronous Counters v/s Synchronous Counters

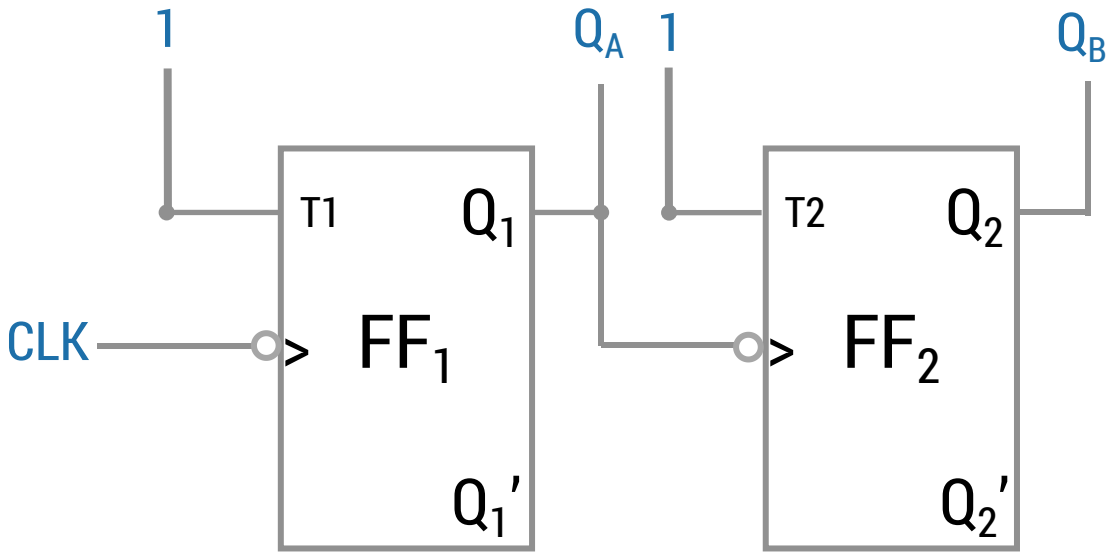
Asynchronous/Ripple/serial Counters	Synchronous/Ring/Johnson/parallel Counters
FFs are connected in such a way that the output of the first FF connected to the clock for the second FF, the output of the second the clock of the third and so on.	There is no connection between the output of first FF and clock input of next FF and so on.
All the FFs are not clocked simultaneously.	All the FFs are clocked simultaneously.
Design and implementation is very simple even for more number of states.	Design and implementation becomes tedious and complex as the number of states increases.
Main drawback of these counters is their low speed as the clock is propagated through a number of FFs before it reaches the last FF.	Since clock is applied to all the FFs simultaneously the total propagation delay is equal to the propagation delay of only one FF. Hence they are faster.
the delay is dependent of the size of the counter.	the delay is independent of the size of the counter.

1.Asynchronous Counters

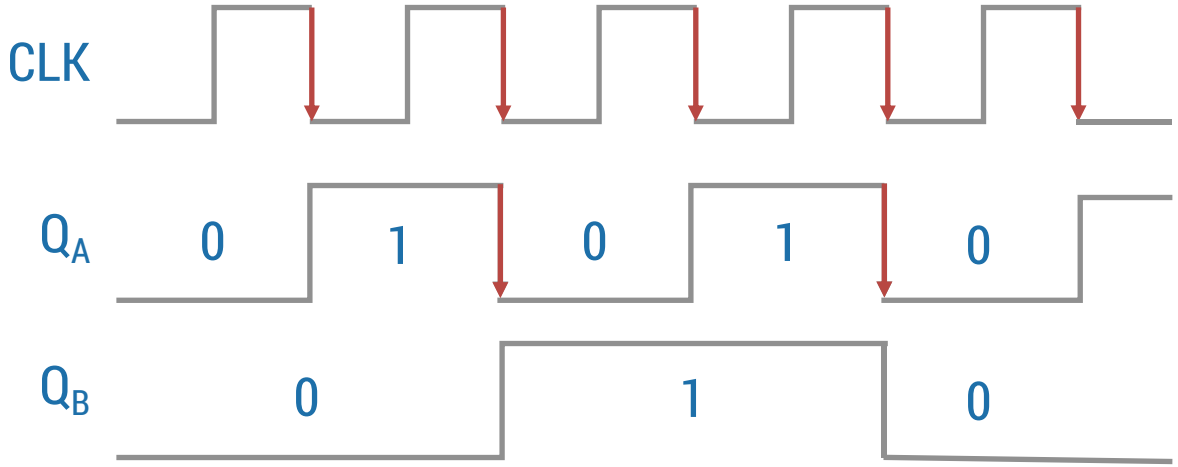
- Group of flip-flops, **count** a stream of **pulses applied** to the counter's Clock input.
- The output is a binary value whose value is equal to the number of pulses received at the CK input.

- Mod 4 counter →4 states(0,1,2,3) → 2 bit counter → 2 FF are required.
- Mod 8 counter → 8 states(0,1,2,3,4,5,6,7) → 3 bit counter → 3 FF are required.
- Mod 10 counter(BCD) → 10 states(0,1,2,3,4,5,6,7,8,9) → 4 bit counter → 4 FF are required.(https://www.youtube.com/watch?v=EVb1cn4QOGM)
- Mod N counter→ N states(0,1,2,3,4……..N-1) → n bit counter → n FF are required.

2-bit Ripple Up-Counter- T FF(MOD-4) Negative Edge-triggered



CLK	Present State		Next State	
	Q_B	Q_A	Q_B	Q_A



http://falstad.com/circuit/e-counter.html

2-bit Ripple Up-Counter- T FF(MOD-4) Negative Edge-triggered

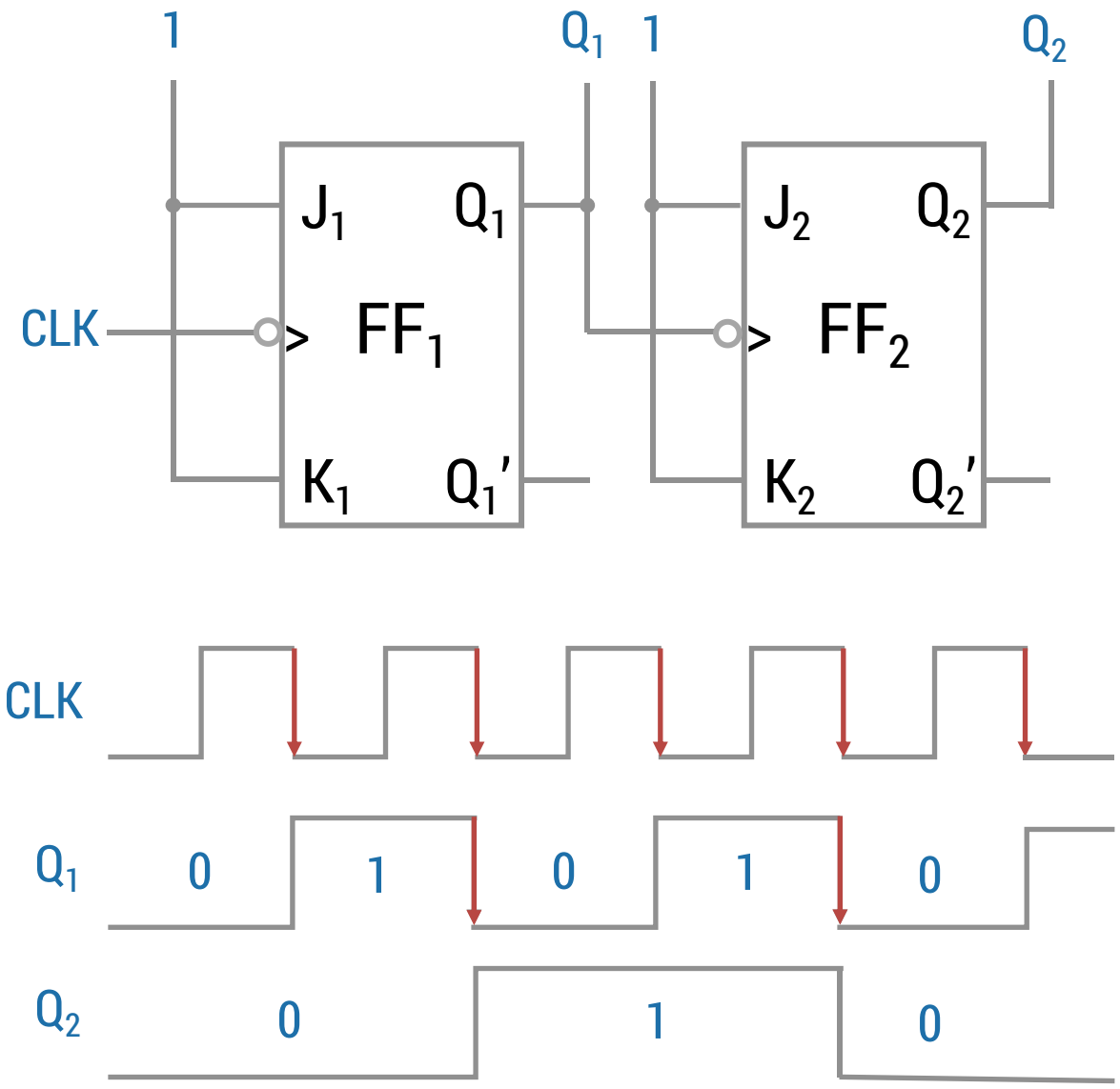
Operation

S.N.	Condition	Operation
1	**Initially let both the FFs be in the reset state**	Q_BQ_A = 00 initially
2	**After 1st negative clock edge**	As soon as the first negative clock edge is applied, FF-A will toggle and Q_A will be equal to 1. Q_A is connected to clock input of FF-B. Since Q_A has changed from 0 to 1, it is treated as the positive clock edge by FF-B. There is no change in Q_B because FF-B is a negative edge triggered FF. Q_BQ_A = 01 after the first clock pulse.
3	**After 2nd negative clock edge**	On the arrival of second negative clock edge, FF-A toggles again and Q_A = 0. The change in Q_A acts as a negative clock edge for FF-B. So it will also toggle, and Q_B will be 1. Q_BQ_A = 10 after the second clock pulse.
4	**After 3rd negative clock edge**	On the arrival of 3rd negative clock edge, FF-A toggles again and Q_A become 1 from 0. Since this is a positive going change, FF-B does not respond to it and remains inactive. So Q_B does not change and continues to be equal to 1. Q_BQ_A = 11 after the third clock pulse.

2-bit Ripple Up-Counter- T FF(MOD-4) Negative Edge-triggered

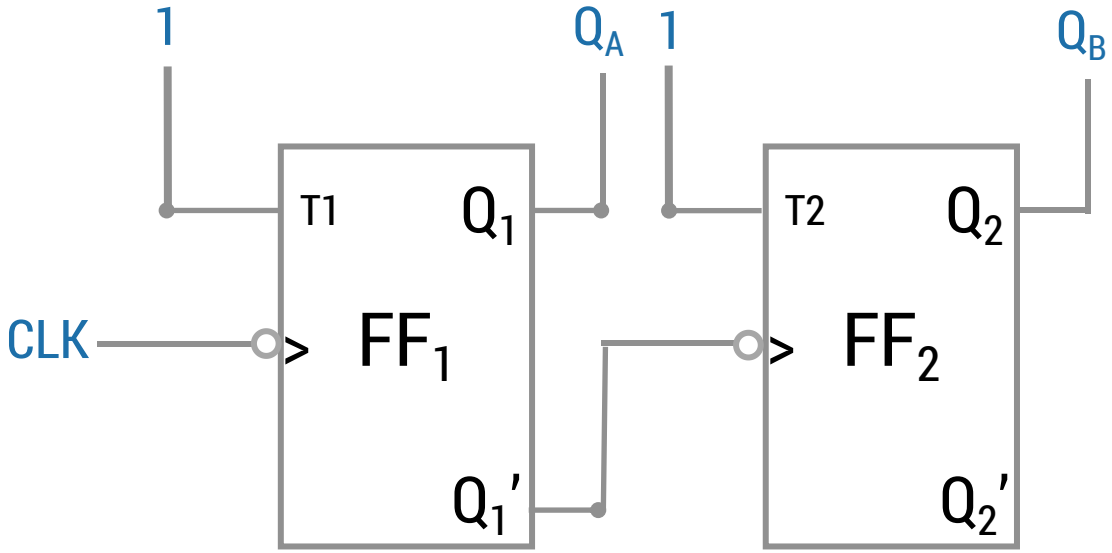
5	**After 4th negative clock edge**	On the arrival of 4th negative clock edge, FF-A toggles again and Q_A becomes 1 from 0. This negative change in Q_A acts as clock pulse for FF-B. Hence it toggles to change Q_B from 1 to 0. Q_BQ_A = 00 after the fourth clock pulse.

2-bit Ripple Up-Counter using Negative Edge-triggered Flip-Flop

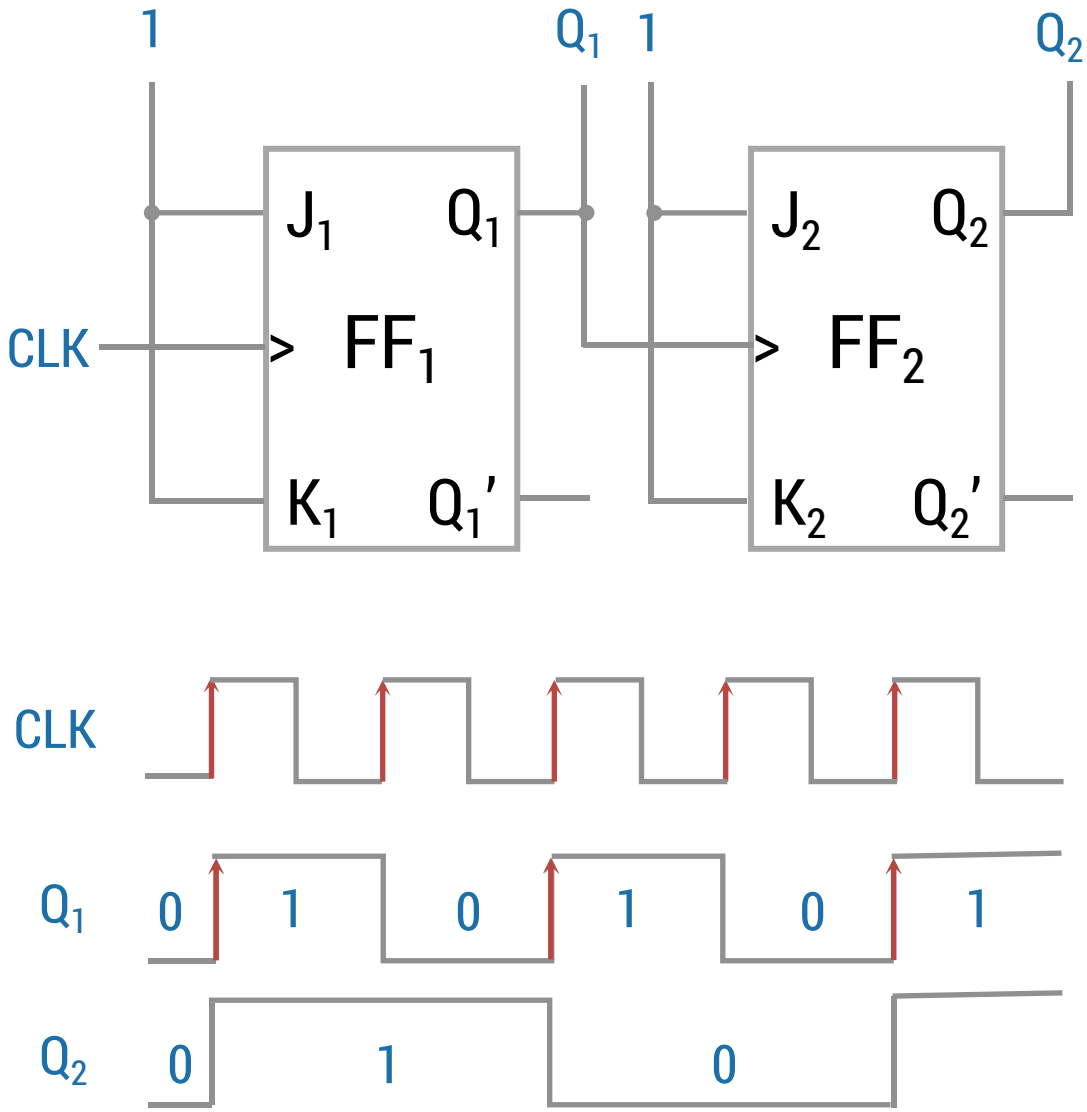


CLK	Present State		Next State	
	Q_2	Q_1	Q_2	Q_1

2-bit Ripple down-Counter- T FF(MOD-4) Negative Edge-triggered

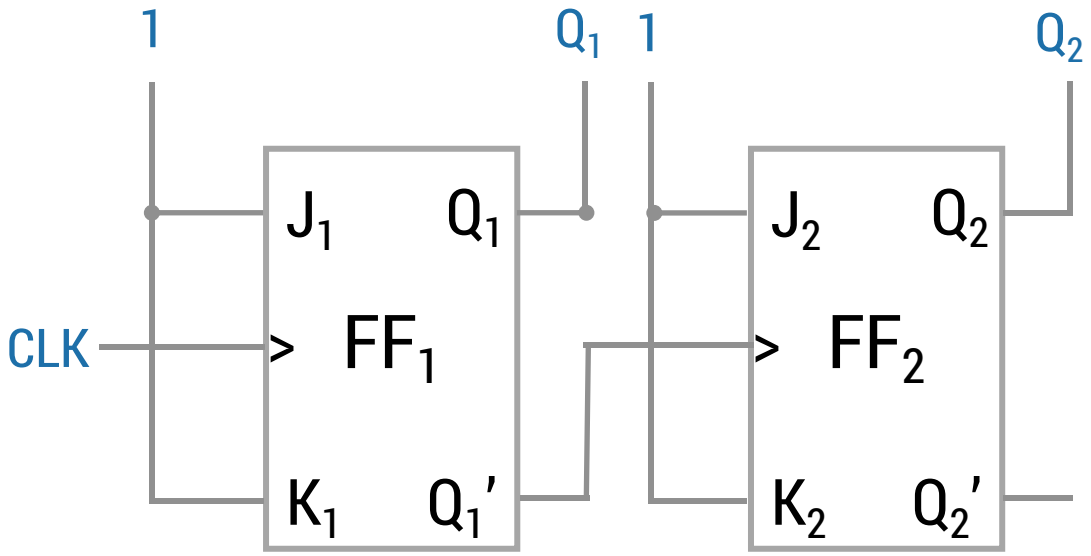


2-bit Ripple Down-Counter using Positive Edge-triggered Flip-Flop



CLK	Present State		Next State	
	Q_2	Q_1	Q_2	Q_1

2-bit Ripple up-Counter using Positive Edge-triggered Flip-Flop



Refer this video link to understand 3 bit and 4 bit negative edge up-counter.

1. https://www.youtube.com/watch?v=ucCtDhYFCJs
2. https://www.youtube.com/watch?v=s1DSZEaCX_g
3. https://www.youtube.com/watch?v=eEeBh8jfDjg

- Design 4-bit Ripple up -Counter using JK FF. Write its TT and Draw Timing diagram.
- Refer Anil K.Maini page no 431

- ripple counter type number 74293 IC.→ four-bit binary ripple counter

Homework

1. Design 3-bit Ripple up -Counter using T/JK FF. Write its TT and Draw Timing diagram.(http://www.prajval.in/edudetail/284/2413/%3Cp%3E%3Cstrong%3EDesign-3-bit-ripple-up-counter-using-negative-edge-triggered-JK-flip-flops-Also-draw-the-waveforms%3C-strong%3E%3C-p%3E-).

1. Design-3-bit-ripple-up-counter-using-negative-edge-triggered-JK-flip-flops-Also-draw-the-waveforms.
2. Design 3-bit Ripple down -Counter using T/JK FF. Write its TT and Draw Timing diagram.
3. Design 4-bit Ripple down -Counter using T/JK FF. Write its TT and Draw Timing diagram.

Up/Down counter

2 bit up/down ripple counter

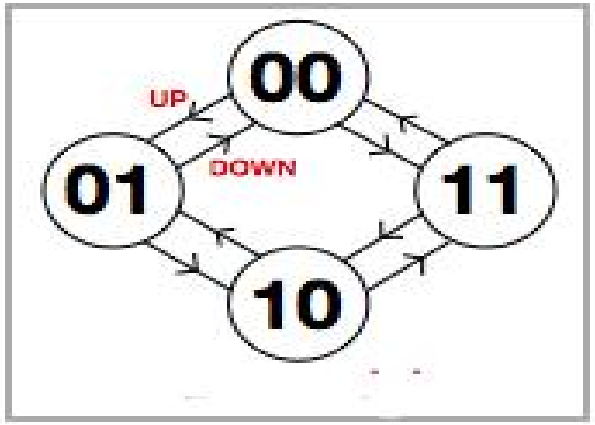
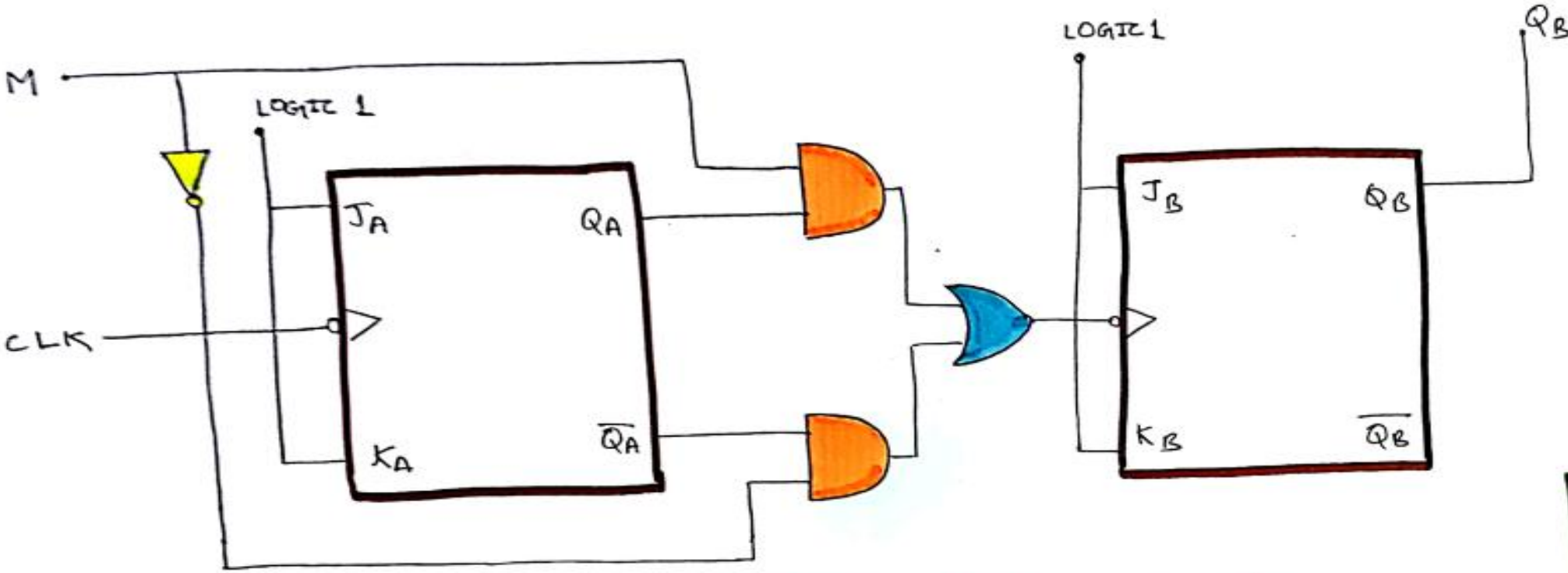


Illustration states 2-bit UP/DOWN counter.



2-bit ripple up/down counter

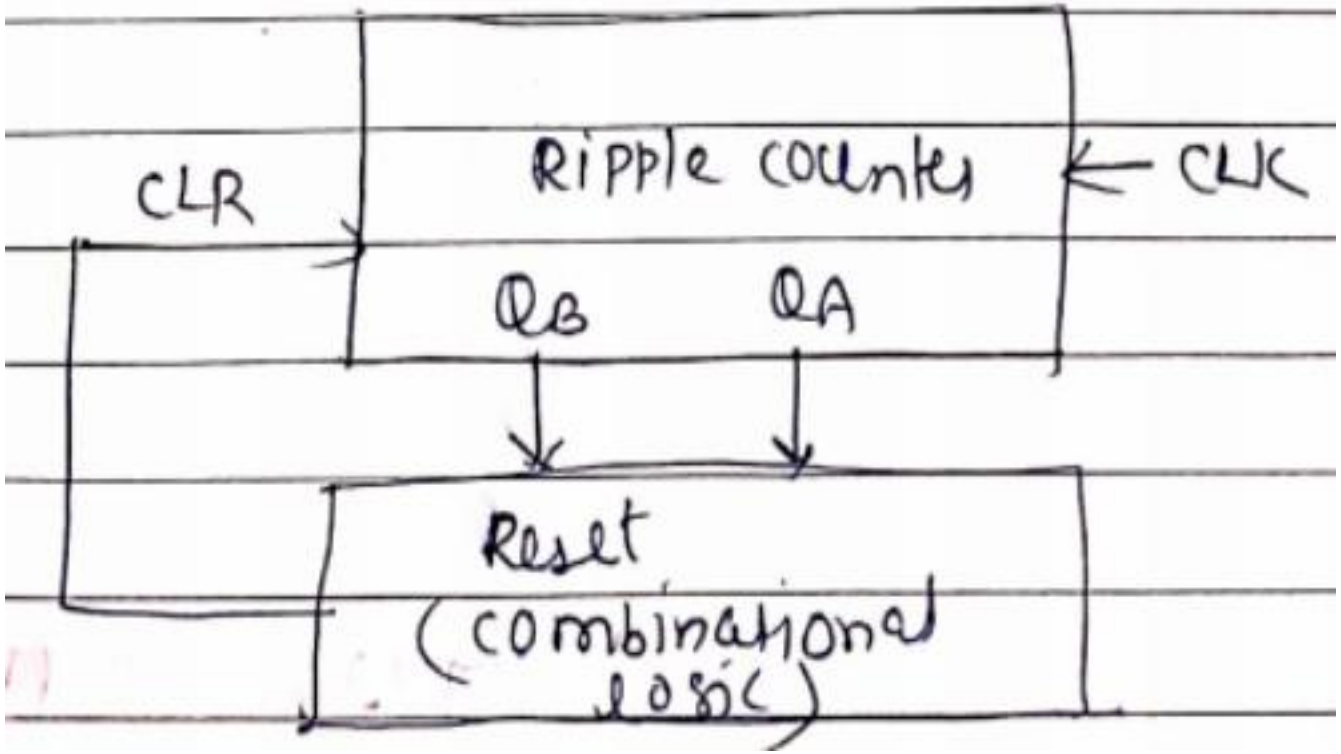
M=1 UP COUNTER

M=0 DOWN COUNTER

Source: https://player.uacdn.net/lesson-raw/CTESRQVKPN4ZGUOGTTJX/pdf/7718910058.pdf

Modulus Ripple Counter

- Mod 4 counter → 2 bit counter → 2 FF are required.
- Mod 8 counter → 3 bit counter → 3 FF are required.
- Mod N counter→ n bit counter → n FF are required.
- Modulus counter= Ripple Counter+ Reset Logic(Combinational logic)



https://www.youtube.com/watch?v=5mfN5KdjcQw

Asynchronous Counters

Design Steps:

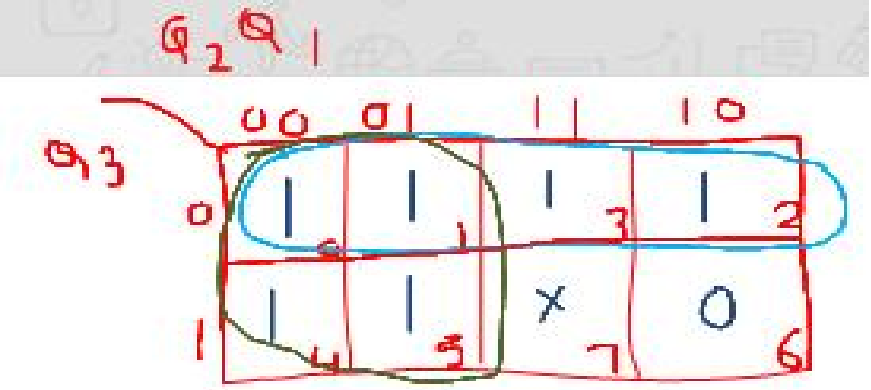
1. Determine number of flip-flop.
2. Choose the type of flip-flop.
3. Write the truth table of the counter.
4. Make the Kmap and derive the boolean equation.
5. Design counter.

Mod-6 Asynchronous/Ripple Counter

1. Mod -6 , 6 states → 0,1,2,3,4,5
2. Maximum no is 5 ,so 3 bits are required.
3. No. of FF=3
4. Types of flip-flop T.
5. Make a truth table.
6. Boolean equations.
7. Design final counter circuit.

Mod-6 Asynchronous/Ripple Counter

After pulses	State			Reset(R)
	Q_3	Q_2	Q_1	
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	**0**



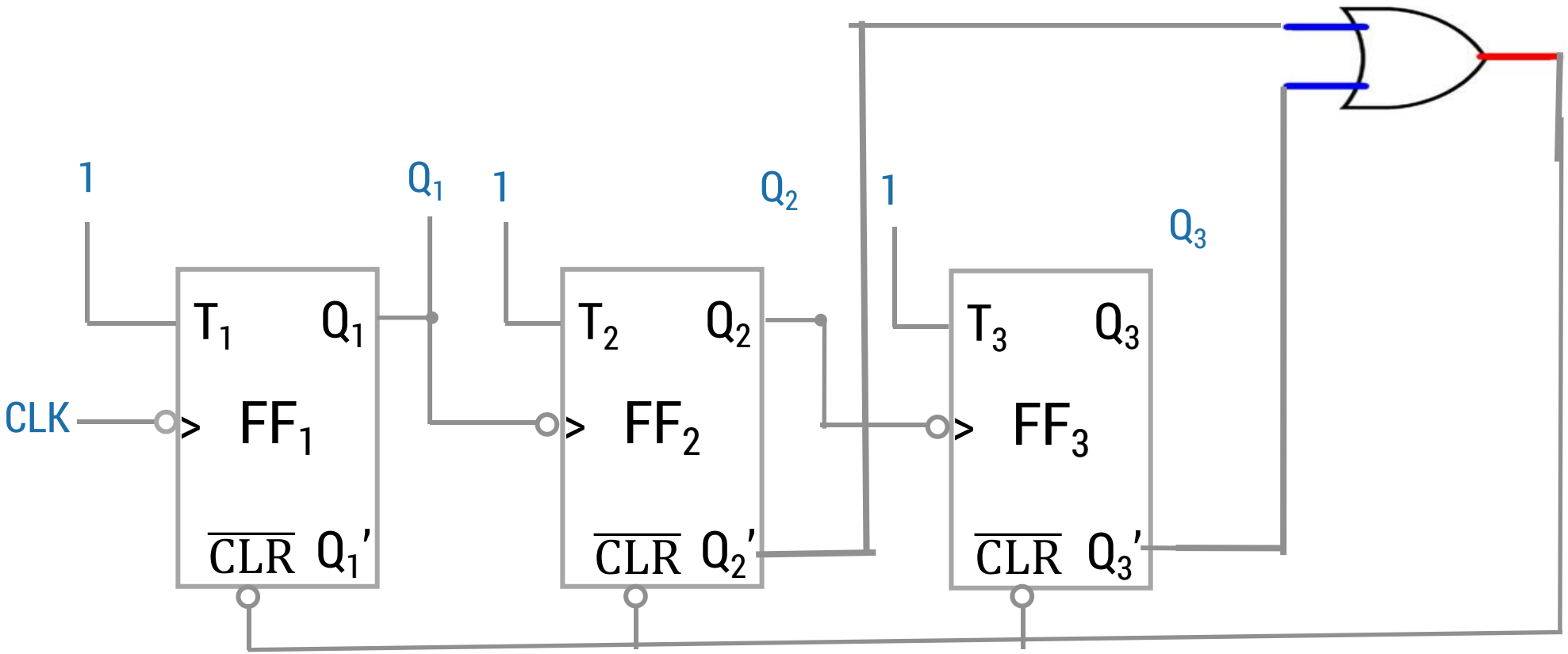
R = 1 for 000 to 101

R = 0 for 110

R = x for 111

$R = Q_3' + Q_2'$

Mod-6 Asynchronous Counter



Decade and BCD Counters

- that goes through 10 unique output combinations and then resets as the clock proceeds further.
- MOD-10 counter.
- 4 flip-flops.
- From 16 states any of the six states by using some kind of feedback is skipped.
- A decade counter does not necessarily count from 0000 to 1001.
- It could even count as 0000, 0001, 0010, 0101, 0110, 1001, 1010, 1100, 1101, 1111, 0000.
- https://upload.wikimedia.org/wikipedia/commons/3/33/DecadeCounter.jpg
- https://www.electronicsforu.com/technology-trends/learn-electronics/decade-counter-circuit-basics
- *BCD counter* is a special case of a decade counter.
- Counts from 0000 to 1001 and then resets.
- https://everycircuit.com/circuit/5043097612320768/decade-counter
- https://www.elprocus.com/bcd-counter-circuit-working/

Synchronous Counters

Section - 4

http://falstad.com/circuit/e-synccounter.html

Design of Synchronous Counters

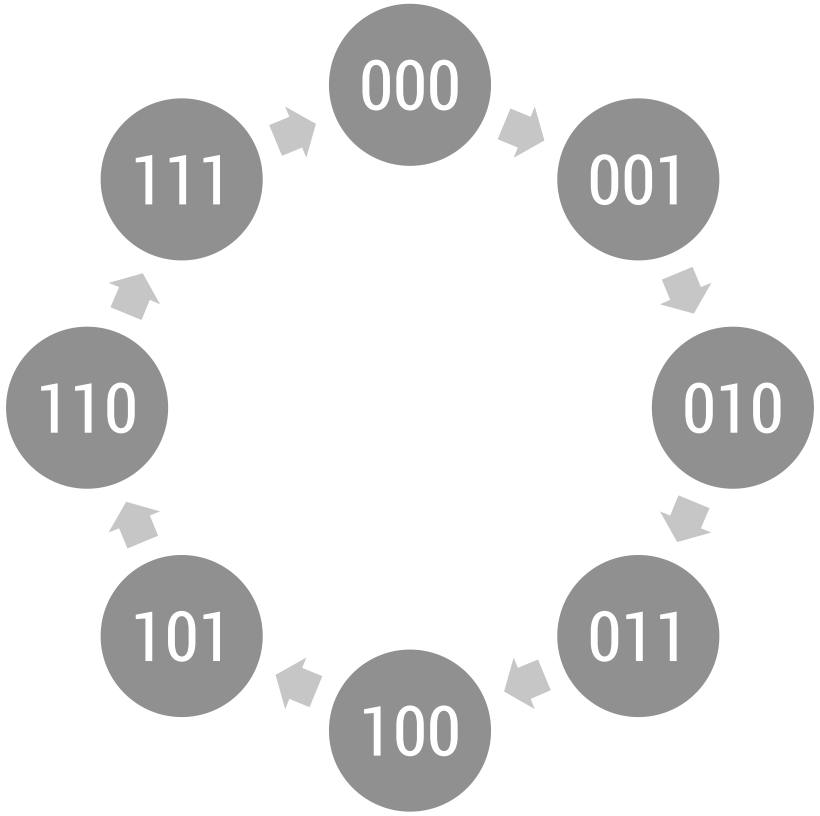
- **Step 1 - Number of flip-flops**: Based on the description of the problem, determine the required number n of the FFs - the smallest value of n is such that the number of states $N \leq 2^n$ and the desired counting sequence.
- **Step 2 - State diagram**: Draw the state diagram showing all the possible states.
- **Step 3 - Choice of flip-flops and excitation table:** Select the type of flip-flops to be used and write the excitation table.
- **Step 4 - Minimal expressions for excitations:** K-maps for the excitations of the flip-flops in terms of the present states and inputs.
- **Step 5 - Logic Diagram**: Draw the logic diagram based on the minimal expressions.

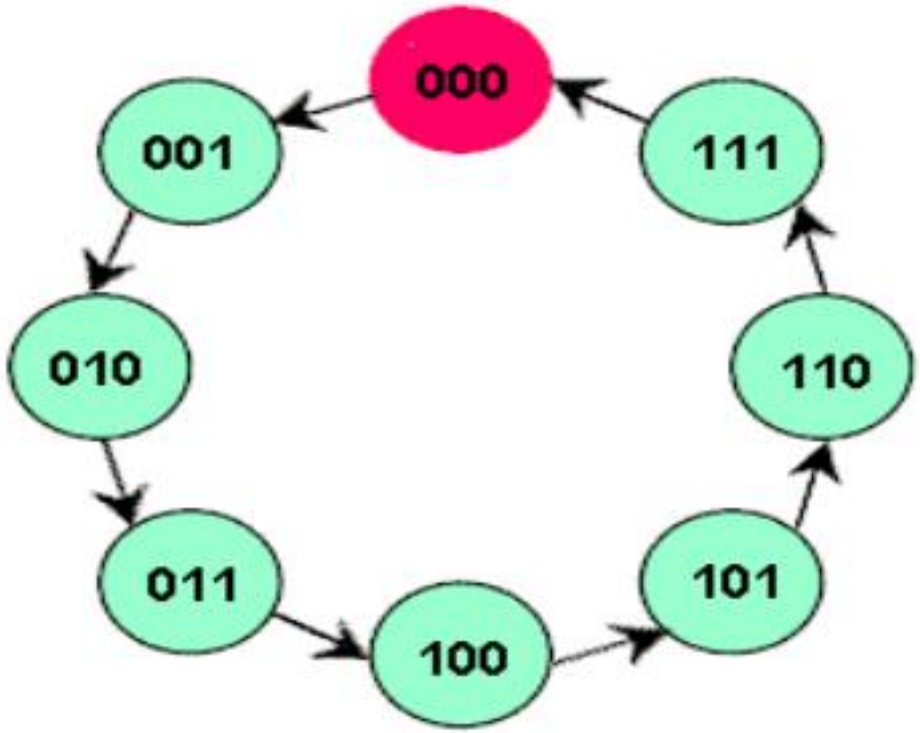
Design of Synchronous 3-bit Up Counters

- Step 1 - Number of flip-flops:

  A 3-bit up-counter requires 3 flip-flops. The counting sequence is 000, 001, 010, 011, 100, 101, 110, 111, 000 …

- Step 2 - Draw the state diagram:





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Clk

Design of Synchronous 3-bit Up Counters

- Step 3 - Select the type of flip-flops and draw the excitation table:

  JK flip-flops are selected and the excitation table of a 3-bit up-counter using J-K flip-flops is drawn as shown below.

PS			NS			Required excitations					
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	J_3	K_3	J_2	K_2	J_1	K_1
0	0	0	0	0	1						
0	0	1	0	1	0						
0	1	0	0	1	1						
0	1	1	1	0	0						
1	0	0	1	0	1						
1	0	1	1	1	0						
1	1	0	1	1	1						
1	1	1	0	0	0						

J-K FF Excitation Table

PS	NS	Required inputs	
Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Design of Synchronous 3-bit Up Counters

- Step 4 - Obtain the minimal expressions:

From excitation table, $J_1 = K_1 = 1$.

K – Maps for excitations J_3, K_3, J_2 and K_2 and their minimized form are as follows:

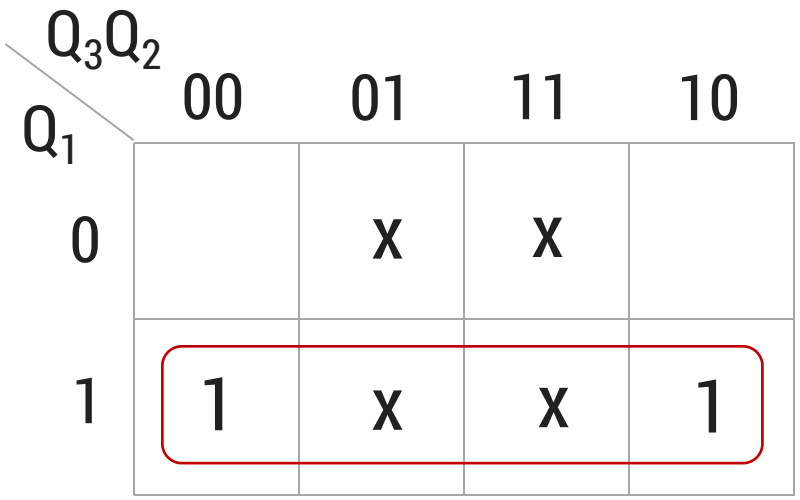
Q_1 \ Q_3Q_2	00	01	11	10
0			x	x
1		1	x	x

$J_3 = Q_2Q_1$

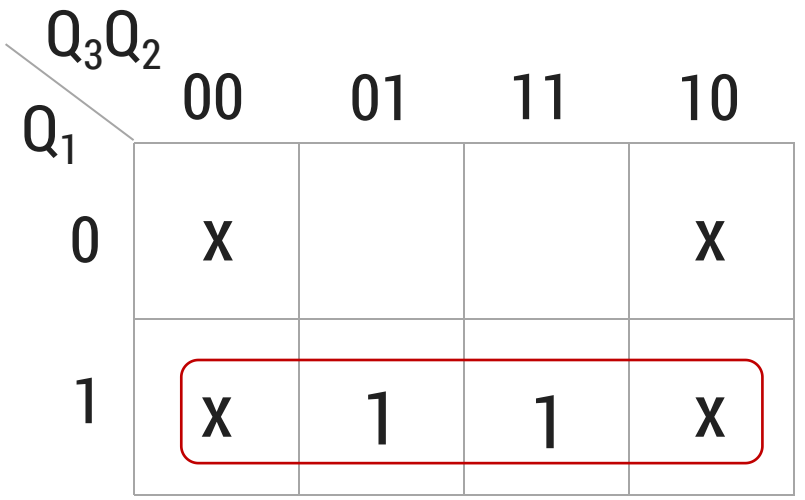
Q_1 \ Q_3Q_2	00	01	11	10
0	x	x		
1	x	x	1	

$K_3 = Q_2Q_1$

Design of Synchronous 3-bit Up Counters



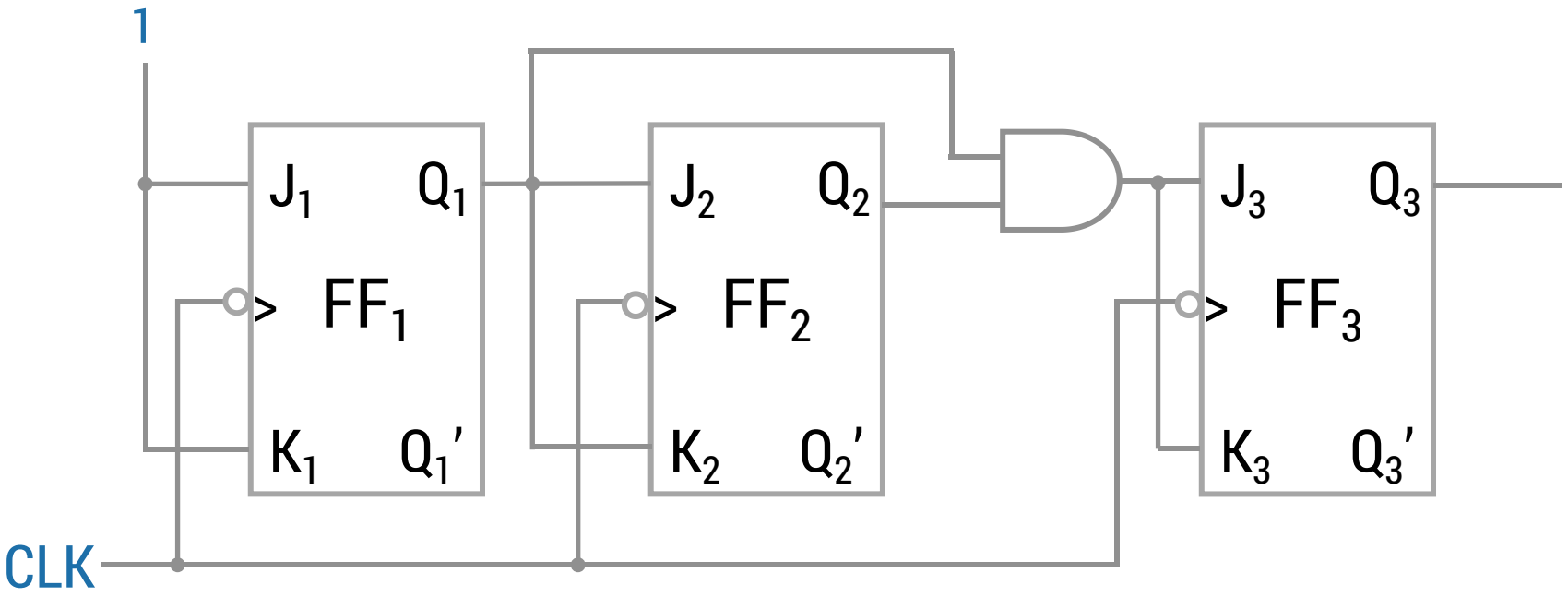
$J_2 = Q_1$



$K_2 = Q_1$

Design of Synchronous 3-bit Up Counters

- Step 5 - Draw the logic diagram:



Designing Counters with Arbitrary Sequences

ALL BELOW LINK WILL BE USEFUL TO UNDERSTAND THE TOPIC SO GO THROUGH ALL VIDEOS.

- https://www.youtube.com/watch?v=Zce6NlHuvfs
- https://www.youtube.com/watch?v=vx4PNd_Hl8U
- https://www.youtube.com/watch?v=ruxiO77HL9k

Decade and BCD Counters

- that goes through 10 unique output combinations and then resets as the clock proceeds further.
- MOD-10 counter.
- 4 flip-flops.
- From 16 states any of the six states by using some kind of feedback is skipped.
- A decade counter does not necessarily count from 0000 to 1001.
- It could even count as 0000, 0001, 0010, 0101, 0110, 1001, 1010, 1100, 1101, 1111, 0000.
- *BCD counter* is a special case of a decade counter.
- Counts from 0000 to 1001 and then resets.

State Table for BCD Counter

Present State				Next State				Output	Flip-Flop inputs			
Q8	Q4	Q2	Q1	Q8	Q4	Q2	Q1	Y	TQ8	TQ4	TQ2	TQ1
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	0	1

- The flip flop input equations can be simplified by means of maps. The simplified functions are
  - $T_{Q1}=1$
  - $T_{Q2}=Q_8'Q_1$
  - $T_{Q4}=Q_2Q_1$
  - $T_{Q8}=Q_8Q_1+Q_4Q_2Q_1$
  - $y=Q_8Q_1$
- The circuit can be easily drawn with four T flip-flops, five AND gates, and one OR gate.

BCD COUNTER

- DRAW YOUR LOGIC DIAGRAM HERE FROM FOUND BOOLEN EQUATION FROM PREVIOUS SLIDE.

Ring Counter- Shift Register Counters

- **Ring counter is an application of Shift resister.**

- **Types of Ring Counter –**

  1. **Straight Ring Counter** 2. **Twisted Ring Counter**

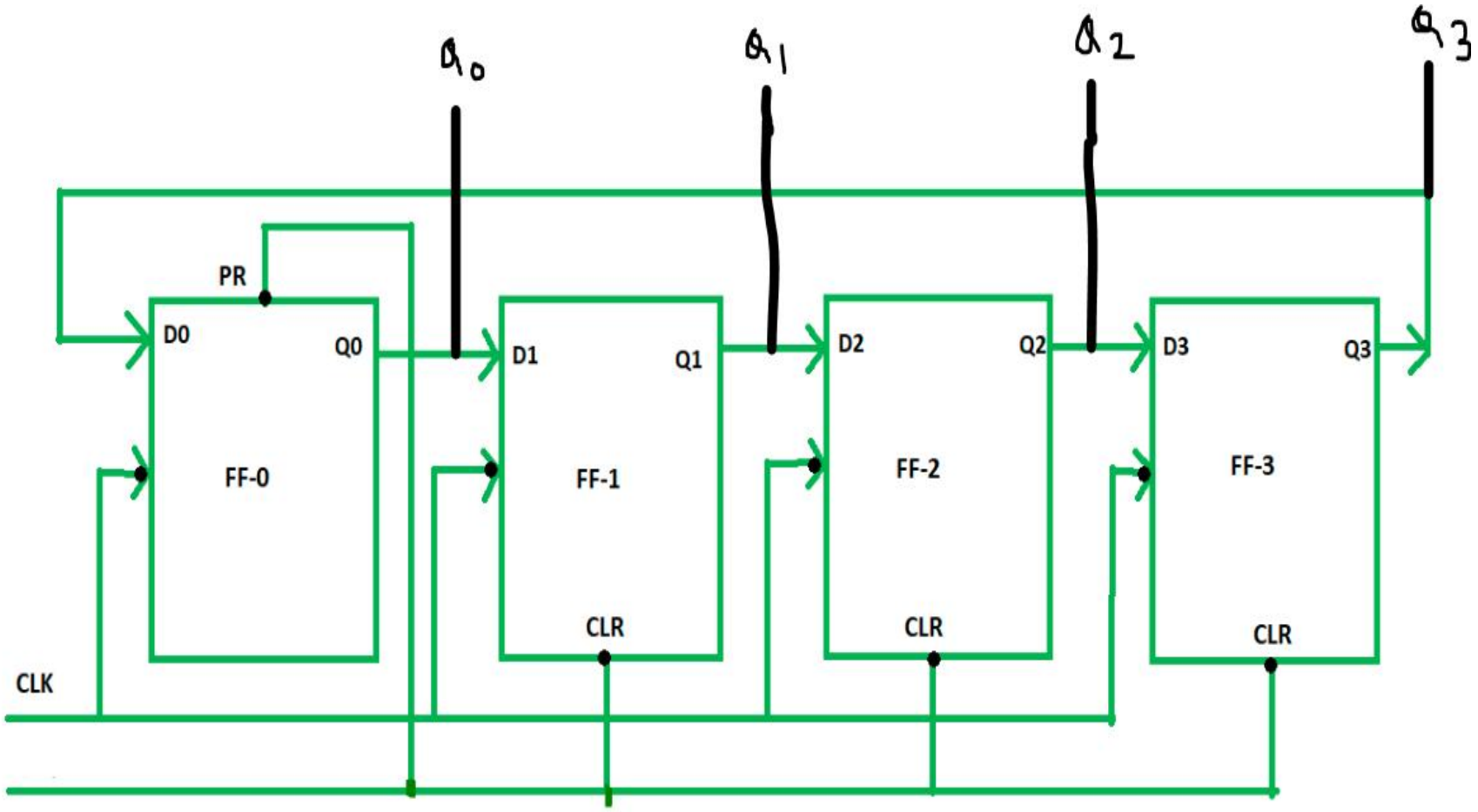
4-bit Ring counter with 4 D flip-flop.

- Straight Ring Counter: One hot Counter : Last flip-flop is connected to the input of the first flip-flop.

- Clock pulse (CLK) is applied to all the flip-flop simultaneously. Therefore, it is a Synchronous Counter.

- No of state = No of bits.

4-bit Ring counter with 4 D flip-flop.

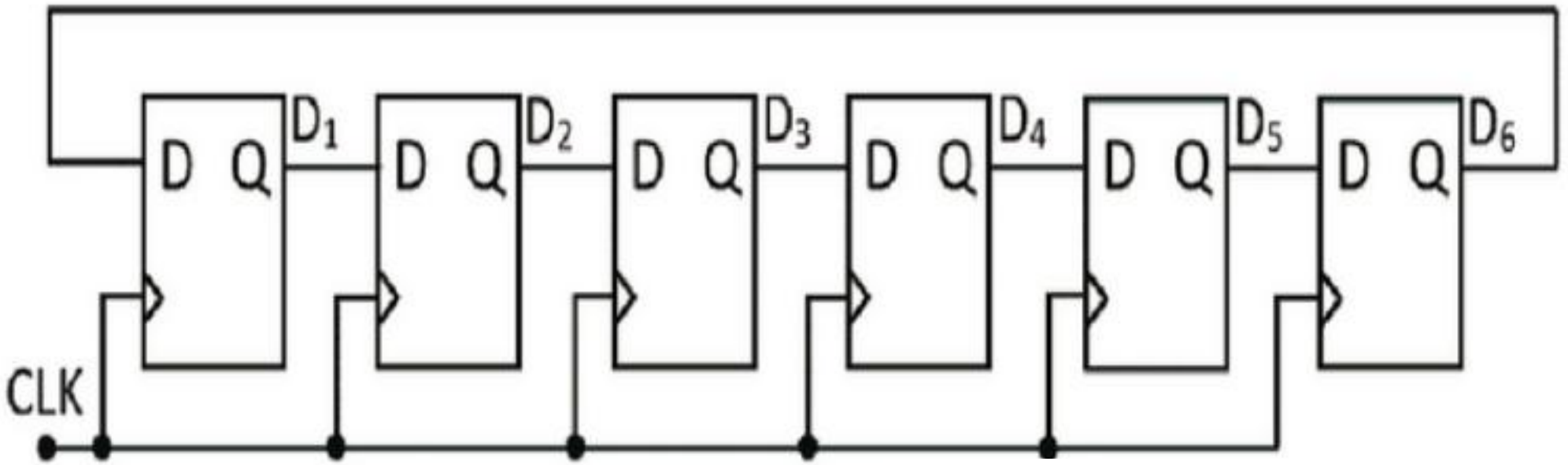


Ring Counter

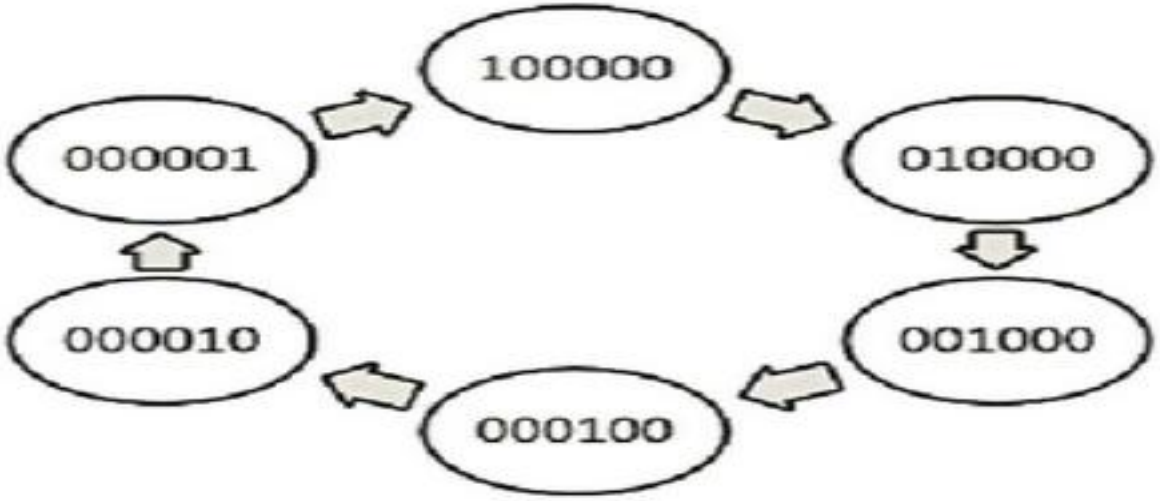
Straight ring counter				
State	Q0	Q1	Q2	Q3
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1

To write about ring counter refer below link
https://www.geeksforgeeks.org/ring-counter-in-digital-logic/?ref=lbp

6-bit Ring counter with 6 D flip-flop.



CLK	D_1	D_2	D_3	D_4	D_5	D_6
1	1	0	0	0	0	0
2	0	1	0	0	0	0
3	0	0	1	0	0	0
4	0	0	0	1	0	0
5	0	0	0	0	1	0
6	0	0	0	0	0	1

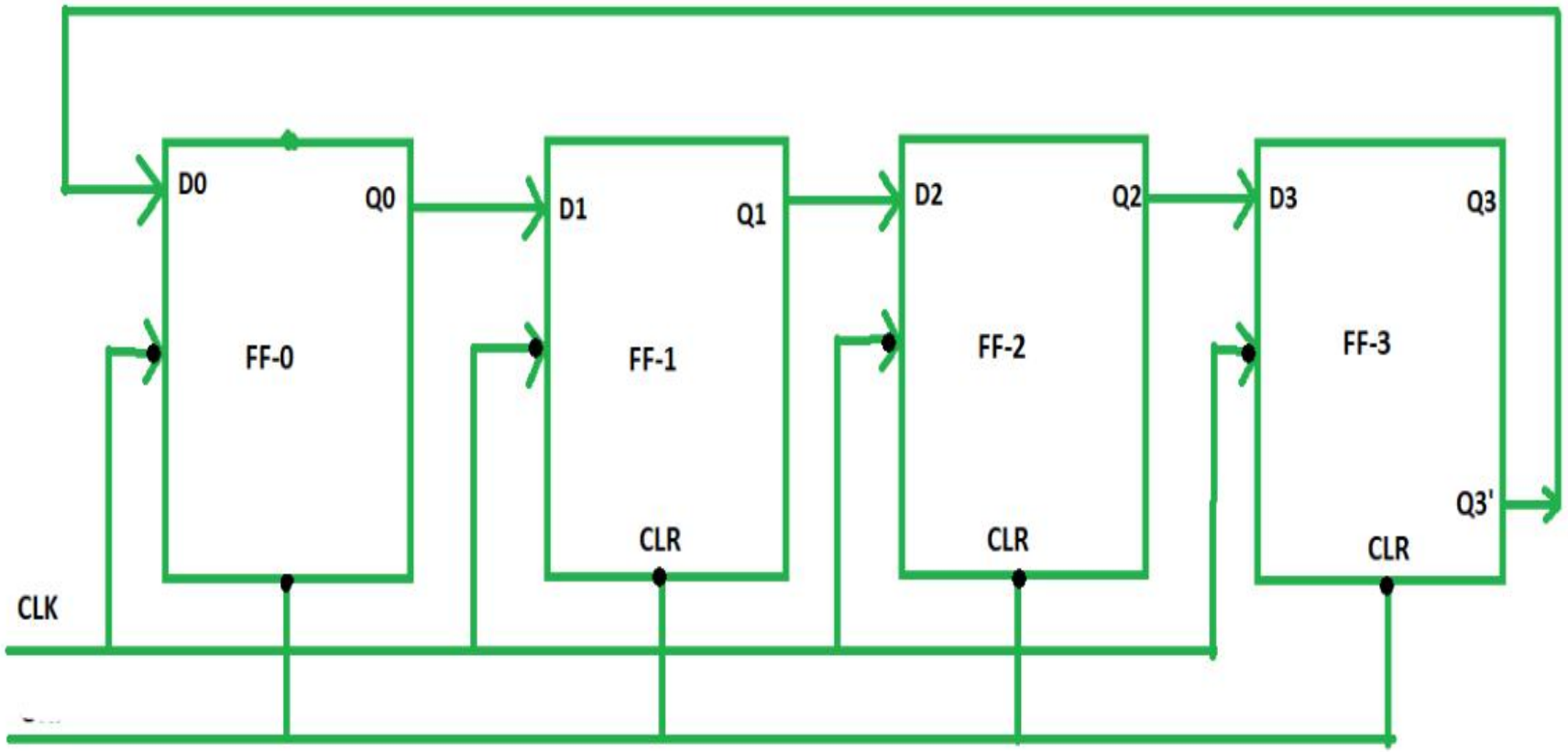


https://www.researchgate.net/figure/State-diagram-and-implementation-of-a-six-bit-ring-counter-with-D-Flip-flops_fig2_322106955

4 bit Twisted Ring Counter

- **Twisted Ring Counter : switch-tail ring counter, walking ring counter or Johnson counter.:**
- connects the **complement** of the output of the last FF to the input of the first FF.
- **No state = 2* No of bits.**

4 bit Twisted Ring Counter



Twisted Ring Counter

Johnson counter				
State	Q0	Q1	Q2	Q3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
0	0	0	0	0

To write about advantage ,dis- advantage ,application and working of this counter refer below link
https://www.geeksforgeeks.org/n-bit-johnson-counter-in-digital-logic/?ref=lbp