(1) How to compile and execute your program; (You can use screenshot to explain)

```
[110521086@eda359_forclass ~/PA1]$
[110521086@eda359_forclass ~/PA1]$ g++ -std=c++11 110521086_PA1.cpp -o testA
[110521086@eda359_forclass ~/PA1]$ ./testA c6288.isc c6288.v
--------DONE--------

Time_All:    13s
Time_Main:    13.61s

sh: pause: command not found
[110521086@eda359_forclass ~/PA1]$ source /usr/cad/cadence/CIC/incisiv.cshrc
[110521086@eda359_forclass ~/PA1]$ source /usr/cad/synopsys/CIC/verdi.cshrc
[110521086@eda359_forclass ~/PA1]$ ncverilog +access+r c6288.v c6288_testbench.v
```

g++ ：編譯 c++檔案

-std = c++11：設定編譯版本為 c++11

110521086_PA1.cpp：要編譯的檔案

-o ：輸出檔案

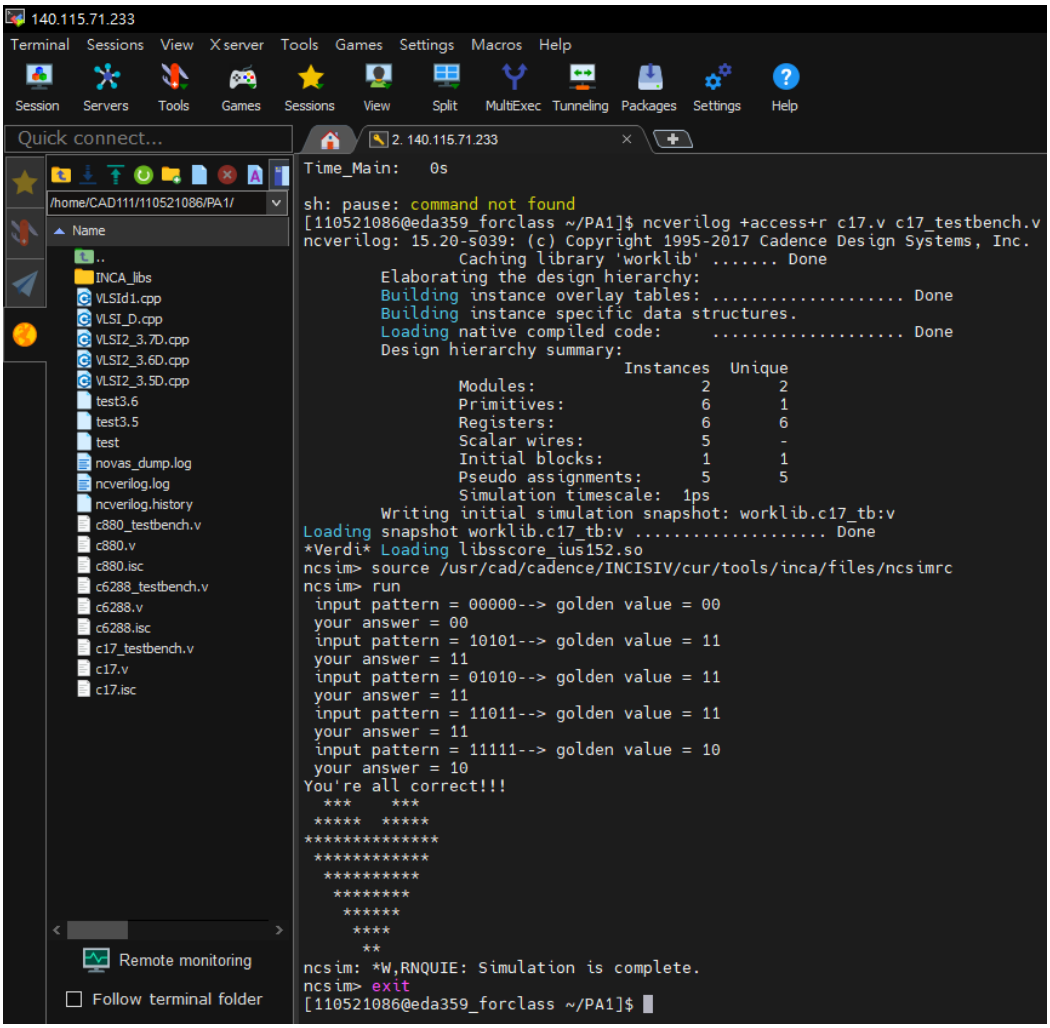
testA：輸出檔檔名

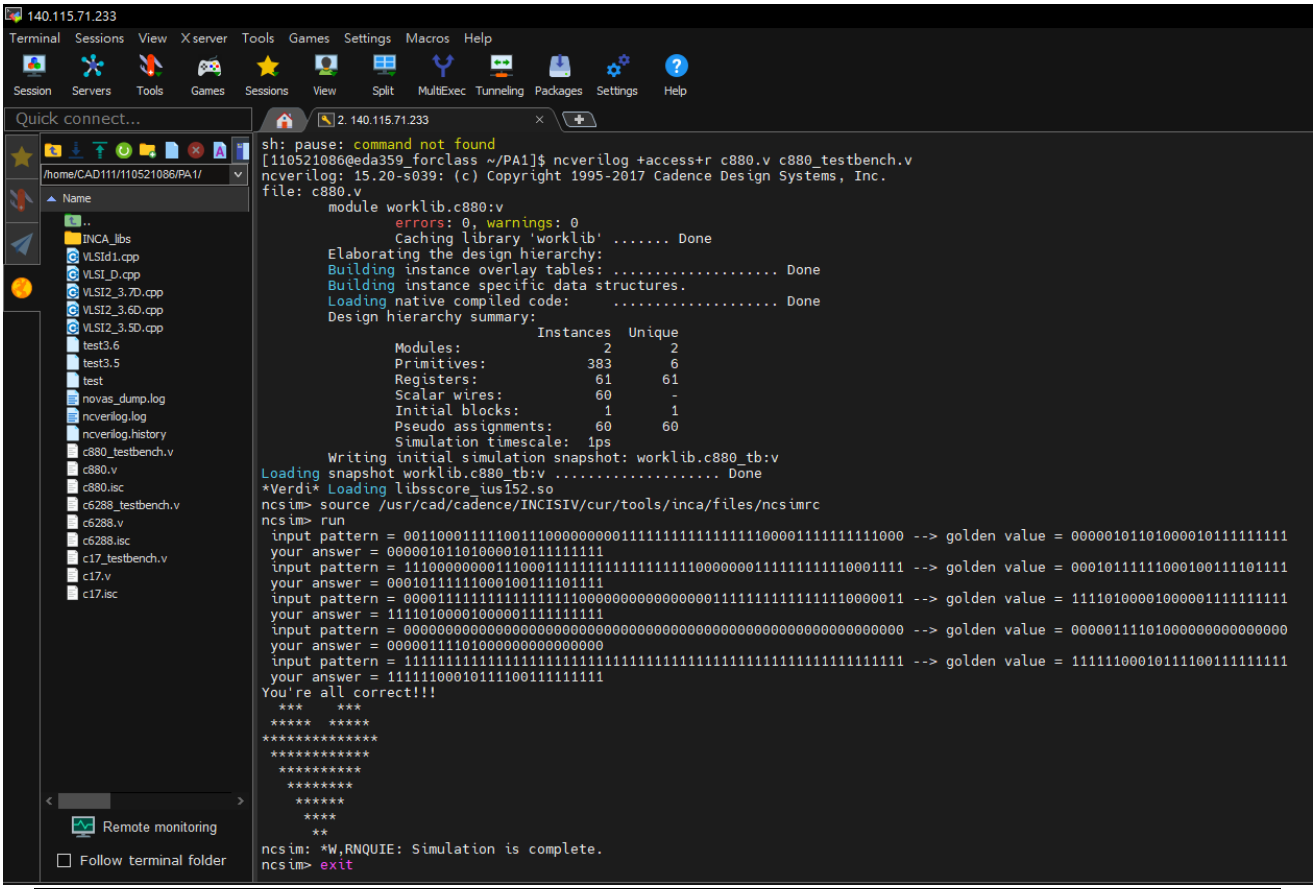
./testA：執行檔案

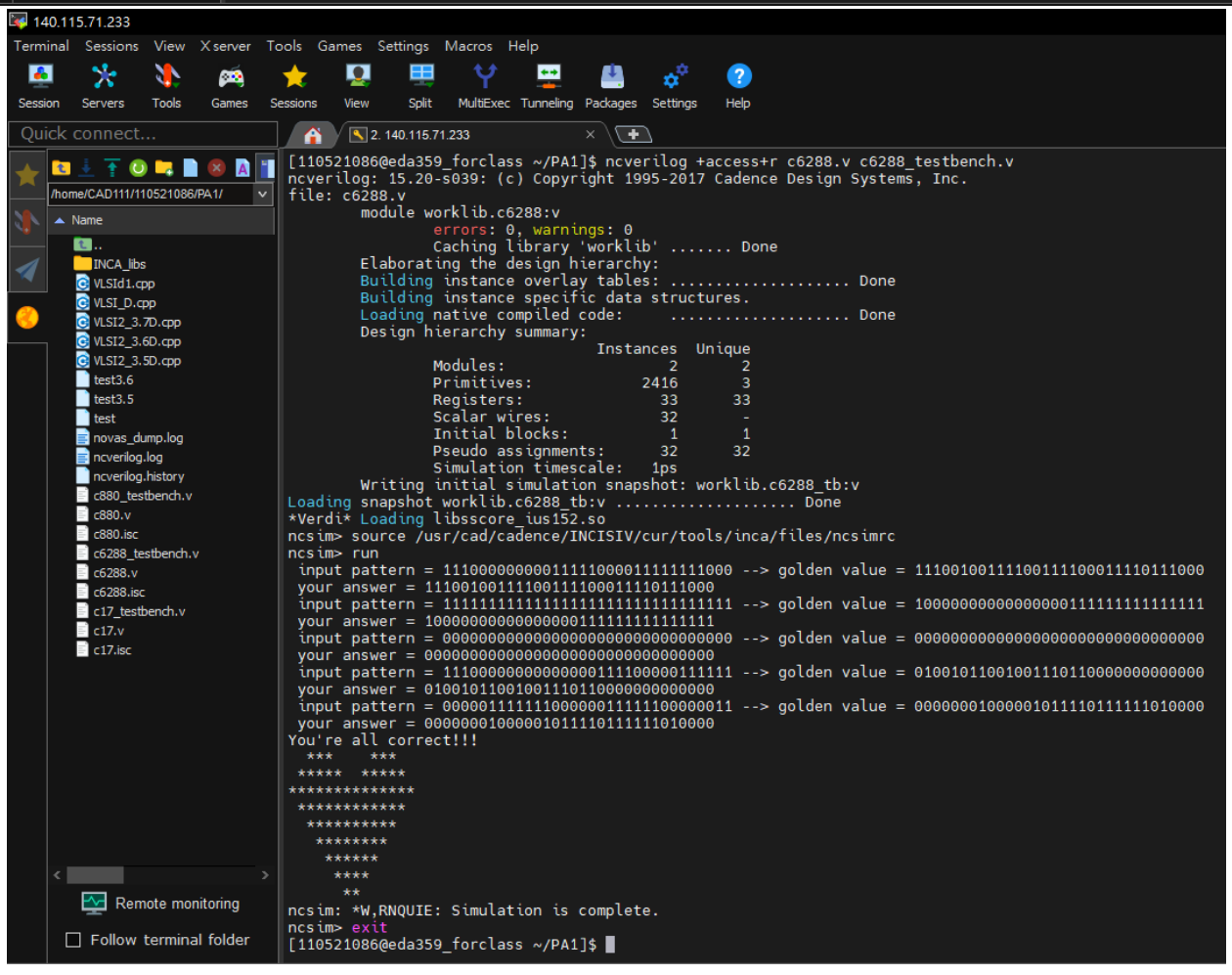
c6288.isc：testA 之輸入檔

c6288.v ：testA 之輸出檔

(2) The completion of the assignment; (If you complete all requirements, just specify all)




140.115.71.233
Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
2. 140.115.71.233
/home/CAD111/110521086/PA1/
Name
INCA_libs
VLSId1.cpp
VLSI_D.cpp
VLSI2_3.7D.cpp
VLSI2_3.6D.cpp
VLSI2_3.5D.cpp
test3.6
test3.5
test
novas_dump.log
ncverilog.log
ncverilog.history
c880_testbench.v
c880.v
c880.isc
c6288_testbench.v
c6288.v
c6288.isc
c17_testbench.v
c17.v
c17.isc
Remote monitoring
Follow terminal folder
sh: pause: command not found
[110521086@eda359_forclass ~/PA1]$ ncverilog +access+r c880.v c880_testbench.v
ncverilog: 15.20-s039: (c) Copyright 1995-2017 Cadence Design Systems, Inc.
file: c880.v
module worklib.c880:v
errors: 0, warnings: 0
Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
Building instance overlay tables: ..... Done
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
Instances Unique
Modules: 2 2
Primitives: 383 6
Registers: 61 61
Scalar wires: 60 -
Initial blocks: 1 1
Pseudo assignments: 60 60
Simulation timescale: 1ps
Writing initial simulation snapshot: worklib.c880_tb:v
Loading snapshot worklib.c880_tb:v ..... Done
Verdi Loading libsscore_ius152.so
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
input pattern = 0011000111110011000000000111111111111111111000011111111111000 --> golden value = 0000010110100001011111111
your answer = 0000010110100001011111111
input pattern = 1110000000011100011111111111111111100000001111111111001111 --> golden value = 0001011111100010011101111
your answer = 0001011111100010011101111
input pattern = 0000111111111111111100000000000000001111111111111110000011 --> golden value = 1111010000100000111111111
your answer = 1111010000100000111111111
input pattern = 0000000000000000000000000000000000000000000000000000000000 --> golden value = 0000011110100000000000000
your answer = 0000011110100000000000000
input pattern = 1111111111111111111111111111111111111111111111111111111111 --> golden value = 1111110001011100111111111
your answer = 1111110001011100111111111
You're all correct!!!
ncsim: *W,RNQUIE: Simulation is complete.
ncsim> exit


140.115.71.233
Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
2. 140.115.71.233
/home/CAD111/110521086/PA1/
Name
INCA_libs
VLSId1.cpp
VLSI_D.cpp
VLSI2_3.7D.cpp
VLSI2_3.6D.cpp
VLSI2_3.5D.cpp
test3.6
test3.5
test
novas_dump.log
ncverilog.log
ncverilog.history
c880_testbench.v
c880.v
c880.isc
c6288_testbench.v
c6288.v
c6288.isc
c17_testbench.v
c17.v
c17.isc
Remote monitoring
Follow terminal folder
[110521086@eda359_forclass ~/PA1]$ ncverilog +access+r c6288.v c6288_testbench.v
ncverilog: 15.20-s039: (c) Copyright 1995-2017 Cadence Design Systems, Inc.
file: c6288.v
module worklib.c6288:v
errors: 0, warnings: 0
Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
Building instance overlay tables: ..... Done
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
Instances Unique
Modules: 2 2
Primitives: 2416 3
Registers: 33 33
Scalar wires: 32 -
Initial blocks: 1 1
Pseudo assignments: 32 32
Simulation timescale: 1ps
Writing initial simulation snapshot: worklib.c6288_tb:v
Loading snapshot worklib.c6288_tb:v ..... Done
Verdi Loading libsscore_ius152.so
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
input pattern = 1110000000001111100001111111000 --> golden value = 1110010011110011110001111011000
your answer = 1110010011110011110001111011000
input pattern = 1111111111111111111111111111111 --> golden value = 1000000000000000011111111111111
your answer = 1000000000000000011111111111111
input pattern = 0000000000000000000000000000000 --> golden value = 0000000000000000000000000000000
your answer = 0000000000000000000000000000000
input pattern = 1110000000000000011100000111111 --> golden value = 0100101100100111011000000000000
your answer = 0100101100100111011000000000000
input pattern = 0000011111110000001111110000011 --> golden value = 0000000100000101111011111010000
your answer = 0000000100000101111011111010000
You're all correct!!!
ncsim: *W,RNQUIE: Simulation is complete.
ncsim> exit
[110521086@eda359_forclass ~/PA1]$

(3) The hardness of this assignment and how you overcome it;

我認為最困難的地方在於將分支線(邏輯閘輸入)重新整理為原來的輸出，我想了很多方式去寫，但都無法改善。後來好不容易寫好，在伺服器上編譯又發現問題，原本 c17 的指向方式，我是尋找 “fan from” 的方式，去找到分支線的源頭，但 c880 並沒有 “fan from"，所以只好重新更換了一種方式，將分支指向正確的源頭，所以我又更換了一種方式，指向正確的數值。再次編譯又發現有些應該要顯示 “gat_out” 會只有顯示 “gat”；更改後又發現有應該要顯示 “gat” 會只有顯示 “gat_out”

解決方式：

發現是 wire_c1~ wire_c8 在每次結束 if 函式時會被我刷新，導致進入 logic_wire 函式後，排除 input gat 的部分無法正常運行。因此重新定義一個全域變數 wire_c 取代 wire_c1~ wire_c8，便可正常運行。（見下圖）

```
//-------------------------------------------------//wire跟out統一成陣列，之後放進for loop
        int ar_wire[8] = {wire01,wire02,wire03,wire04,wire05,wire06,wire07,wire08};
        int ar_out[8] = {outputnum01,outputnum02,outputnum03,outputnum04,outputnum05,outputnum06,outputnum07,outputnum08};
        string ar_logic[8] = {"and gat","nand gat","or gat","nor gat","not gat","buf gat","xor gat","xnor gat"};

//-------------------------------------------------//符合條件者進行處理分支
        if (wire01 == 11){
            col1 = col +1;
            string wire441 = numc(wire01,s);
            wire_c += wire441 +",";
            mat5 = logic_wire(impt, col1,wire_c,mat5,s);
        }
        if (wire02 == 11){
            col2 = col +1;
            string wire442 = numc(wire02,s);
            wire_c += wire442 +",";
            mat5 = logic_wire(impt,col2,wire_c,mat5,s);
        }
        if (wire03 == 11){
            col3 = col +1;
            string wire443 = numc(wire03,s);
            wire_c += wire443 +",";
            mat5 = logic_wire(impt,col3,wire_c,mat5,s);
```

(4) Any suggestions about this programming assignment?

很感謝助教協助回答我們的問題，很多跟我一起修的同學們都受到「小企鵝」問題所苦惱，感謝助教幫我們解決問題；另外，我覺得這個作業真的有難度，有時候都要寫到很晚才能睡覺。

給自己的建議：別在截止日期剩 2 個禮拜的時候才開始趕作業