AIB CHIPLET INTERFACE SPECIFICATION PREVIEW

October 2018

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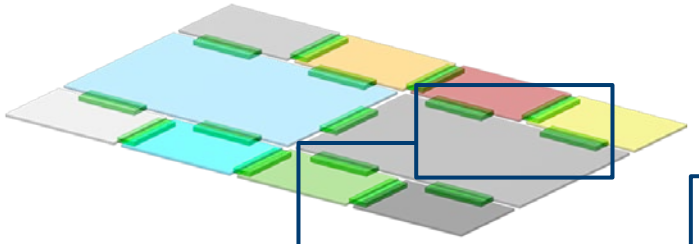
AIB Specification Preview

As the specification completes editing for release, this document serves as a preview of important AIB features, form and capability. Further, this presentation further provides exemplary implementations of the AIB specification.

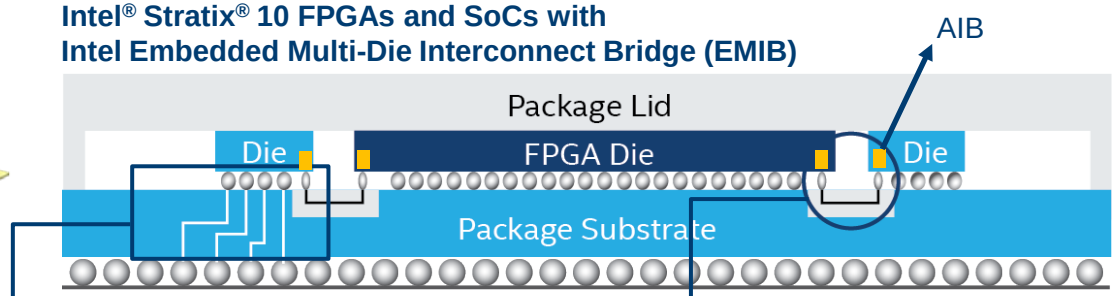
AIB Over High-Density Packaging

As a wide parallel interface, AIB is well suited for high-density packaging



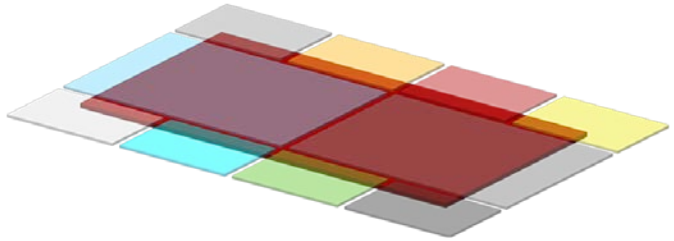
Multiple bridges possible

Intel® Stratix® 10 FPGAs and SoCs with Intel Embedded Multi-Die Interconnect Bridge (EMIB)

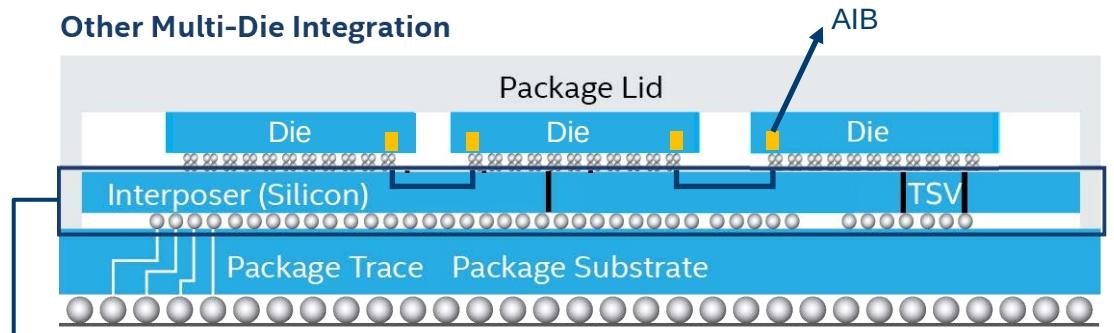


The rest of the package: RF, other I/Os, and power are unaffected

Localized high-density die-to-die interconnect

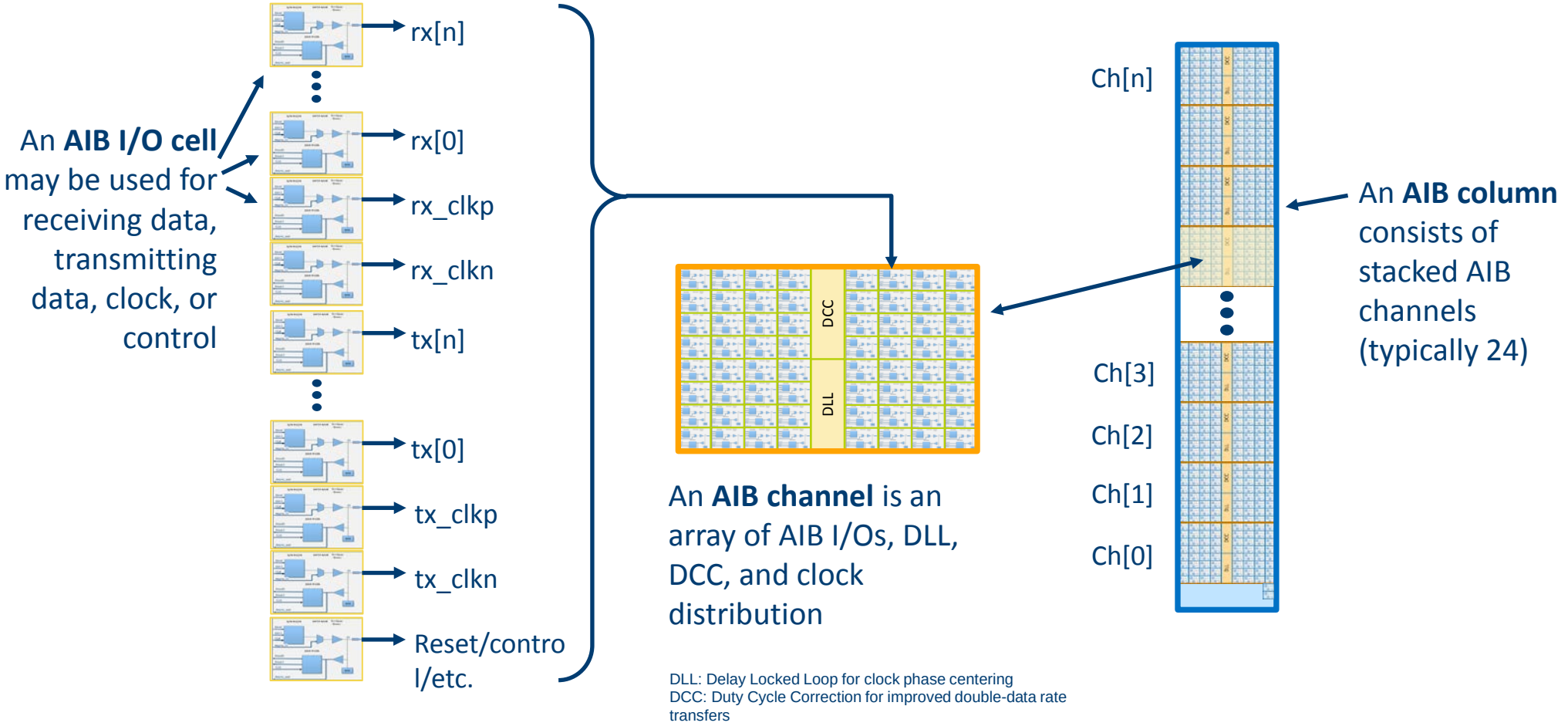


Other Multi-Die Integration



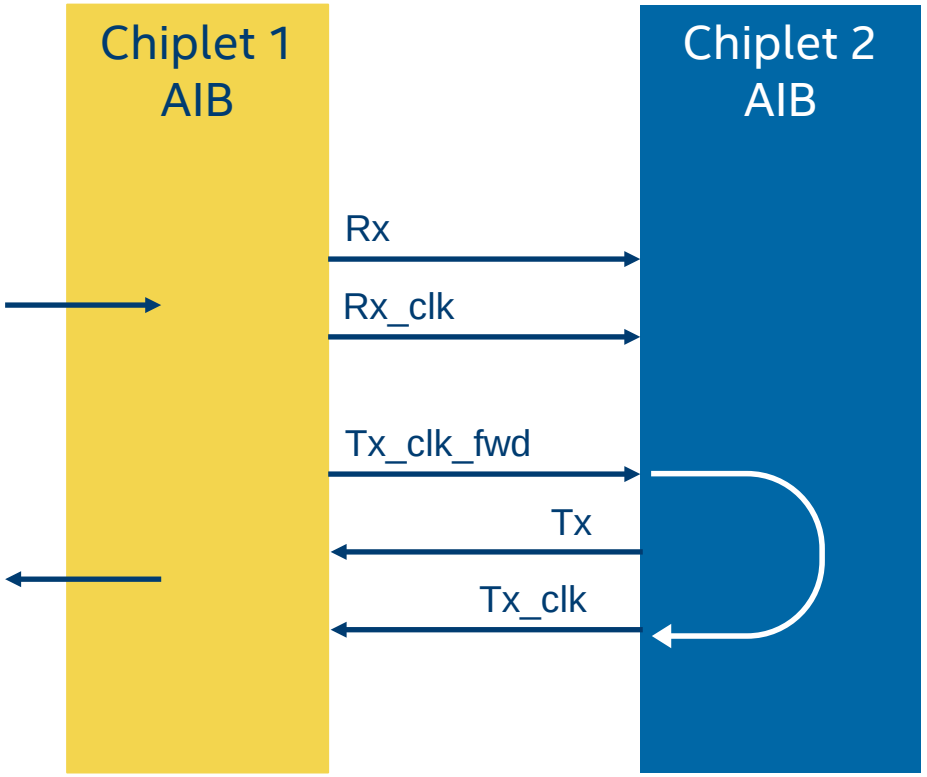
All signals will travel through the Interposer, including RF signals

AIB I/O Cell, Channel, and Column



DLL: Delay Locked Loop for clock phase centering
DCC: Duty Cycle Correction for improved double-data rate transfers

Typical AIB Clocking Configuration (One Channel)



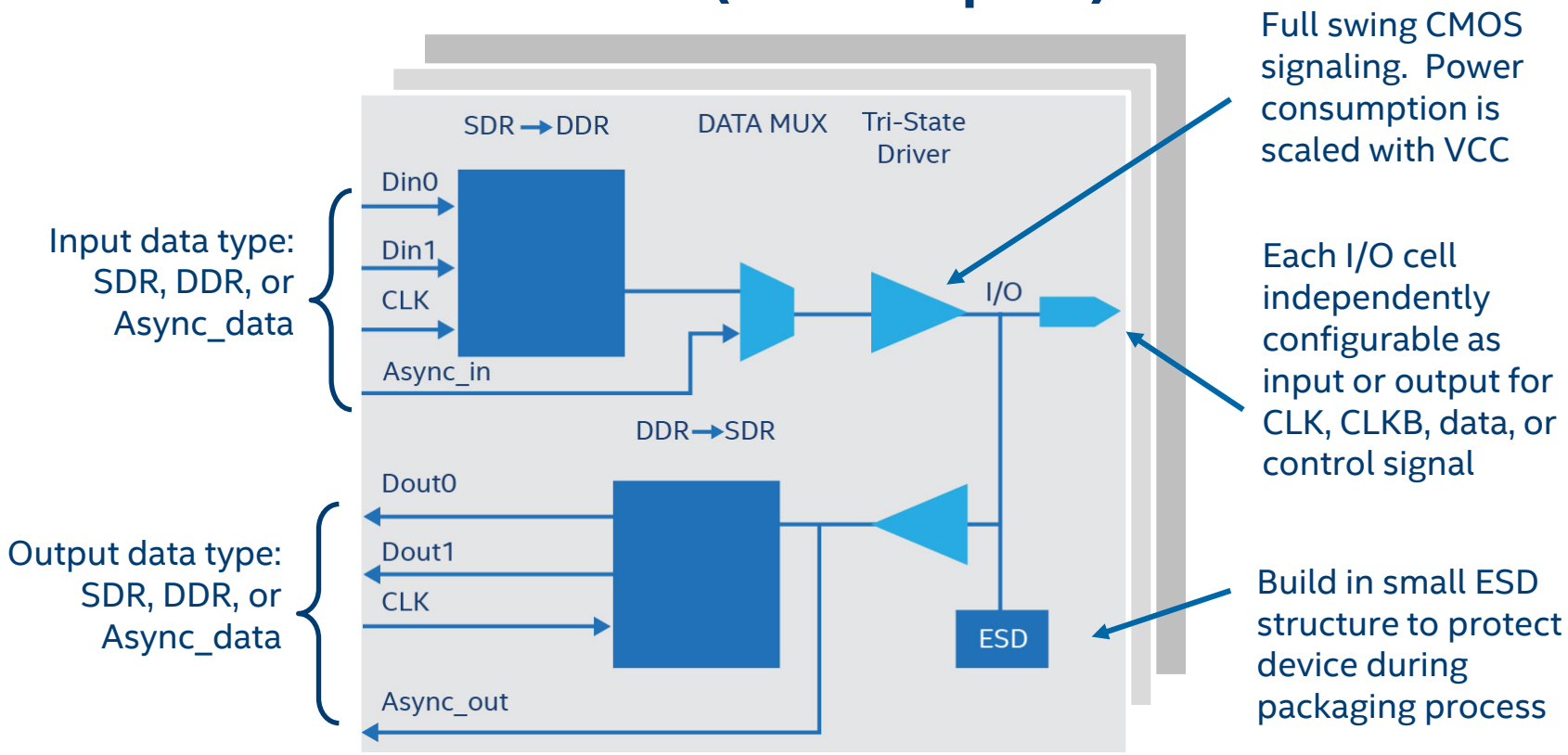
AIB Base and Plus Configurations

AIB Configuration	Data Rate	I/O	High Level Description
AIB Base	1Gbps	SDR	AIB I/O
AIB Plus	2Gbps	SDR/DDR	AIB I/O and AIB Adapter

Signal Class	Single/Differential ended signal	Sync/Async	Typical Usage
Clock	DE using 2 SE lines	Synchronous (DDR/SDR)	• RX/TX transfer clock
Data	SE	Synchronous (DDR/SDR)	• RX/TX transfer data
Side Band Control	SE	Synchronous (SDR time multiplexed)	• Status, (DLL/DCC) lock signals • Calibration status
	SE	Asynchronous	• Reset, Power-on-Reset

For AIB Plus, an AIB Adapter (retiming register, reset controller and sideband control TX/RX) is layered on top of AIB I/O to ease clock domain transfer requirements and provide control functions

AIB I/O Basic Structure (Example)



I/O cells are grouped to form an AIB channel, multiple AIB channels are stacked in a column

I/Os are statically assigned input or output, so a fixed input or output design that meets AIB signaling specs can be compliant. I/Os need to meet testability which requires a loopback path at the pin.

AIB Master and Slave

Master side provides sideband clock, Slave controls power-on-reset

A dual-mode chiplet can be configured to Master or Slave

Area	AIB Master & Slave Differences
Power-on-Reset (POR) and Device_detect bumps	POR is output from Slave to Master Device_detect is output from Master to Slave, “I am here”)
Free running clock source	Master provides always-on (free running clock) to Slave
Sideband control signal register	Different sideband control register length
Reset and calibration state machine	Different requirements for master vs. slave device during power-on-reset.

AIB Data per Channel

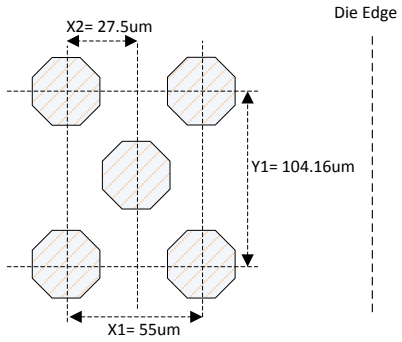
AIB Generation	AIB Configuration	Data/channel	Control Signals	Clock	Async Signals	Data Rates	Gbps/mm	Energy (pJ/bit)	
AIB-GEN1 – 55 um	AIB Base	40 up to 160 in increments of 40	-	4	4	2	1,000	1	55 um Bump Pitch
	AIB Plus		4	12					
AIB-GEN1 – 10 um	AIB Base	40 up to 640 in increments of 40	-	4	4	2 (init)/ 4 (later)	4,000 / 8,000	0.2	Projected 10 um Bump Pitch
	AIB Plus		4	12					

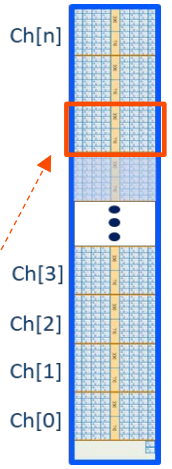
I/O counts in multiples of 40 for compatibility and migratability

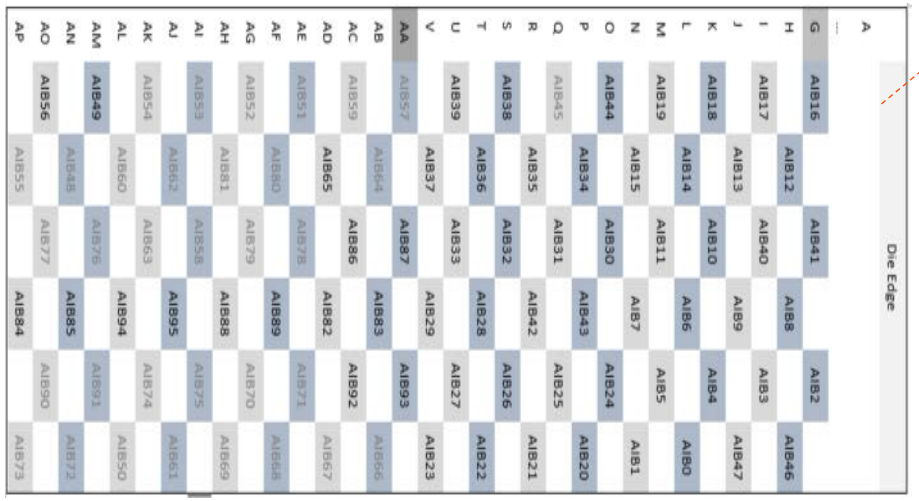
Example total throughput for GEN1-55 maximum AIB column:

- 160 RX/TX/channel x 24 channel x 2 Gbps = 7,680 Gbps/AIB column

AIB Microbump Array (one 55 u channel)





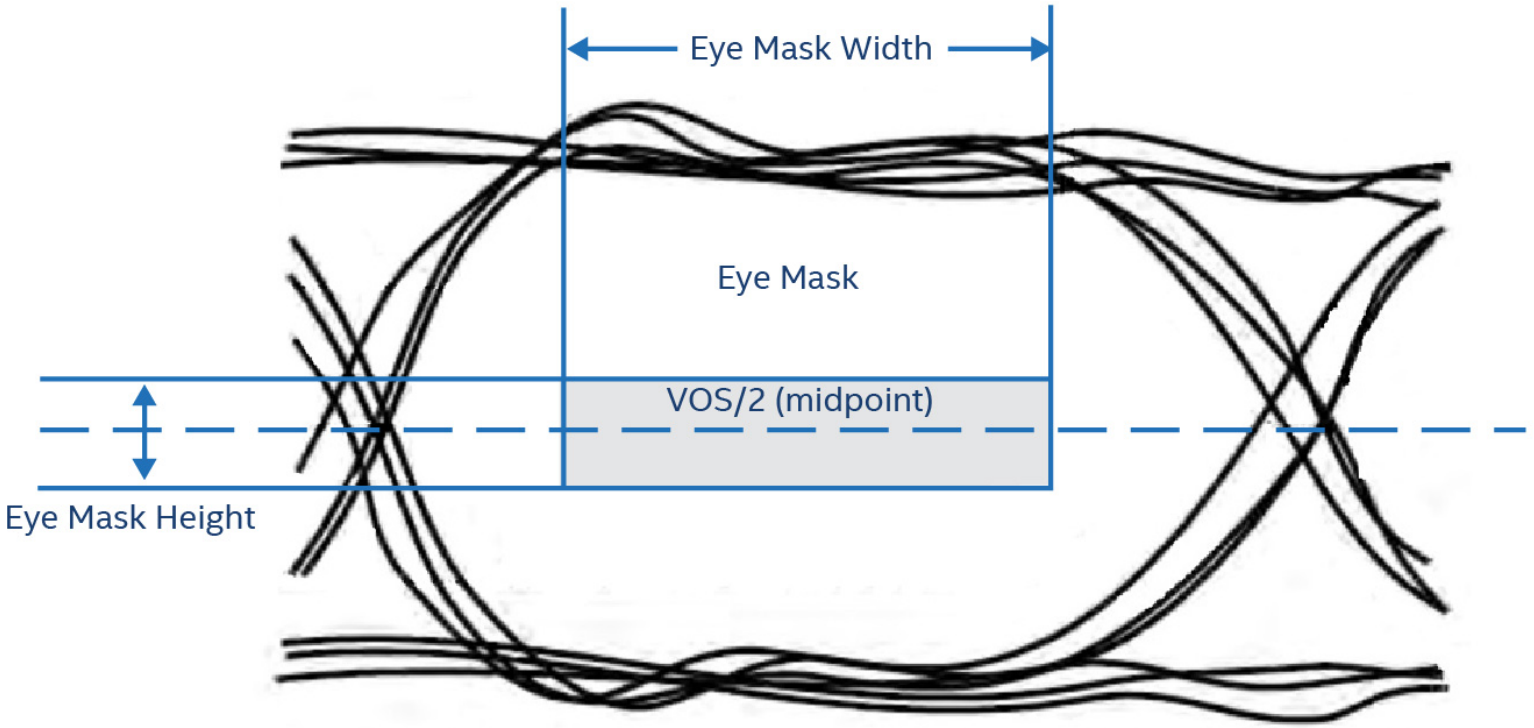


Bump ID	Master Bump Name	IO Type	Function
AIB0	ms_data[0]	out	TX[0]
AIB1	ms_data[1]	out	TX[1]
AIB2	ms_data[2]	out	TX[2]
AIB3	ms_data[3]	out	TX[3]
AIB4	ms_data[4]	out	TX[4]
AIB5	ms_data[5]	out	TX[5]
AIB6	ms_data[6]	out	TX[6]
AIB7	ms_data[7]	out	TX[7]
AIB8	ms_data[8]	out	TX[8]
AIB9	ms_data[9]	out	TX[9]
AIB10	ms_data[10]	out	TX[10]
AIB11	ms_data[11]	out	TX[11]
AIB12	ms_data[12]	out	TX[12]
AIB13	ms_data[13]	out	TX[13]
AIB14	ms_data[14]	out	TX[14]
AIB15	ms_data[15]	out	TX[15]
AIB16	ms_data[16]	out	TX[16]
AIB17	ms_data[17]	out	TX[17]
AIB18	ms_data[18]	out	TX[18]
AIB19	ms_data[19]	out	TX[19]
AIB20	sl_data[0]	in	RX[0]
AIB21	sl_data[1]	in	RX[1]
AIB22	sl_data[2]	in	RX[2]
AIB23	sl_data[3]	in	RX[3]
AIB24	sl_data[4]	in	RX[4]
AIB25	sl_data[5]	in	RX[5]
AIB26	sl_data[6]	in	RX[6]
AIB27	sl_data[7]	in	RX[7]
AIB28	sl_data[8]	in	RX[8]
AIB29	sl_data[9]	in	RX[9]
AIB30	sl_data[10]	in	RX[10]
AIB31	sl_data[11]	in	RX[11]

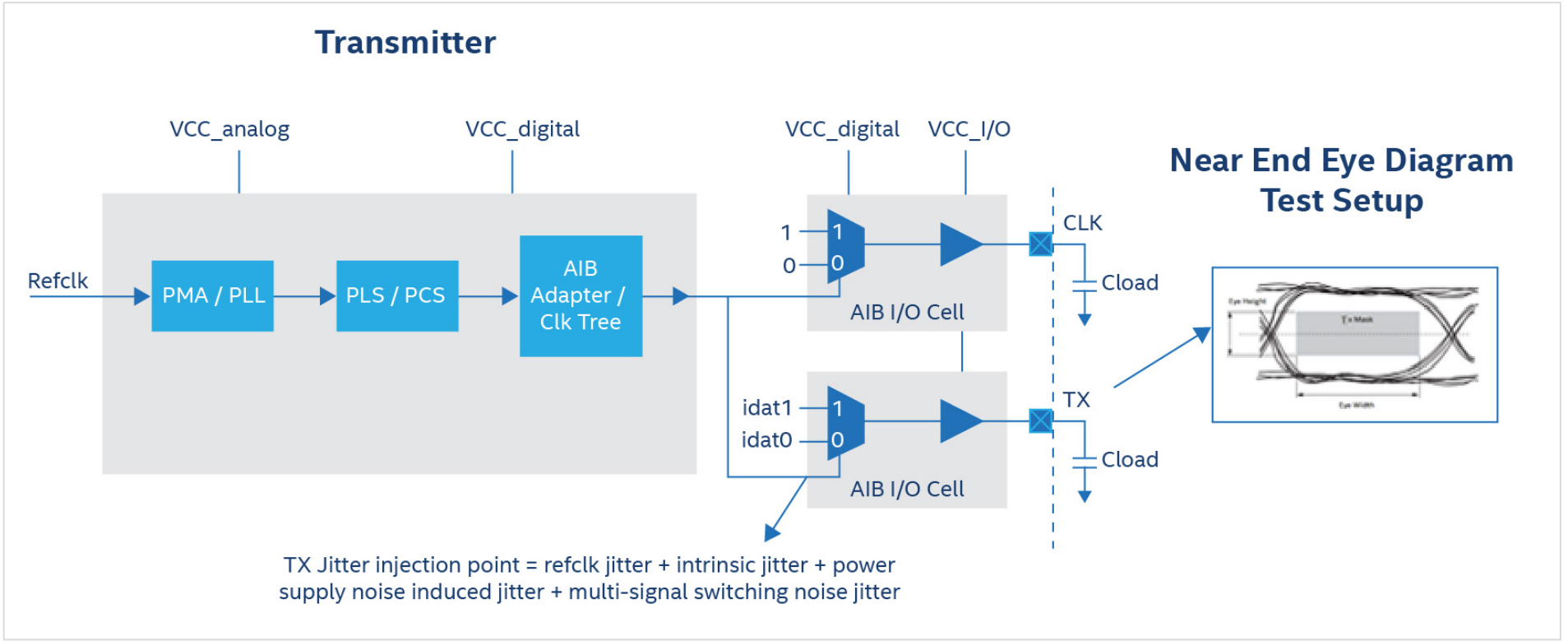
Bump ID	Master Bump Name	IO Type	Function
AIB32	sl_data[12]	in	RX[12]
AIB33	sl_data[13]	in	RX[13]
AIB34	sl_data[14]	in	RX[14]
AIB35	sl_data[15]	in	RX[15]
AIB36	sl_data[16]	in	RX[16]
AIB37	sl_data[17]	in	RX[17]
AIB38	sl_data[18]	in	RX[18]
AIB39	sl_data[19]	in	RX[19]
AIB40	ms_tran_clkb	out	TXCLKB
AIB41	ms_tran_clk	out	TXCLK
AIB42	sl_tran_clkb	in	RXCLKB
AIB43	sl_tran_clk	in	RXCLK
AIB44	sl_rstn	in	RSTN
AIB45	reserved_AIB45	tri	reserved
AIB46	spare[0]	IO	spare[0]
AIB47	spare[1]	IO	spare[1]
AIB48	reserved_AIB48	tri	reserved
AIB49	ms_rstn	out	RSTN
AIB50	reserved_AIB50	tri	reserved
AIB51	reserved_AIB51	tri	reserved
AIB52	reserved_AIB52	tri	reserved
AIB53	reserved_AIB53	tri	reserved
AIB54	reserved_AIB54	tri	reserved
AIB55	reserved_AIB55	tri	reserved
AIB56	ms_adapt_rstn	out	ARSTN
AIB57	reserved_AIB57	tri	reserved
AIB58	reserved_AIB58	tri	reserved
AIB59	reserved_AIB59	tri	reserved
AIB60	reserved_AIB60	tri	reserved
AIB61	reserved_AIB61	tri	reserved
AIB62	reserved_AIB62	tri	reserved
AIB63	reserved_AIB63	tri	reserved

Bump ID	Master Bump Name	IO Type	Function
AIB64	reserved_AIB64	tri	reserved
AIB65	sl_adapter_rstn		ARSTN
AIB66	reserved_AIB66	tri	reserved
AIB67	reserved_AIB67	tri	reserved
AIB68	reserved_AIB68	tri	reserved
AIB69	reserved_AIB69	tri	reserved
AIB70	reserved_AIB70	tri	reserved
AIB71	reserved_AIB71	tri	reserved
AIB72	reserved_AIB72	tri	reserved
AIB73	reserved_AIB73	tri	reserved
AIB74	reserved_AIB74	tri	reserved
AIB75	reserved_AIB75	tri	reserved
AIB76	reserved_AIB76	tri	reserved
AIB77	reserved_AIB77	tri	reserved
AIB78	reserved_AIB78	tri	reserved
AIB79	reserved_AIB79	tri	reserved
AIB80	reserved_AIB80	tri	reserved
AIB81	reserved_AIB81	tri	reserved
AIB82	sl_sr_clkb	in	SRCLKB
AIB83	sr_sl_clk	in	SRCLK
AIB84	sr_ms_clkb	out	STCKB
AIB85	sr_ms_clk	out	STCK
AIB86	ms_clkb	out	RXFCLKB
AIB87	ms_clk	out	RXFCLK
AIB88	reserved_AIB88	tri	reserved
AIB89	reserved_AIB89	tri	reserved
AIB90	reserved_AIB90	tri	reserved
AIB91	reserved_AIB91	tri	reserved
AIB92	sr_sl_load	in	SRL
AIB93	sr_sl_data	in	SRD
AIB94	sr_ms_load	out	STL
AIB95	sr_ms_data	out	STD

AIB Electrical Specification, Eye Mask Definition



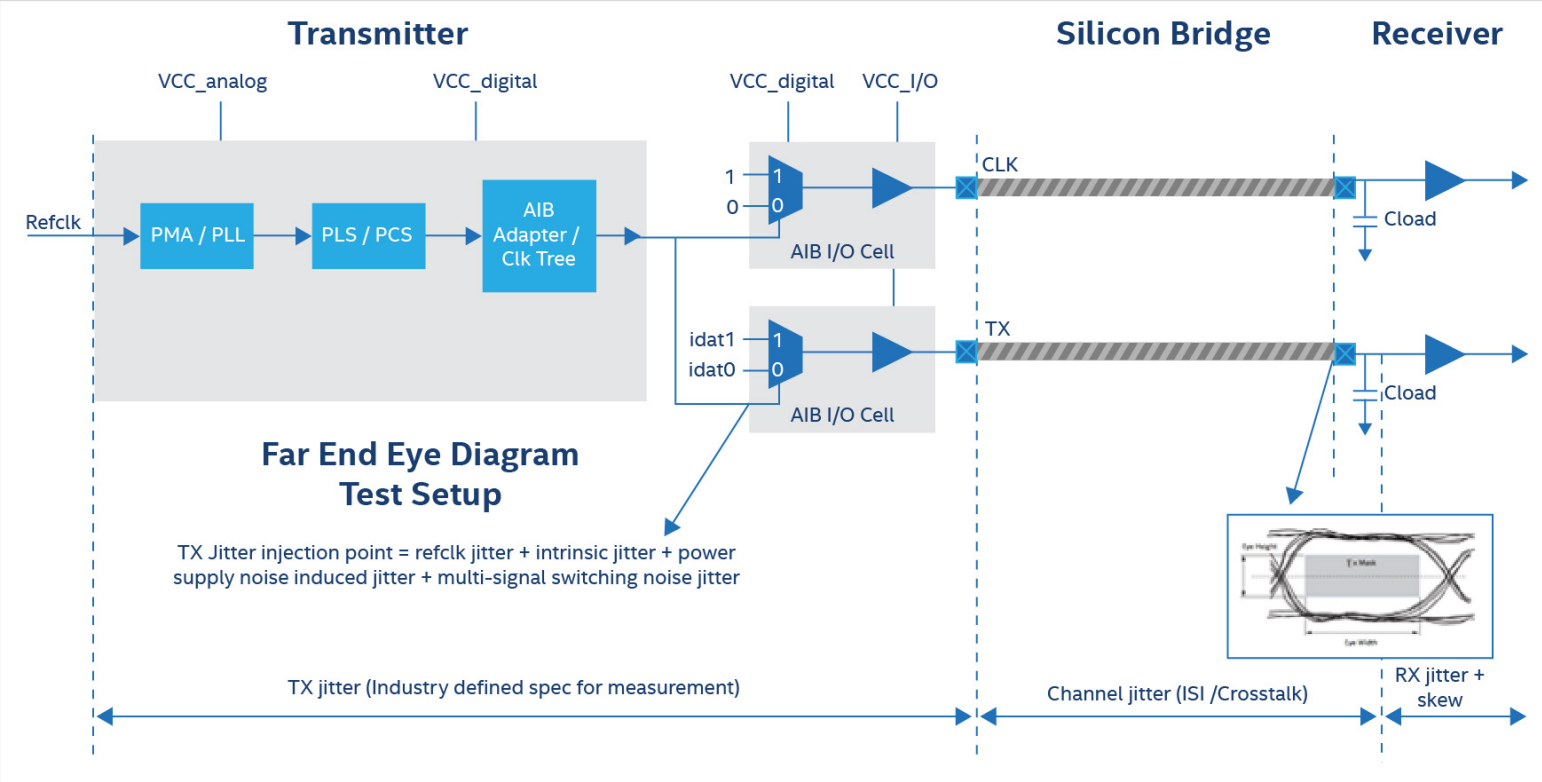
AIB Electrical Specification, Near End Eye Mask



Cload = 0.5 pF for 55 um bump pitch

Symbol	AC Timing Spec	TX (Near End)
Veh	Eye mask height (from 0.5x Vos)	+/- 90 mV
Tew	Min clock & data eye mask width	0.56 UI (a)

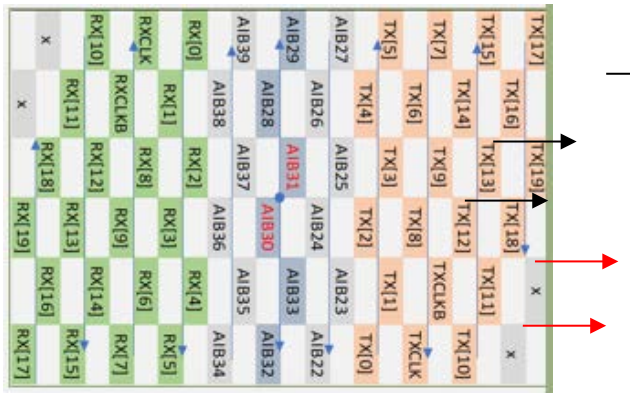
AIB Electrical Specification, Far End Eye Mask

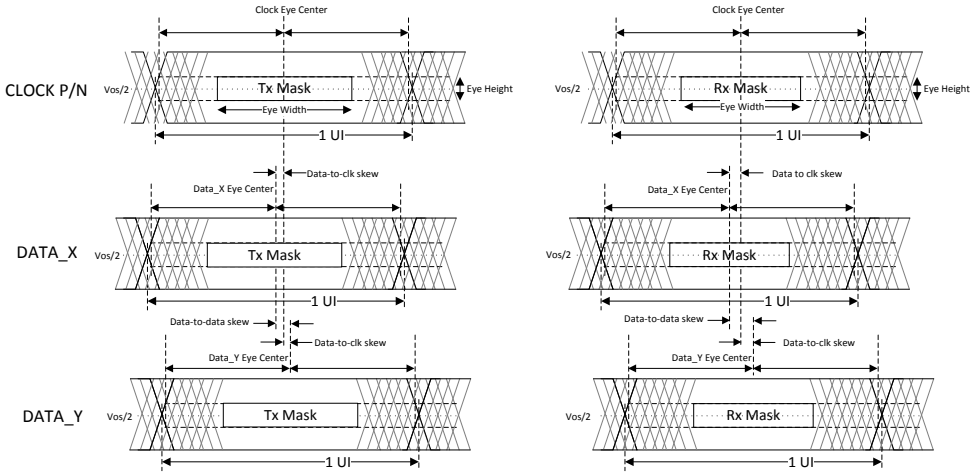


Cload = 0.5 pF for 55 um bump pitch

Symbol	AC Timing Spec	TX (Near End)	Channel	Lane to Lane Skew	RX (Far End)
Veh	Eye mask height (from 0.5x Vos)	+/- 90 mV			+/- 90 mV
Tew	Min clock & data eye mask width	0.56 UI (a)	0.1 UI (b)		0.4 UI

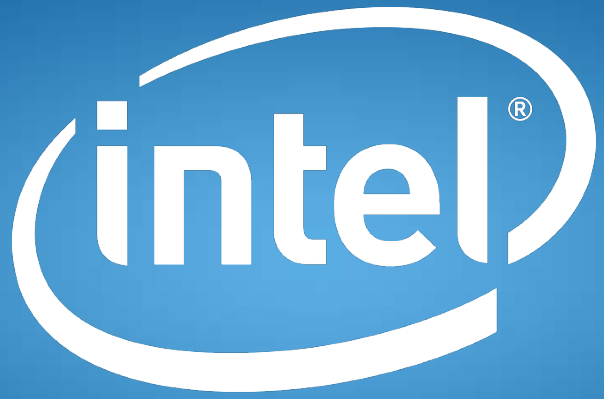
AIB Electrical Specification, DCD, and Clock Data Skew





Symbol	AC Timing Spec	TX (Near End)	Channel	Lane to Lane Skew	RX (Far End)
Veh	Eye mask height (from 0.5x Vos)	+/- 90 mV			+/- 90 mV
Tew	Min clock & data eye mask width	0.56 UI (a)	0.1 UI (b)		0.4 UI
Tfew	Forwarded clock eye mask width (ms_clk/clkb & sl_clk/clkb)	0.66 UI	0.1 UI	No skew requirement	0.56 UI
Tdcd	Clock DCD	+/- 3% (DDR) +/- 10% (SDR)			+/- 3% (DDR) +/- 10% (SDR)
Tds_ne	Max data to data skew (NE)			0.04 UI (c)	
Tdcs_ne	Max data to clock skew (NE)			0.02 UI (c)	
Tds_fe	Max data to data skew (FE w/o RX package skew)			0.06 UI (c)	
Tdcs_fe	Max data to clock skew (FE w/o RX package skew)			0.03 UI (c)	

Output Voltage Level = 0.7-0.9 V



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