

CHIPS Meets POSH&IDEA: The Advanced Interface Bus (AIB), Open Source and Physical Design Generation

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The Case for Chiplets



*"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."*¹

Gordon E. Moore

¹3rd Page of Moore's 1965 paper, "Cramming more components onto integrated circuits"



What is CHIPS?

CHIPS will develop the **design tools and integration standards** required to demonstrate **modular electronic systems** that can leverage **the best of DoD and commercial** designs and technology.

Intel is a performer on the DARPA CHIPS project

Today – Monolithic

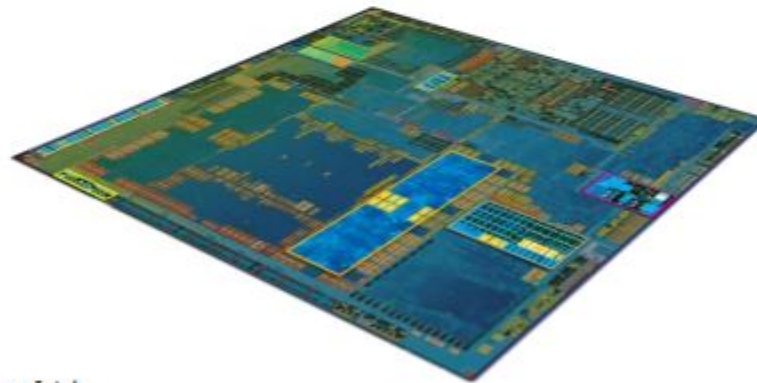
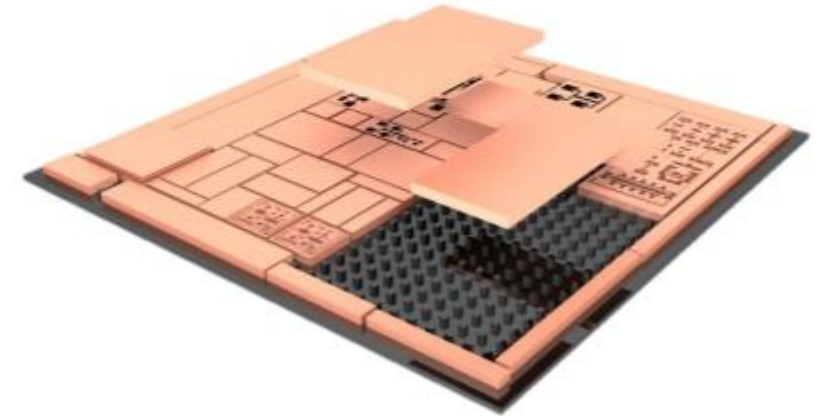


Image: Intel

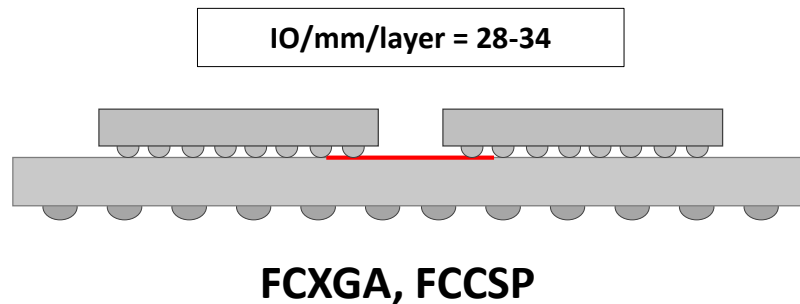
Tomorrow – Modular



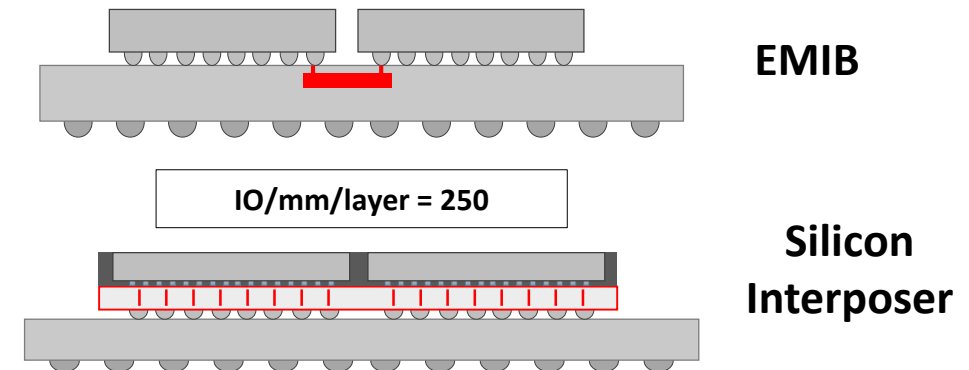
CHIPS is focused on creating modular IP – not new IP!

High-Density Packaging

Standard Flip-Chip Packaging Technology



High-Density Packaging Technology

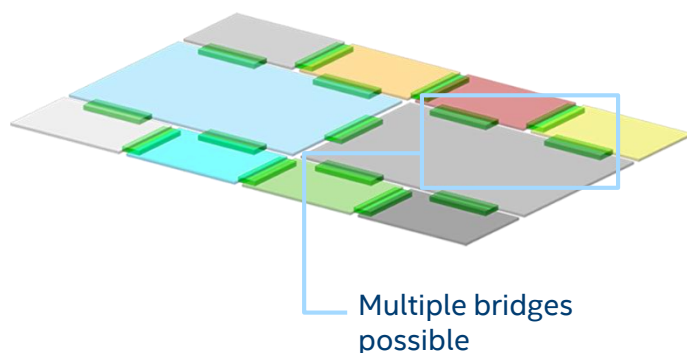


High-density packaging technology provides 7-8x IO density increase

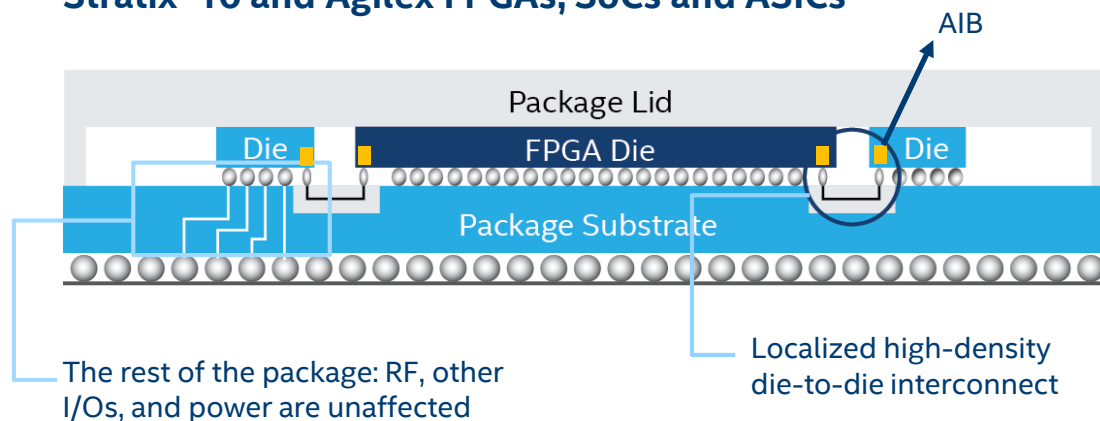
High-Density Packaging

EMIB or Silicon Interposer: Enabling technology for wide parallel interfaces

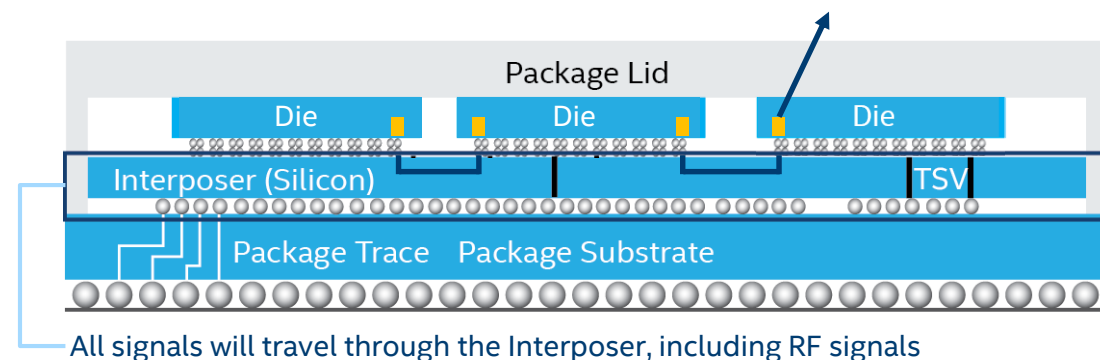
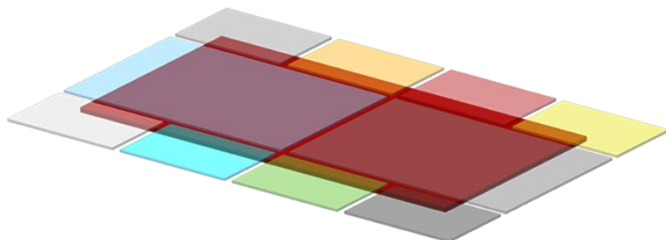
AIB over EMIB



Stratix® 10 and Agilex FPGAs, SoCs and ASICs



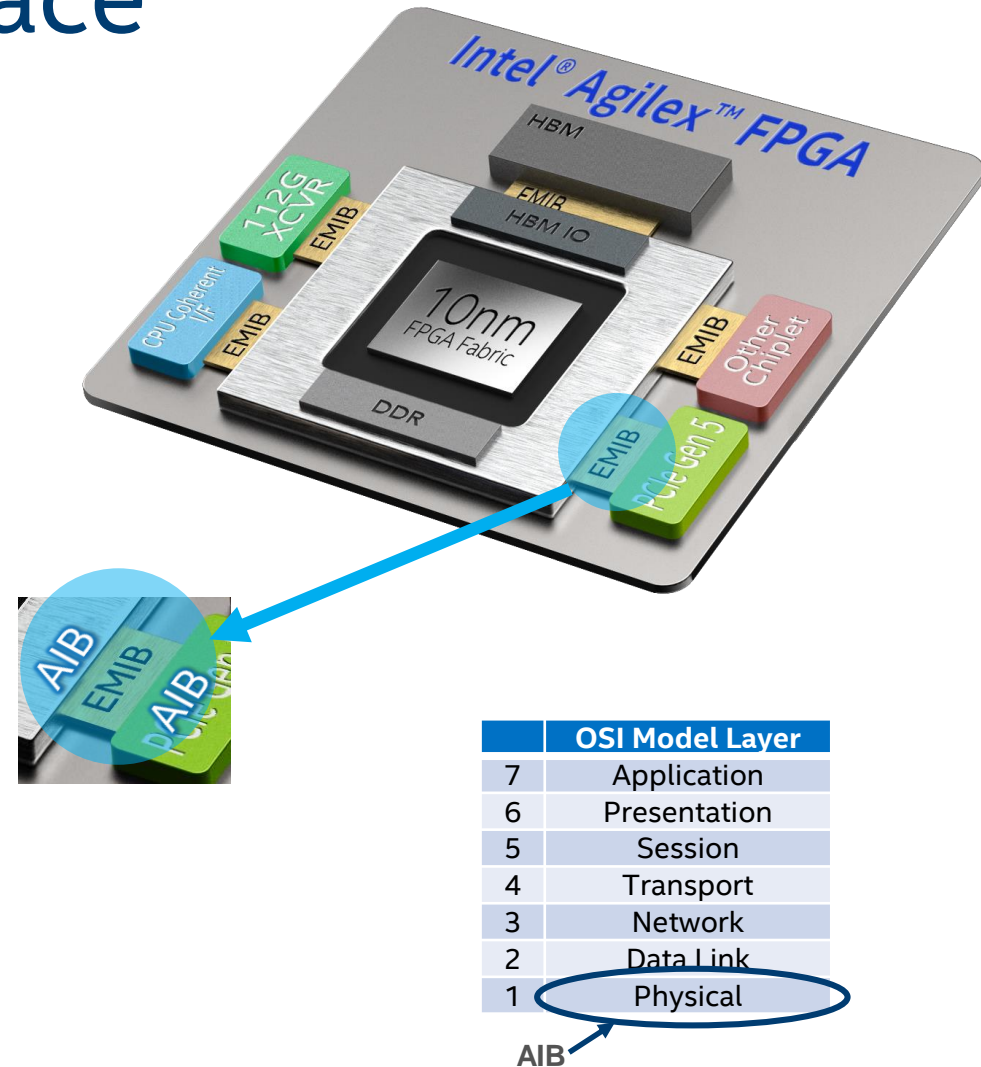
AIB over Silicon Interposer



AIB Die-to-Die Physical Interface

AIB: Common chiplet wide parallel physical interface

- **Advanced Interface Bus (AIB)**
- AIB is a clock-forwarded parallel data transfer like DDR DRAM
- Advanced Packaging with a 2.5D interposer like CoWoS* or EMIB
- AIB is PHY level: OSI Layer 1
- Build protocols like AXI*-4 or PCI Express* on top of AIB



Growing AIB-Based Chiplet Ecosystem

Chiplets in production with Intel® Stratix™ 10 FPGAs

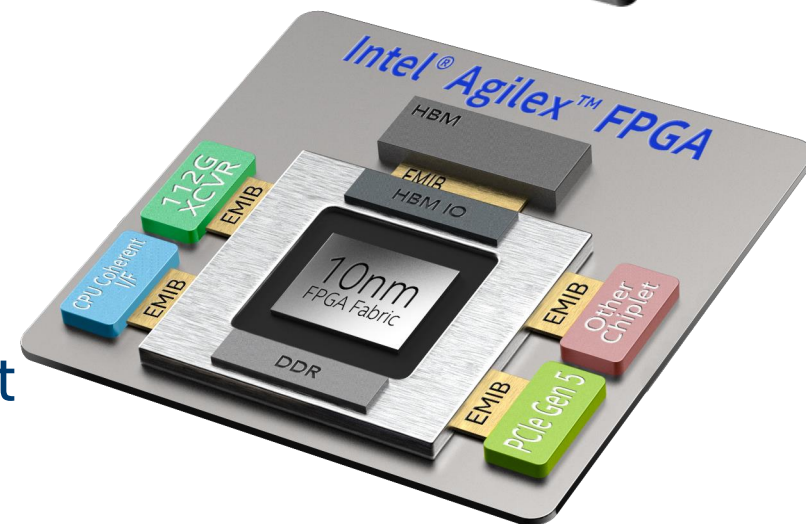
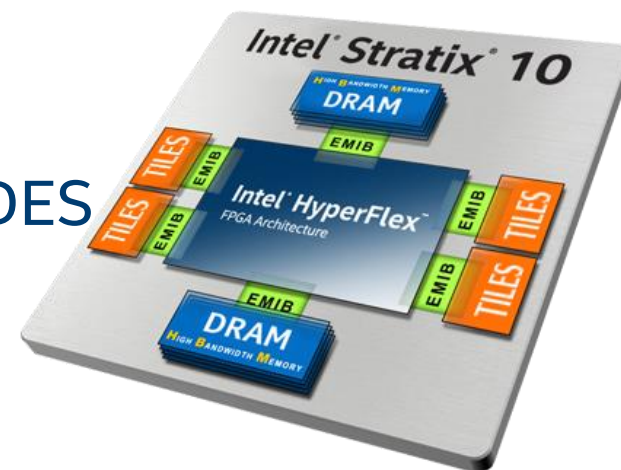
- L-Tile 17G SERDES, H-Tile 28G SERDES, E-Tile 58G SERDES

New chiplets with Intel® Agilex™ FPGAs

- F-Tile 112 Gbps serializer /deserializer (SERDES)
- P-Tile PCI Express* (PCIe) Gen4
- R-Tile PCIe Gen5 and Compute Express Link* (CXL)
- Custom intellectual property (IP) via Intel® eASIC™

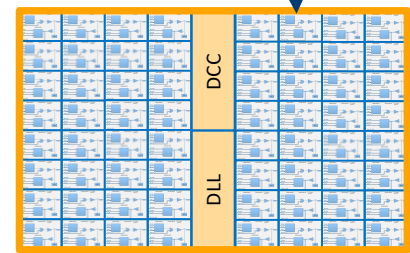
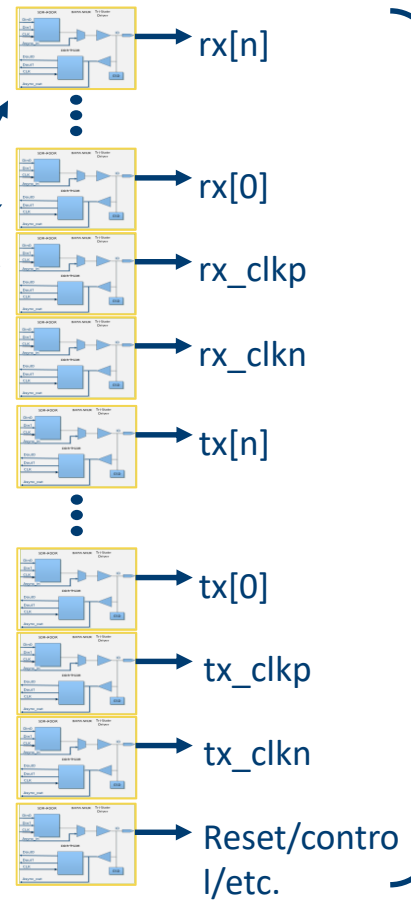
Industry adoption

- Jariet Technologies 64Gsamples/s ADC/DAC chiplet
- Ayar Labs photonics chiplet
- *Others coming soon*



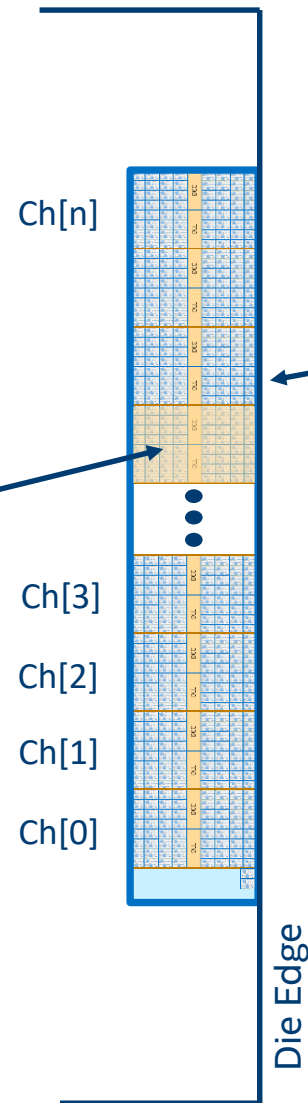
AIB I/O Cell, Channel, and Column

An **AIB I/O cell** may be used for receiving data, transmitting data, clock, or control



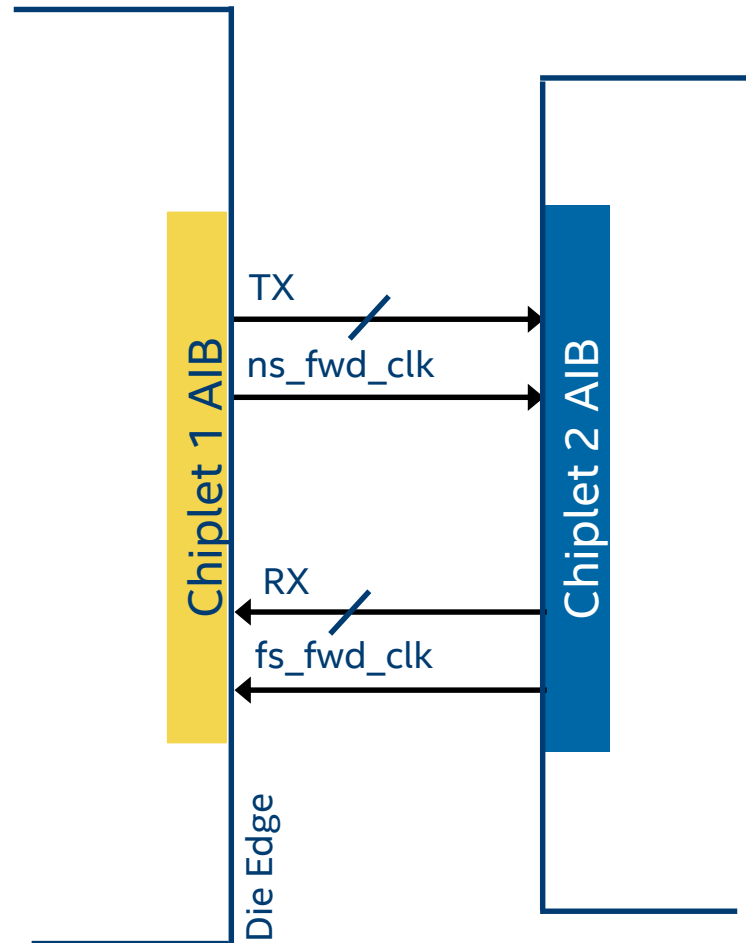
An **AIB channel** is an array of AIB I/Os, DLL, DCC, and clock distribution

DLL: Delay Locked Loop for clock phase centering
DCC: Duty Cycle Correction for improved double-data rate transfers



An **AIB column** consists of stacked AIB channels (typically 24)

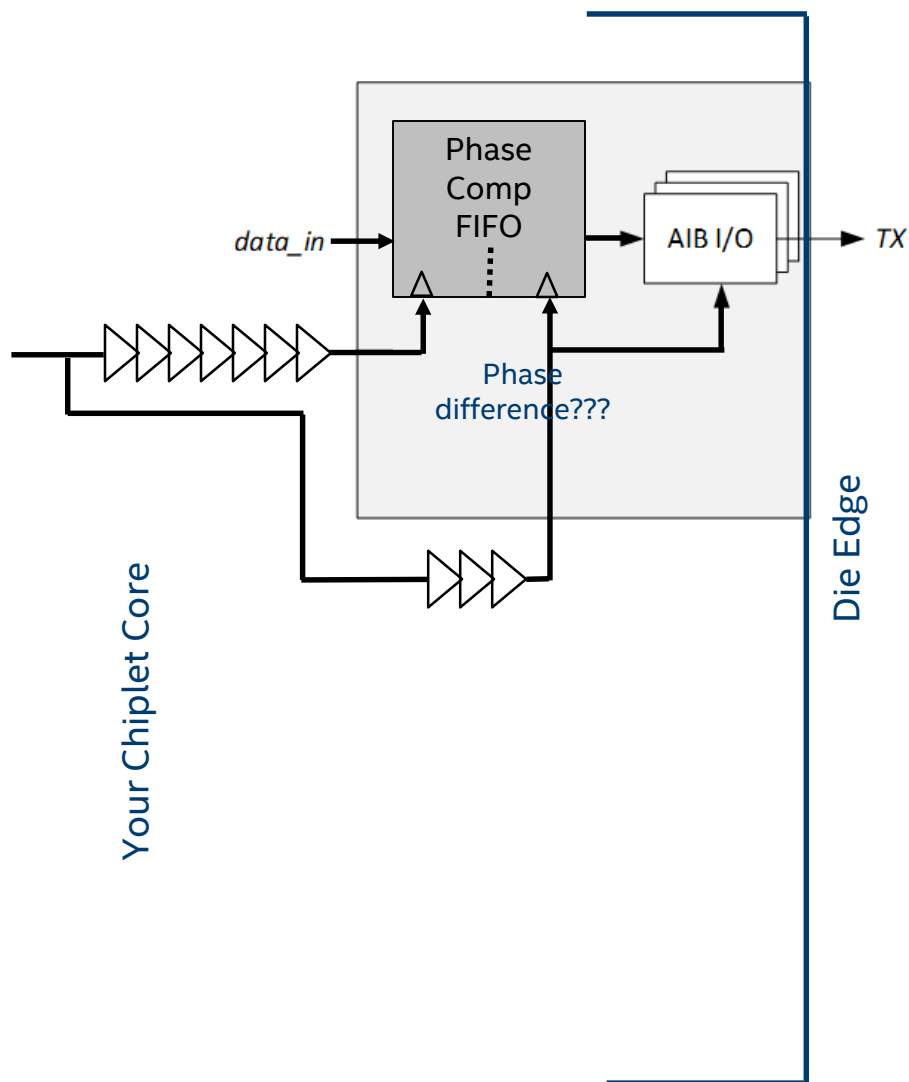
Simplest AIB Clocking Configuration (One Channel)



Each chiplet originates its own clock for transmitting to the other side

- Each channel can forward an independent clock or the same clock

Clocking Inside Your Chiplet



The clock distribution between your chiplet core and the AIB I/O may be a completely different tree, even when the clocks are the same source (0 PPM difference)

- *Mesochronous: same frequency, unknown phase*
- You need a phase compensation FIFO in this case

Channels

I have a 512 bit data bus each way. Why do I need to use channels?

A single transmit (TX) clock must be balanced to each TX I/O cell in the channel, same with receive (RX) clock

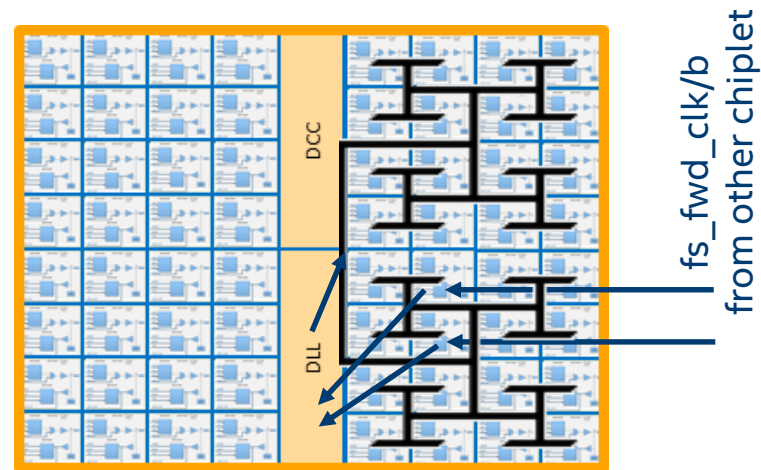
- Clock routing and controlling skew limit the number of I/Os per clock
- A wide bus will need to be spread across channels

Pick too many I/Os per channel, then:

- You waste I/Os in low-bandwidth applications like Gigabit Ethernet

Pick too few I/Os per channel then:

- You have to spread most higher bandwidth links across more than one channel



Example of AIB channel
balanced clock distribution

AIB 2.0 Technology Drivers

Microbump spacing

- 55u is in production
- 35u provides a doubling of density.

I/O voltage

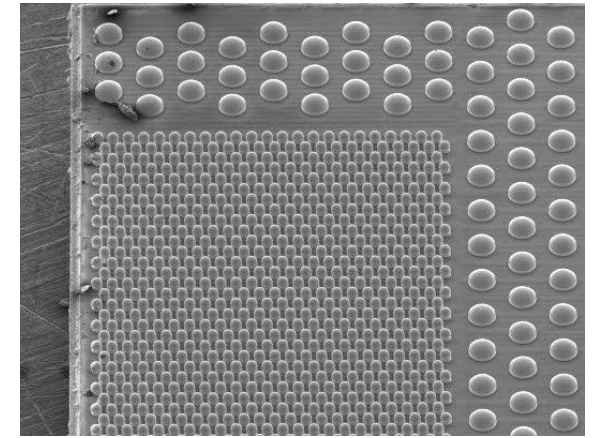
- 0.4V swing (down from 0.9V) to achieve <0.5pJ/bit

Line rate

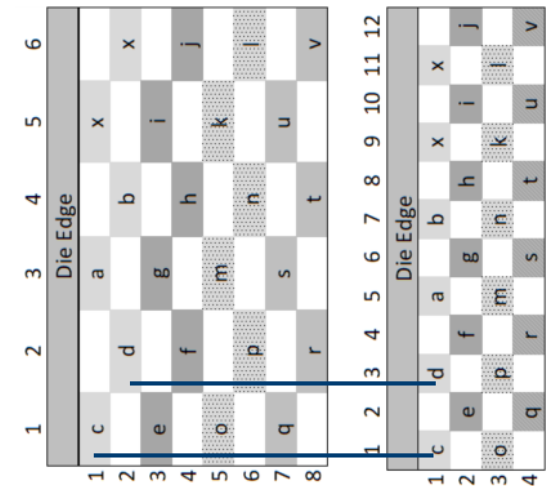
- Very high-bandwidth applications such as direct RF sampling analog-to-digital converters (ADCs) or digital-to-analog converters (DACs) will continue to push higher bandwidth
- Doubling the data rate to 4Gbps

Microbump spacing + I/O voltage + line rate → **AIB 2.0**

Tile backward compatibility and reuse is essential

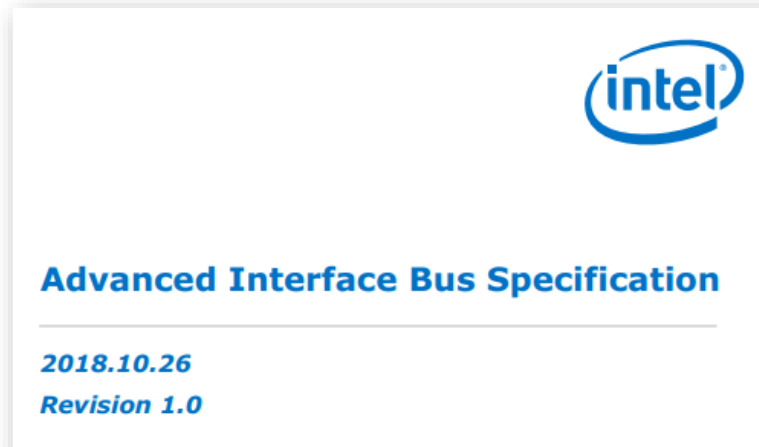


Intel® Stratix® 10 FPGA 55u microbump array



**55u to 35u microbump
assignment for straight-line
routing compatibility**

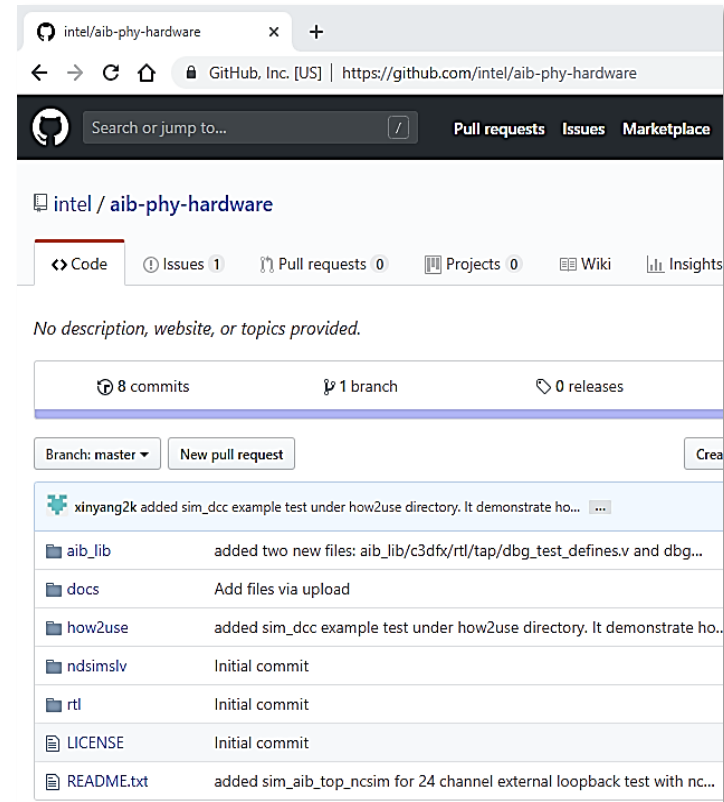
AIB Public Releases



AIB Specification Released October 2018

AIB Public Specification includes:

- Electrical specs, bump array mechanicals, data/clock/ control signal definitions, reset handshaking, JTAG reqts
- Available at <https://github.com/intel/aib-phy-hardware/tree/master/docs>

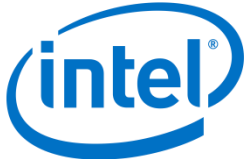


AIB Open Source Released January 2019

AIB Open Source on GitHub

- Register transfer level (RTL), netlists, generic cell library
- Available at <https://github.com/intel/aib-phy-hardware>
- Purpose: **reduce development cost**

Intel Open Source Process



Security

Security Development

Home

MySDL Admin

SDL Essentials

Classic SDL

Resources

Security Exceptions

Reports

SAFE Crypto Subteam

PSIRT

Customer Inquiry

Report an Issue

Questions or Ideas

Advanced Interface

Open source release of Advanced Interface

Code Center

Code Center

Application IP Plan

Terminology

- Application – IP Plan
- Project
- Bill of Materials (BOM)
- Component
 - KnowledgeBase (KB)
 - Custom Project (CP)

Intel Software Legal Compliance

☒ SDL330 - Conduct Manual Code Reviews

☒ SDL430 - Fix Critical and High (ECVSS) Vulnerabilities

SWLC Tools & Practices

Concepts

IP Planning

- Bill of Materials (BOM)
- License Obligations
- Export Control

Code Scans

- Code audited
- Origin of code
- License obligations

Product Description

Advanced Interface hardware open

The export classification of technical assistance prior to collaboration

This product can be found here <https://spg.intel.com> allowed to be e

Create Component

SWLC Tools

Knowledge

Export Compliance Classification

Hi David,

The review of your product has been completed. This email is to inform you of the export classification status of this product. The export classification status applies to the product as submitted as of today. Any changes to the product will require a new PCQ submission and further review. The U.S. Export Classification for this product is as follows:

The "Yes" Checklist

- Has your management approved the project? **Y**
 - Name of approving manager
- Is your IP plan complete?

From: Yan, Kenneth

Sent: Thursday, January 28, 2019 3:01 PM

Subject: RE: IP Planning

RTL is out of scope
- Have you determined the export classification requirements here <https://spg.intel.com>?
 - "This product can be found here <https://spg.intel.com>"
 - PCQ 7870
- Have you completed the export classification requirements?
 - Approved by Branch Manager
 - Proper usage, FYI
- Have you met all the requirements?
 - Name of your BU sponsor
 - Link to your MySDL

2.1 Product update mechanisms

Verilog open source will be posted to a repository on GitHub. Updates to GitHub will be administered by David Kehlet david.kehlet@intel.com. In David's absence, responsibility will be assigned to Jose Alvarez jose.alvarez@intel.com. The PSG CTO office will review pull requests and issues filed on GitHub. The PSG CTO office will ensure the change is developed and released.

Open Source Approval Review

Analysis Complete

Analysis of your project is now complete.

Started On: Jan 28, 2019 3:01:57 PM

Finished On: Jan 28, 2019 3:03:40 PM

Started By: julie.zhang@intel.com

Project: AIB PHY HARDWARE rev0

Total # of Files: 373

Files Analyzed: 373

Bytes Analyzed: 3,769,415

Scan Errors: 0

Scan Warnings: 0

Details:

(INFO) Files pending identification: 1

(INFO) Files scanned successfully with no discoveries: 372

(INFO) Logged messages by severity: 4 info

☒ Proceed to the next step

OK

Blackduck/Protex Scan

GEC) Shipping

its.aspx"

brands? Y

SG champion

D=5747

Completed

Last Updated

2019-01-17

2019-01-17

Updated By

Depends

June

Help

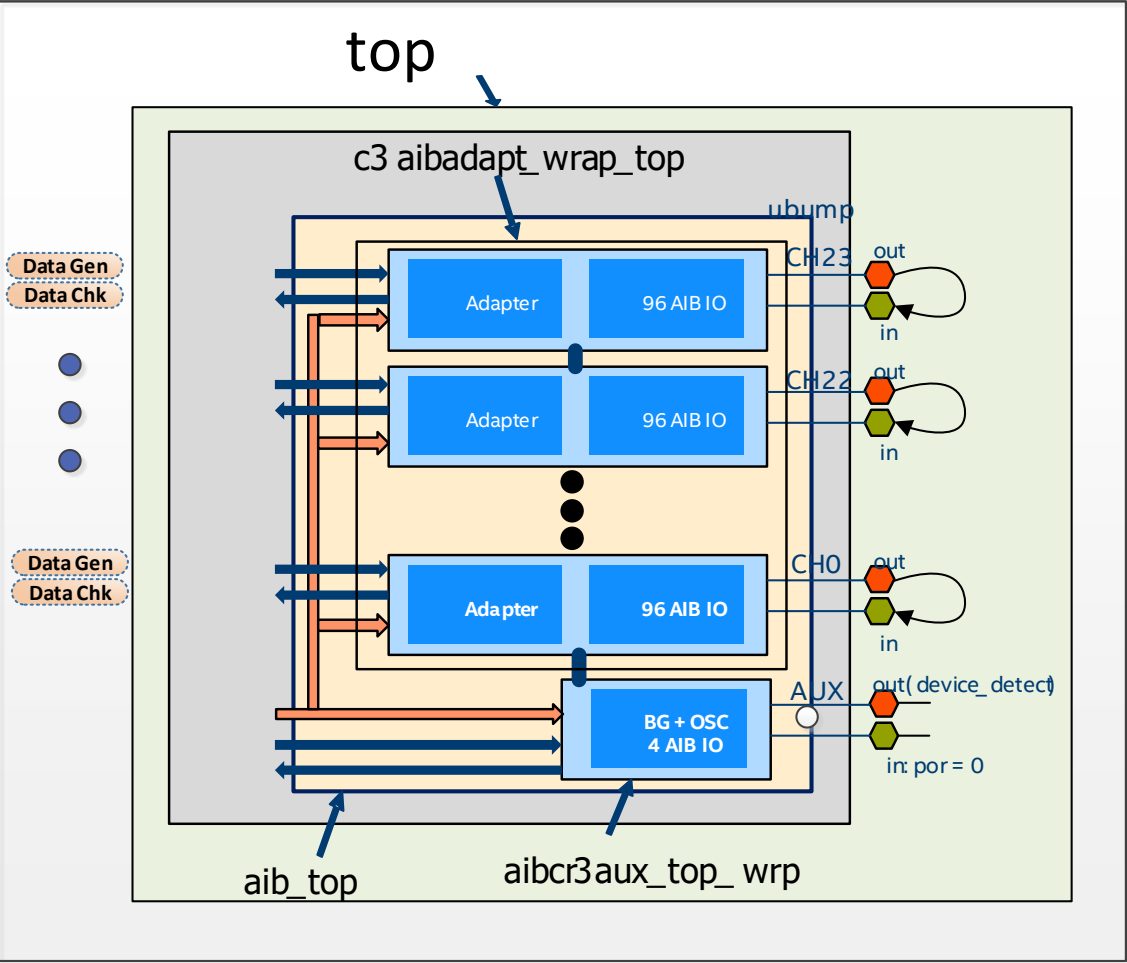
1/1

1/1

3/3

5/5

Example of Testing 24 Channel AIB



intel / aib-phy-hardware

Code Issues 0 Pull requests 0 Proj

Branch: master aib-phy-hardware / how2use /

xinyang2k added sim_modelsim under how2use directory. This is th

..

sim_aib_top	added how2use directory, ad
sim_aib_top_ncsim	added sim_aib_top_ncsim for
sim_dcc	added sim_dcc example test t
sim_modelsim	added sim_modelsim under h
sim_phasecom	added sim_phasecom simulat
README.txt	added sim_modelsim under h

Generic Cells

```
// SPDX-License-Identifier: Apache-2.0
// Copyright (C) 2019 Intel Corporation. All rights reserved
// *****
// *****
// Copyright © 2016 Altera Corporation. All rights reserved. Altera products are
// protected under numerous U.S. and foreign patents, maskwork rights, copyrights and
// other intellectual property laws.
// *****
// Module Name : c3lib_and2_svt_4x
// Date       : Thu Sep 15 13:44:58 2016
// Description : 2-input AND gate (SVT, 4x drive strength)
// *****

module c3lib_and2_svt_4x(
    in0,
    in1,
    out

);

input    in0;
input    in1;
output   out;

    assign out = in0 & in1;

endmodule
```

Open Source has a behavioral model for this AND gate
A user should replace this with a PDK-specific cell

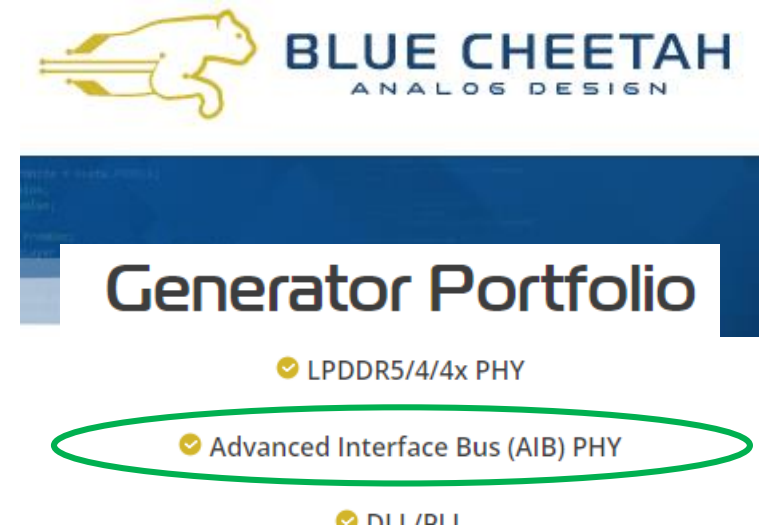
AIB IP Generation Project: Intel and Blue Cheetah

Technology and design flow to create physical designs from specifications and circuit generators

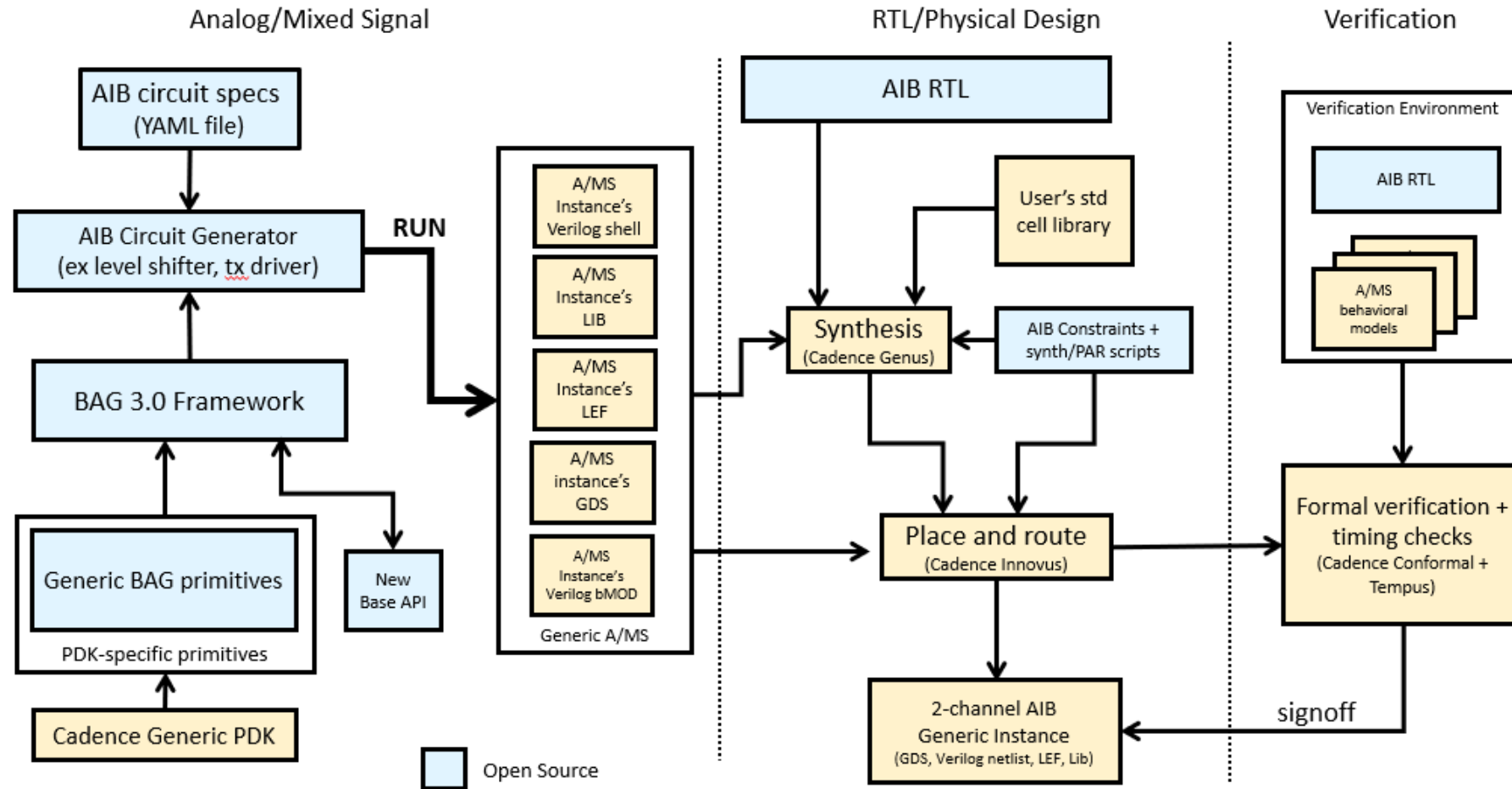
Uses Berkeley Analog Generator 3.0

Potential dramatic reduction in porting labor

Developed specifications and generators for AIB using Intel 22FFL PDK



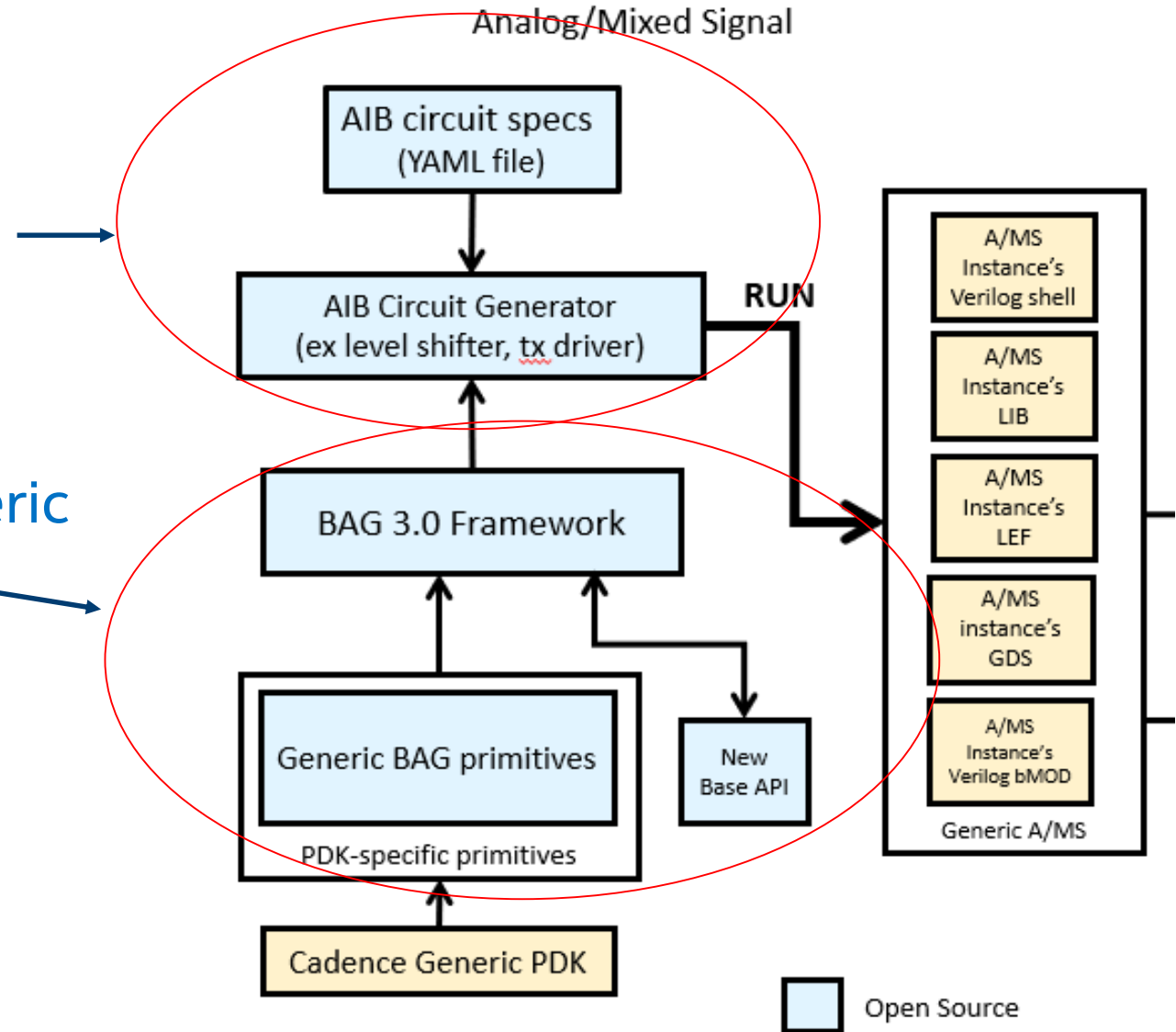
AIB Generator Design Flow with Generic PDK



AIB Generator

AIB specific: AIB Circuit Specs, AIB Circuit Generator

Generic: BAG 3.0 Framework, Generic BAG primitives, New Base API

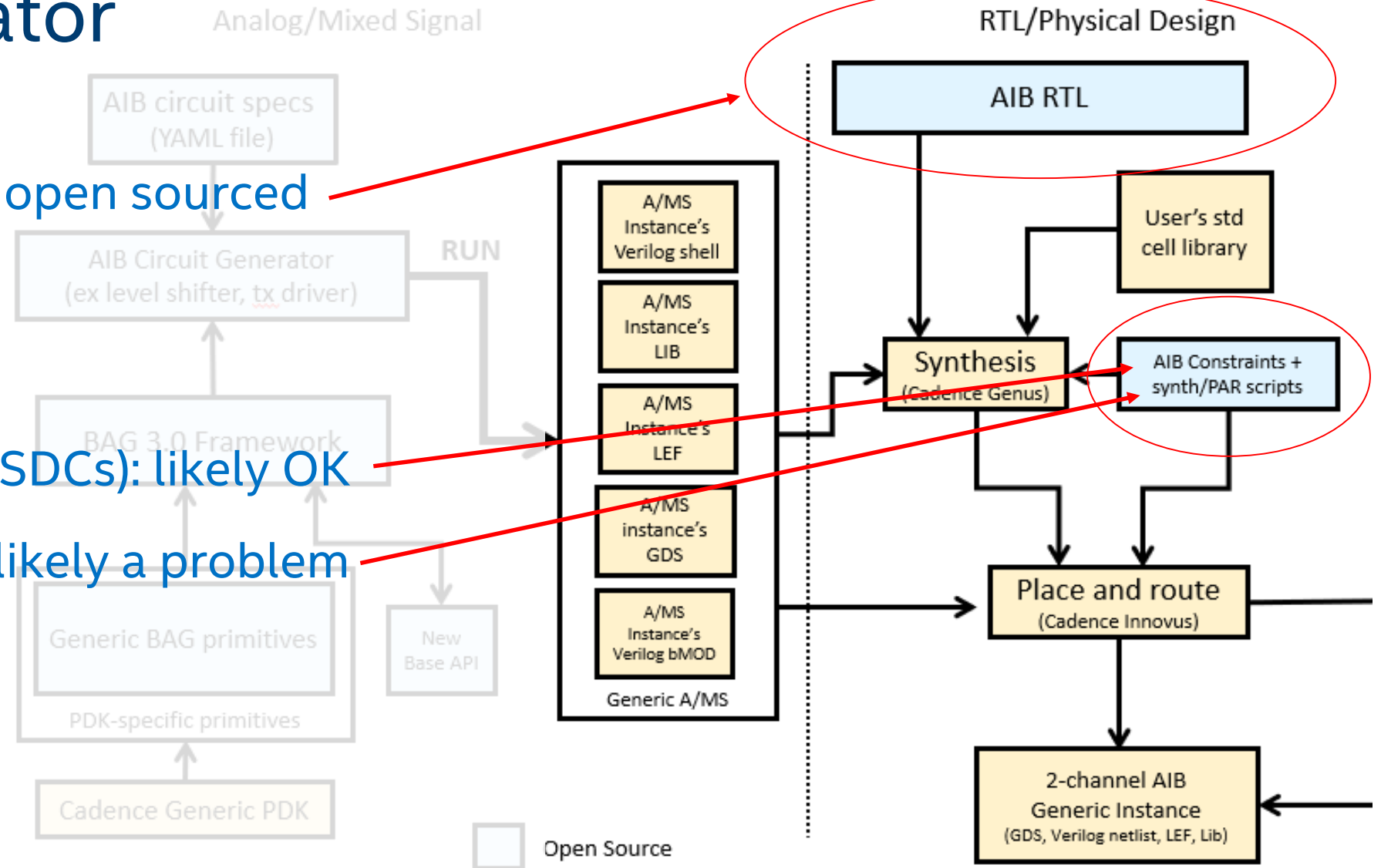


AIB Generator

AIB RTL: already open sourced

AIB Constraints (SDCs): likely OK

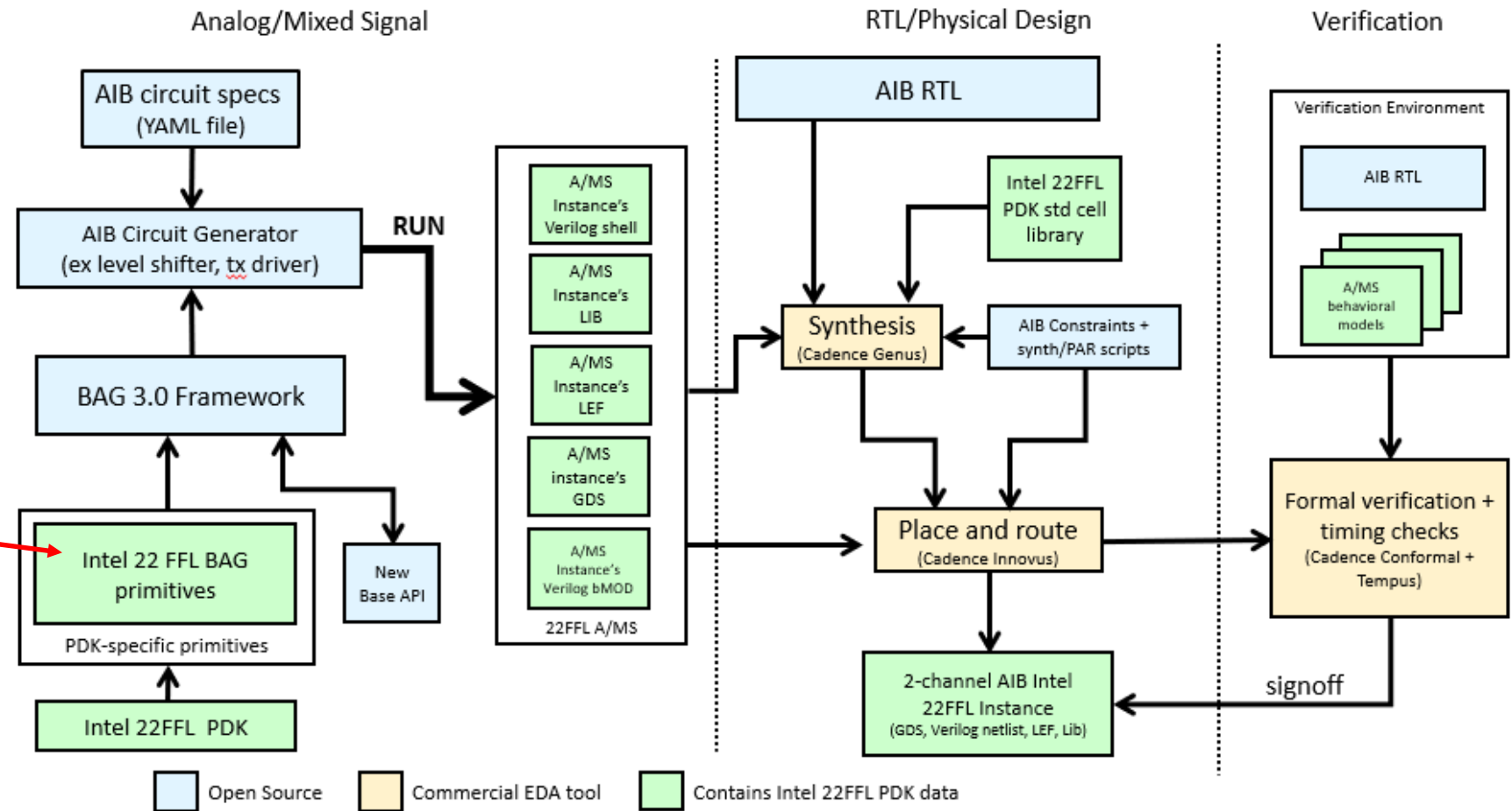
AIB PAR scripts: likely a problem



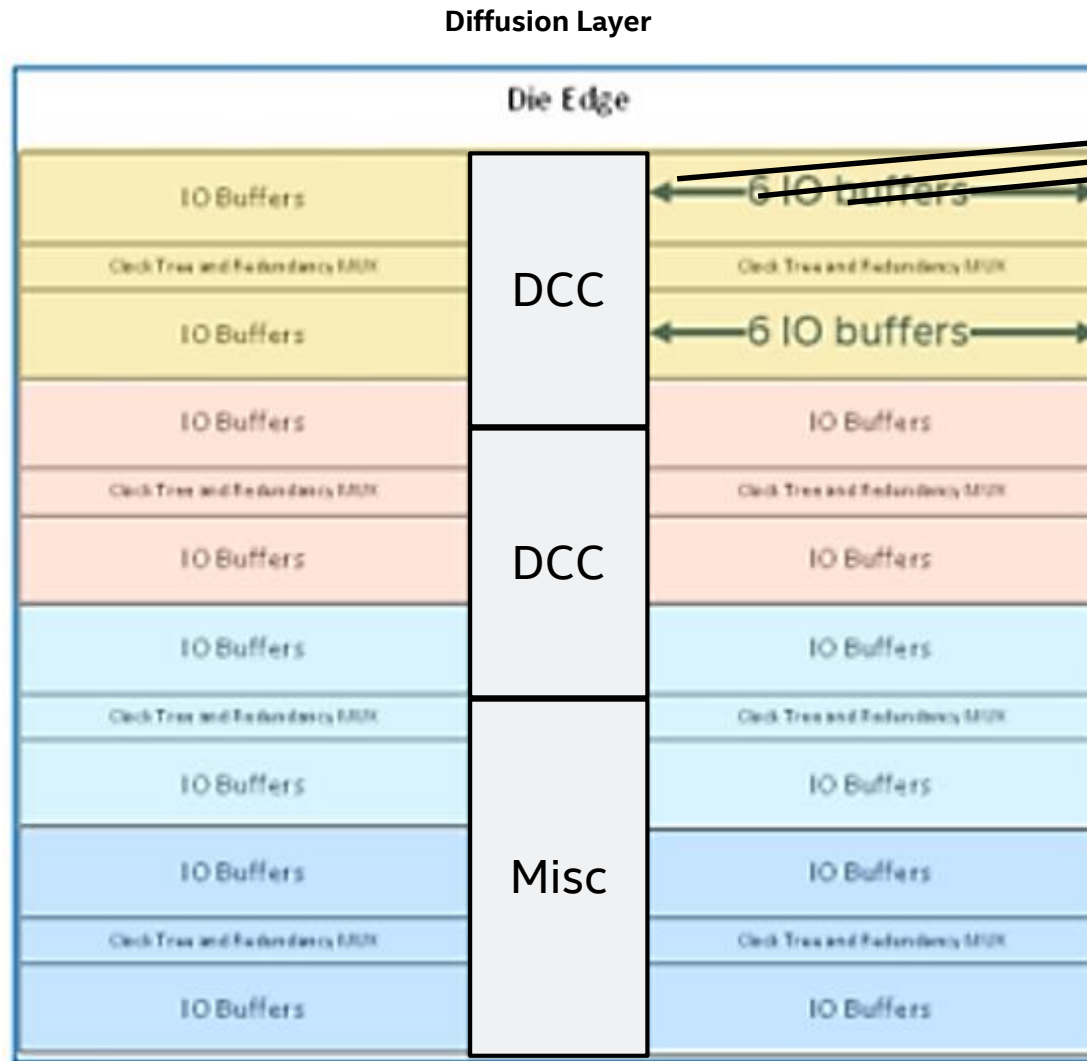
AIB Generator Design Flow with Intel 22FFL PDK

Open source flow works, even though we cannot open source anything with Intel PDK data

“Secret sauce” is in the “Intel 22FFL Bag primitives”



IO Cell Placement and Microbump Routing



Redistribution to Microbumps

	1	2	3	5	6
Edge of Chiplet					
A	VCCIO		VCCIO		VCCIO
B		VCCIO		VCCIO	VCCIO
C	VCCIO		VCCIO		VCCIO
D		VCCIO		VCCIO	VCCIO
E	VSS		VSS		VSS
F		VSS		VSS	VSS
G	AIB16		AIB41		AIB2
H		AIB12		AIB8	AIB46
I	AIB17		AIB40		AIB3
J		AIB13		AIB9	AIB47
K	AIB18		AIB10		AIB4
L		AIB14		AIB6	AIB0
M	AIB19		AIB11		AIB5
N		AIB15		AIB7	AIB1
O	AIB44		AIB30		AIB24
P		AIB34		AIB43	AIB20
Q	AIB45		AIB31		AIB25
R		AIB35		AIB42	AIB21
S	AIB38		AIB32		AIB26
T		AIB36		AIB28	AIB22
U	AIB39		AIB33		AIB27
V		AIB37		AIB29	AIB23
W	VSS		VSS		VSS
X		VSS		VSS	VSS
Y	VCCD		VCCD		VCCD
Z		VCCD		VCCD	VCCD
AA	AIB57		AIB87		AIB93
AB		AIB64		AIB83	AIB66
AC	AIB59		AIB86		AIB92
AD		AIB65		AIB82	AIB67
AE	AIB51		AIB78		AIB71
AF		AIB80		AIB89	AIB68
AG	AIB52		AIB79		AIB70
AH		AIB81		AIB88	AIB69

CHIPS Meets POSH&IDEA

Test Chip Using AIB IP Generator Technology

- 12/2019 AIB Generator test chip “tape in”
- Q1 2020 Intel 22FFL internal shuttle

We would like to thank **Mr. Andreas Olofsson** for his support.

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