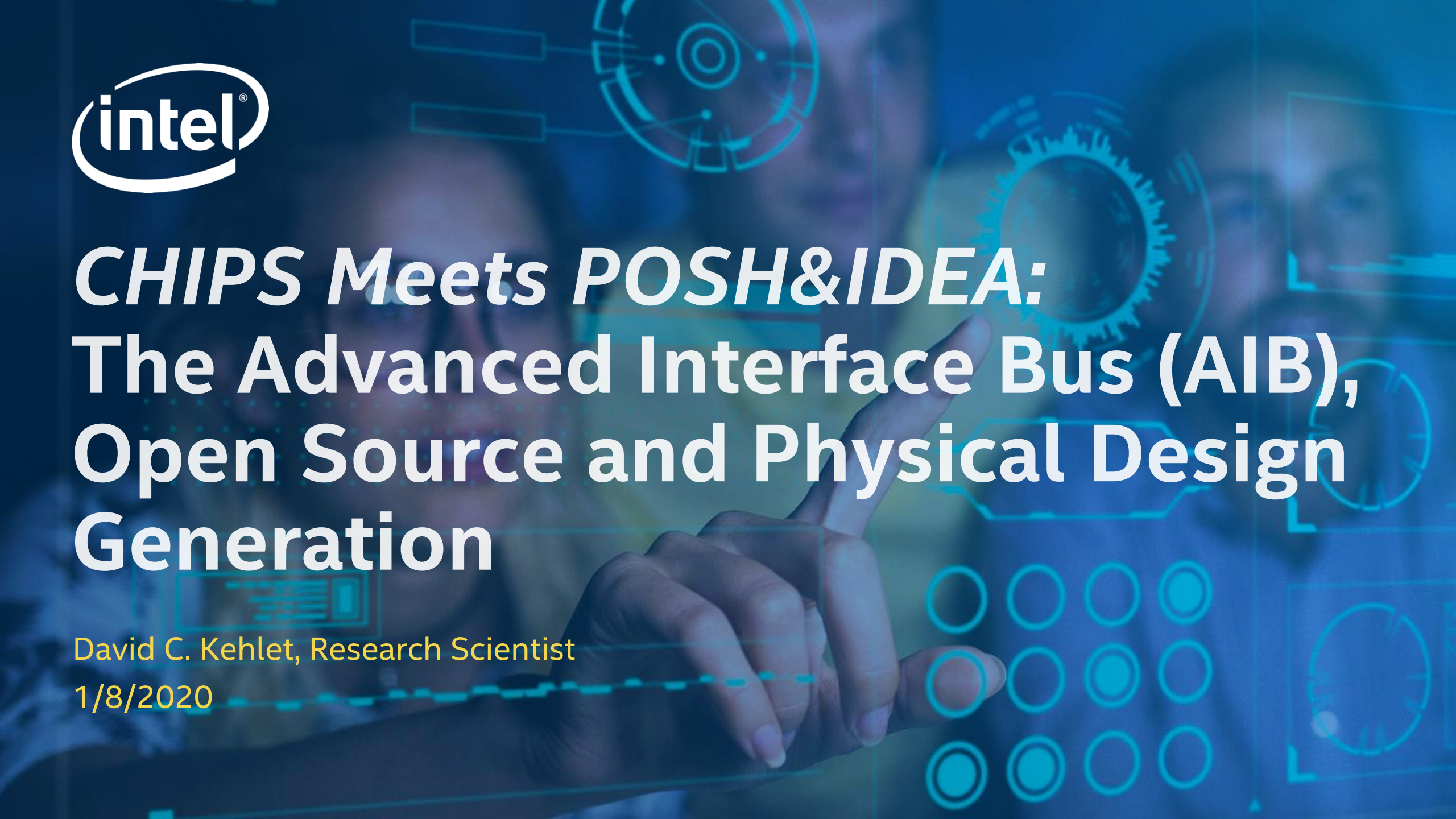

CHIPS Meets POSH&IDEA: The Advanced Interface Bus (AIB), Open Source and Physical Design Generation

David C. Kehlet, Research Scientist

1/8/2020

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The Case for Chiplets

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected." [1]

Gordon E. Moore

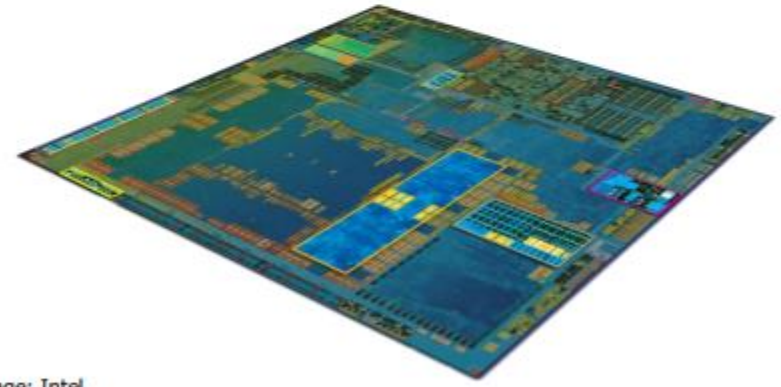
[1] 3rd Page of Moore's 1965 paper, "Cramming more components onto integrated circuits"

Intel is a performer on the DARPA CHIPS project

What is CHIPS?

CHIPS will develop the **design tools and integration standards** required to demonstrate **modular electronic systems** that can leverage **the best of DoD and commercial** designs and technology.

Today – Monolithic



Tomorrow – Modular

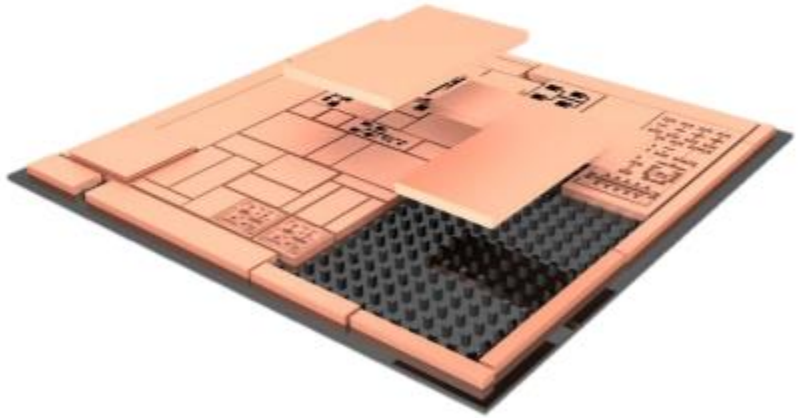
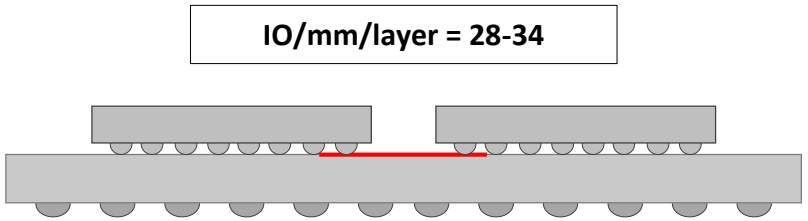


Image: Intel

CHIPS is focused on creating modular IP – not new IP!

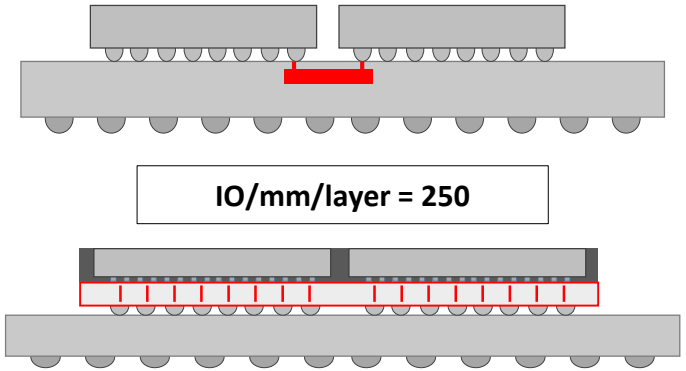
High-Density Packaging

Standard Flip-Chip Packaging Technology



FCXGA, FCCSP

High-Density Packaging Technology



EMIB

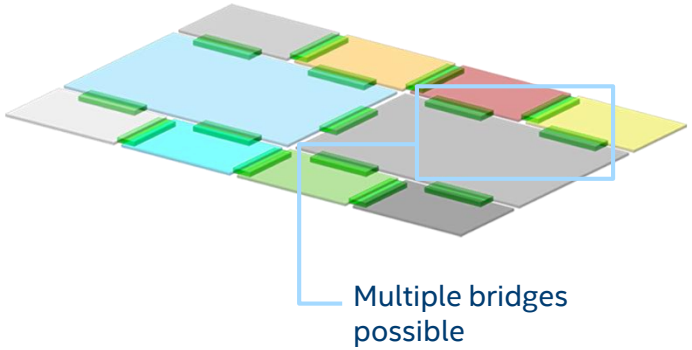
Silicon Interposer

High-density packaging technology provides 7-8x IO density increase

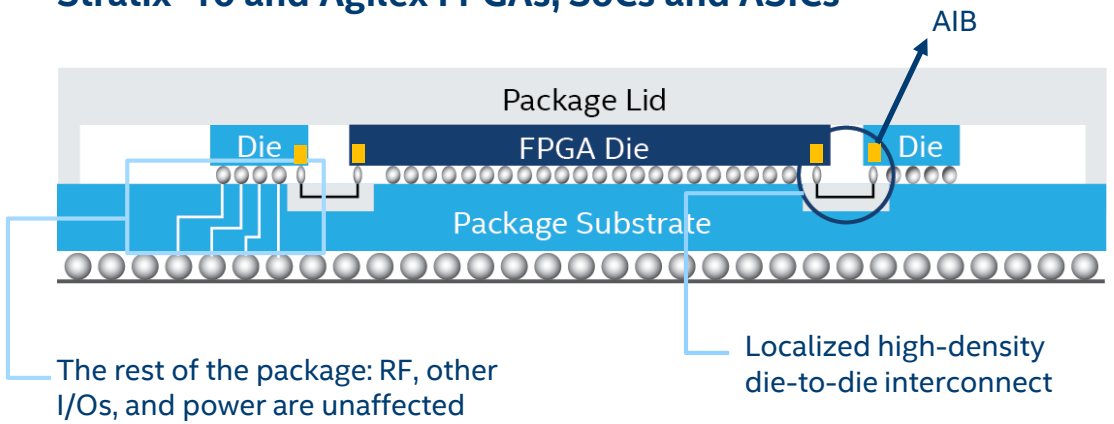
High-Density Packaging

EMIB or Silicon Interposer: Enabling technology for wide parallel interfaces

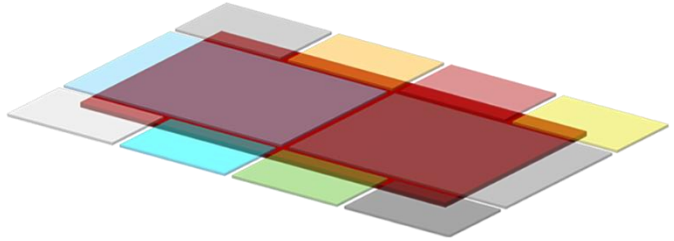
AIB over EMIB

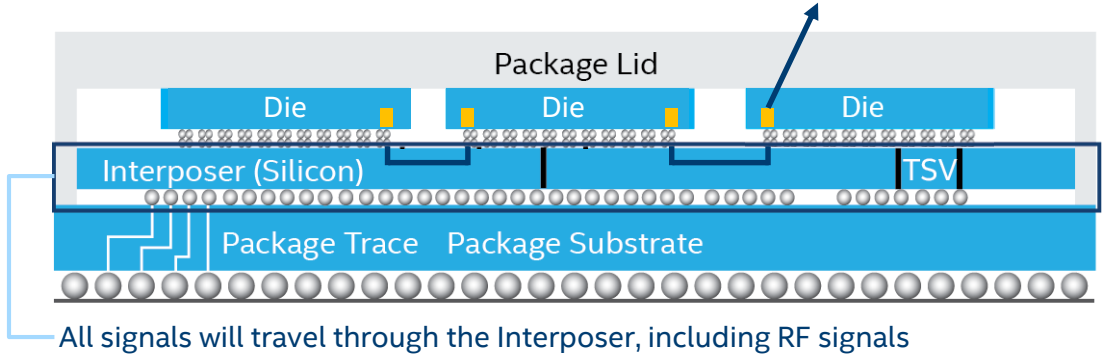


Stratix® 10 and Agilex FPGAs, SoCs and ASICs



AIB over Silicon Interposer

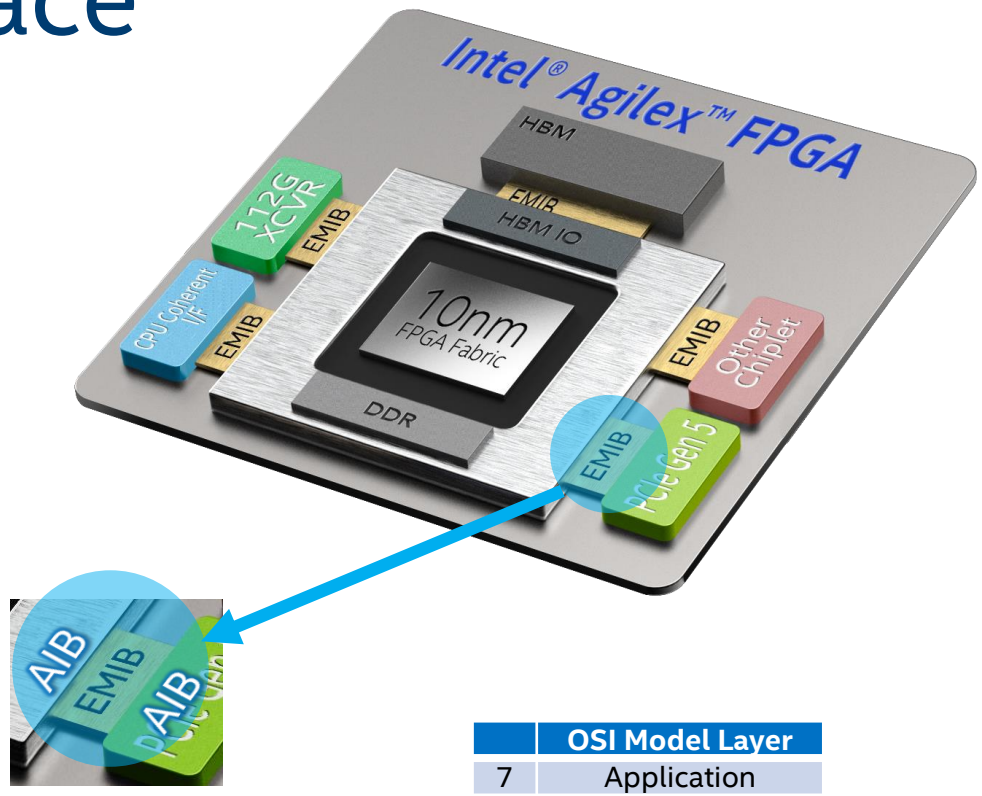




AIB Die-to-Die Physical Interface

AIB: Common chiplet wide parallel physical interface

- **A**dvanced **I**nterface **B**us (AIB)
- AIB is a clock-forwarded parallel data transfer like DDR DRAM
- Advanced Packaging with a 2.5D interposer like CoWoS* or EMIB
- AIB is PHY level: OSI Layer 1
- Build protocols like AXI*-4 or PCI Express* on top of AIB



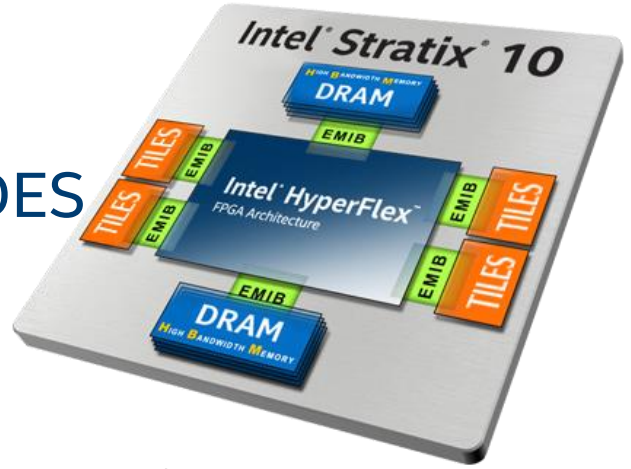
	OSI Model Layer
7	Application
6	Presentation
5	Session
4	Transport
3	Network
2	Data Link
1	Physical

AIB

Growing AIB-Based Chiplet Ecosystem

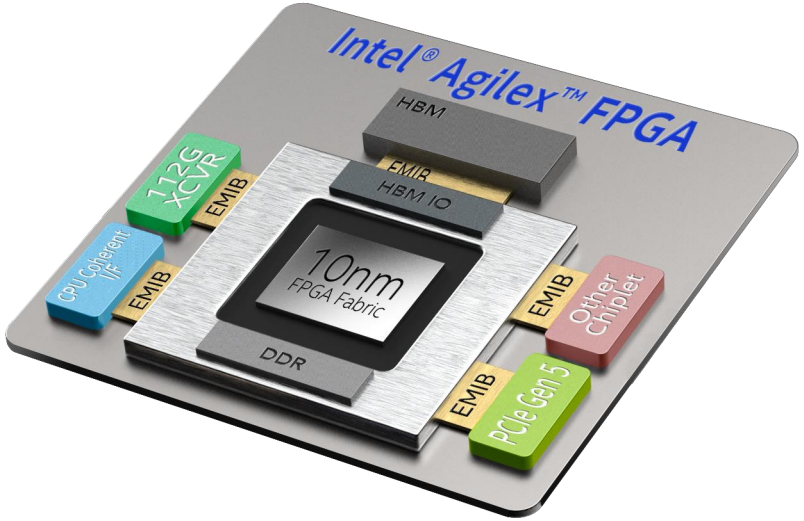
Chiplets in production with Intel® Stratix™ 10 FPGAs

- L-Tile 17G SERDES, H-Tile 28G SERDES, E-Tile 58G SERDES



New chiplets with Intel® Agilex™ FPGAs

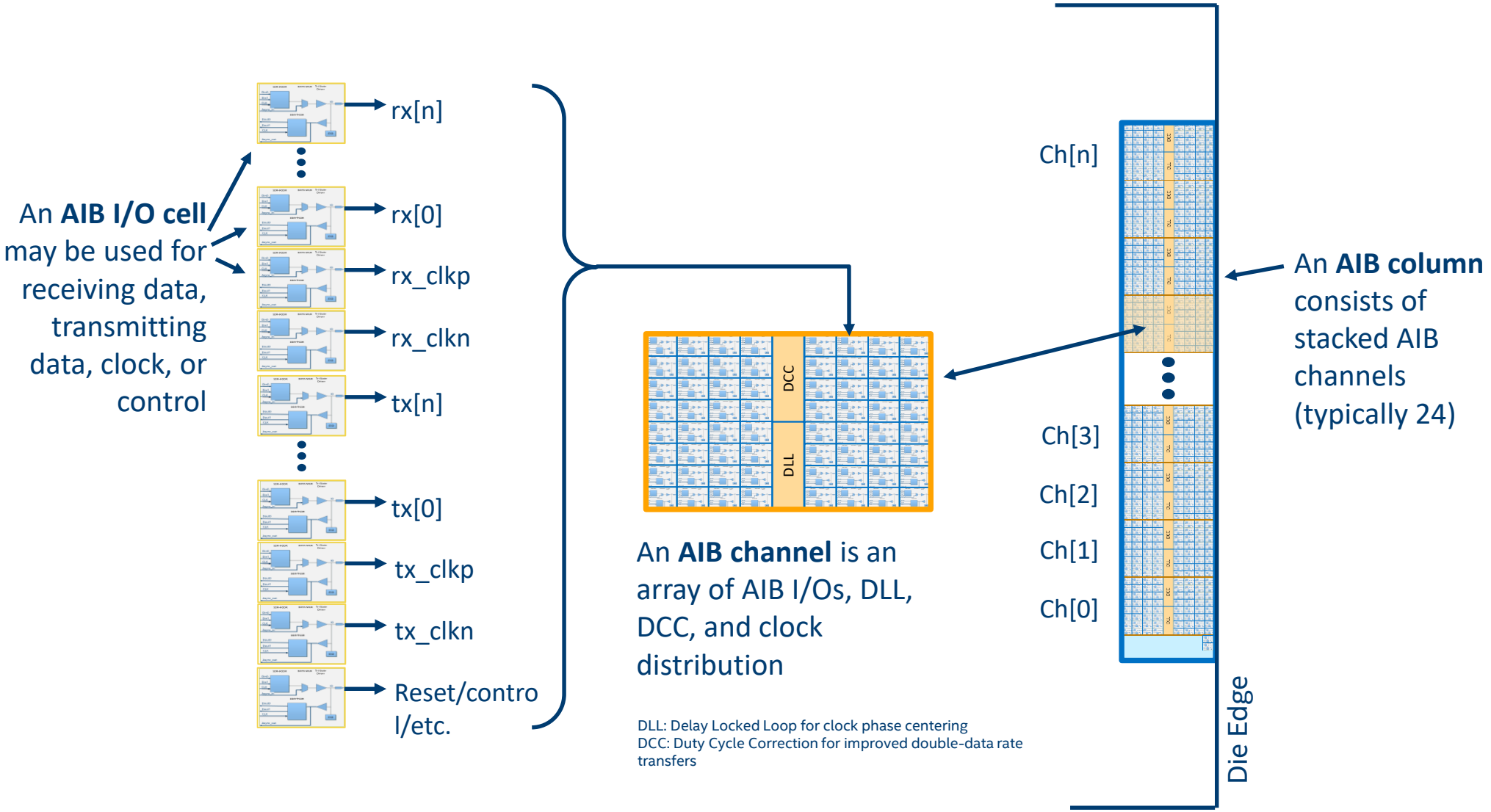
- F-Tile 112 Gbps serializer /deserializer (SERDES)
- P-Tile PCI Express* (PCIe) Gen4
- R-Tile PCIe Gen5 and Compute Express Link* (CXL)
- Custom intellectual property (IP) via Intel® eASIC™



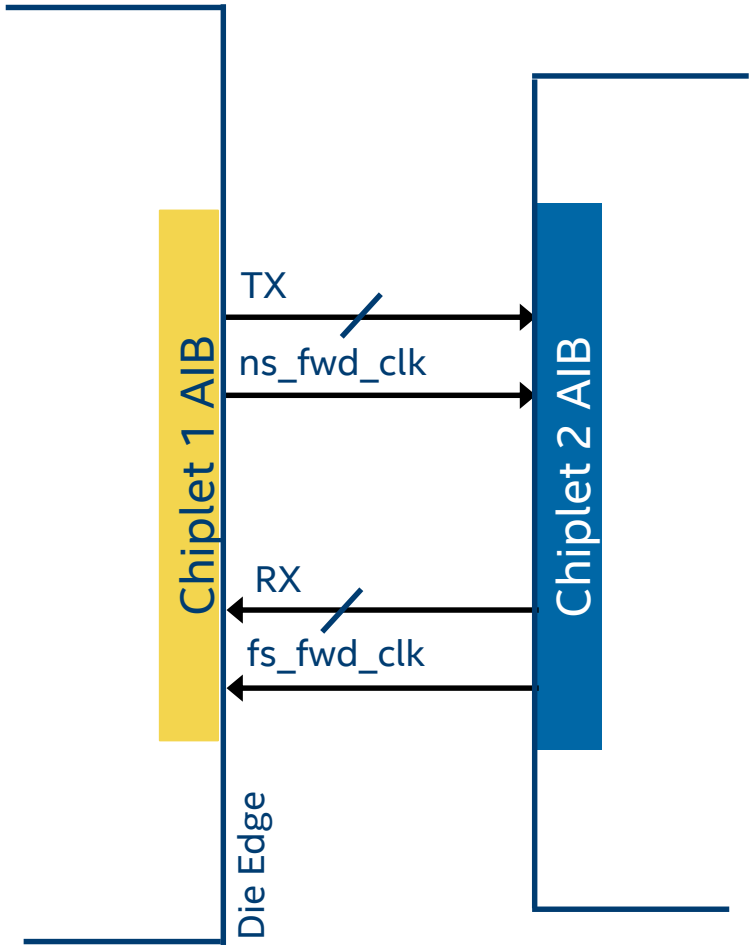
Industry adoption

- Jariet Technologies 64Gsamples/s ADC/DAC chiplet
- Ayar Labs photonics chiplet
- *Others coming soon*

AIB I/O Cell, Channel, and Column



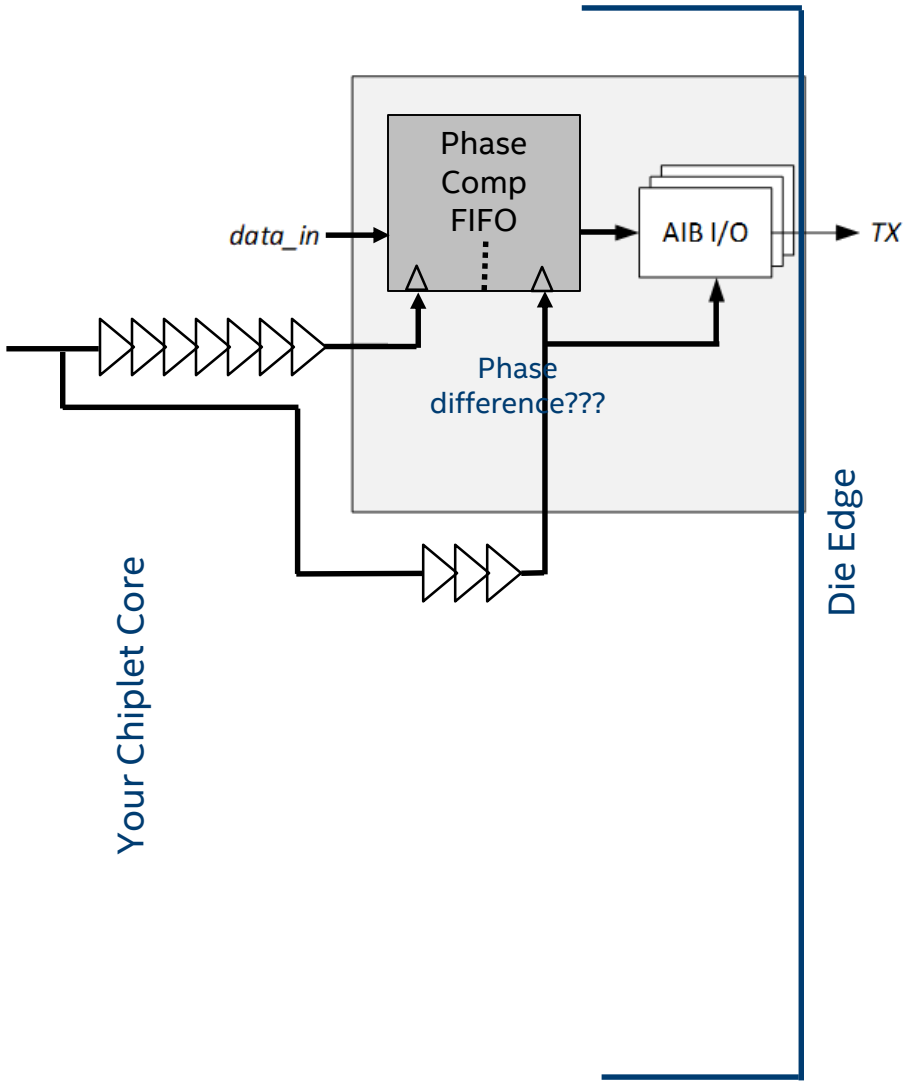
Simplest AIB Clocking Configuration (One Channel)



Each chiplet originates its own clock for transmitting to the other side

- Each channel can forward an independent clock or the same clock

Clocking Inside Your Chiplet



The clock distribution between your chiplet core and the AIB I/O may be a completely different tree, even when the clocks are the same source (0 PPM difference)

- *Mesochronous: same frequency, unknown phase*
- You need a phase compensation FIFO in this case

Channels

I have a 512 bit data bus each way. Why do I need to use channels?

A single transmit (TX) clock must be balanced to each TX I/O cell in the channel, same with receive (RX) clock

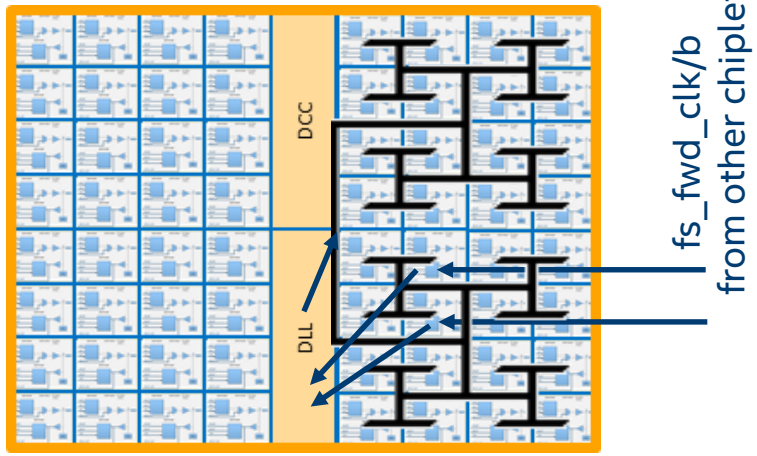
- Clock routing and controlling skew limit the number of I/Os per clock
- A wide bus will need to be spread across channels

Pick too many I/Os per channel, then:

- You waste I/Os in low-bandwidth applications like Gigabit Ethernet

Pick too few I/Os per channel then:

- You have to spread most higher bandwidth links across more than one channel



Example of AIB channel balanced clock distribution

AIB 2.0 Technology Drivers

Microbump spacing

- 55u is in production
- 35u provides a doubling of density.

I/O voltage

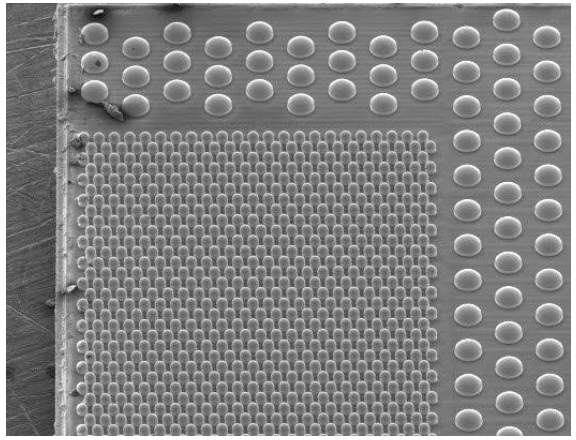
- 0.4V swing (down from 0.9V) to achieve <0.5pJ/bit

Line rate

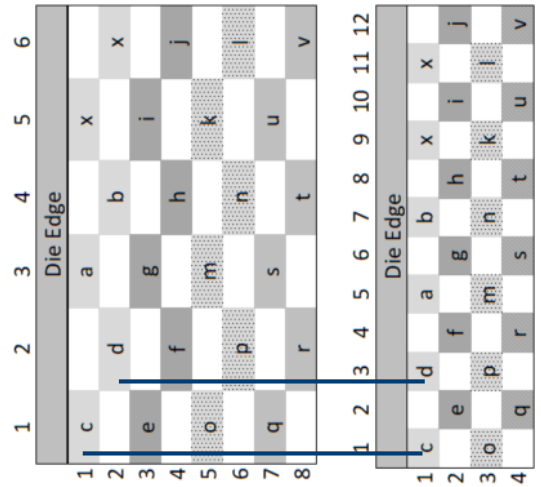
- Very high-bandwidth applications such as direct RF sampling analog-to-digital converters (ADCs) or digital-to-analog converters (DACs) will continue to push higher bandwidth
- Doubling the data rate to 4Gbps

Microbump spacing + I/O voltage + line rate → **AIB 2.0**

Tile backward compatibility and reuse is essential

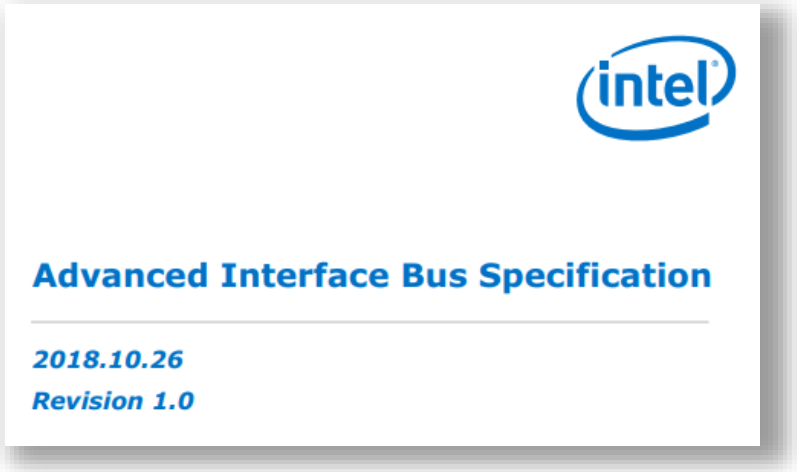


Intel® Stratix® 10 FPGA 55u microbump array



55u to 35u microbump assignment for straight-line routing compatibility

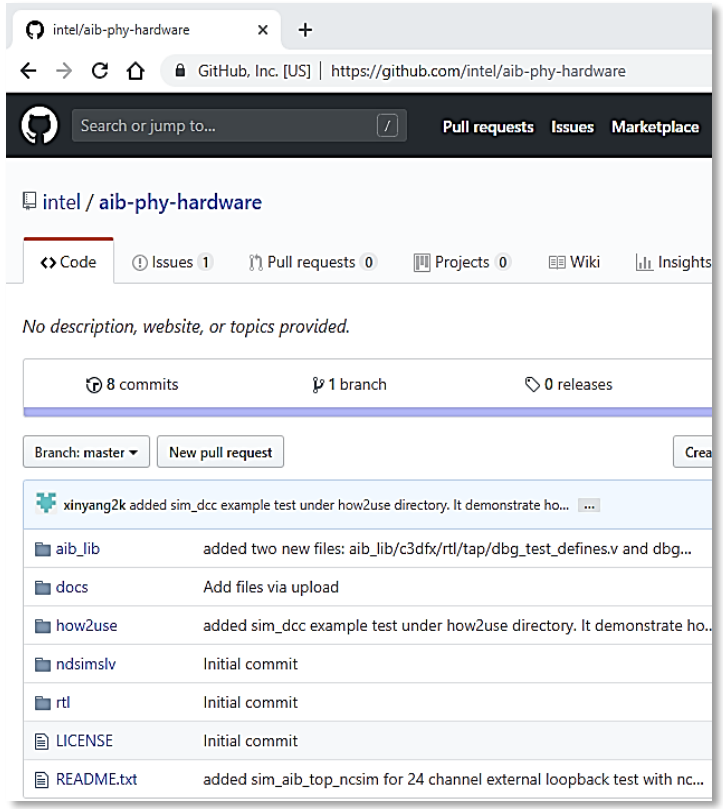
AIB Public Releases



AIB Specification Released October 2018

AIB Public Specification includes:

- Electrical specs, bump array mechanicals, data/clock/ control signal definitions, reset handshaking, JTAG reqts
- Available at https://github.com/intel/aib-phy-hardware/tree/master/docs

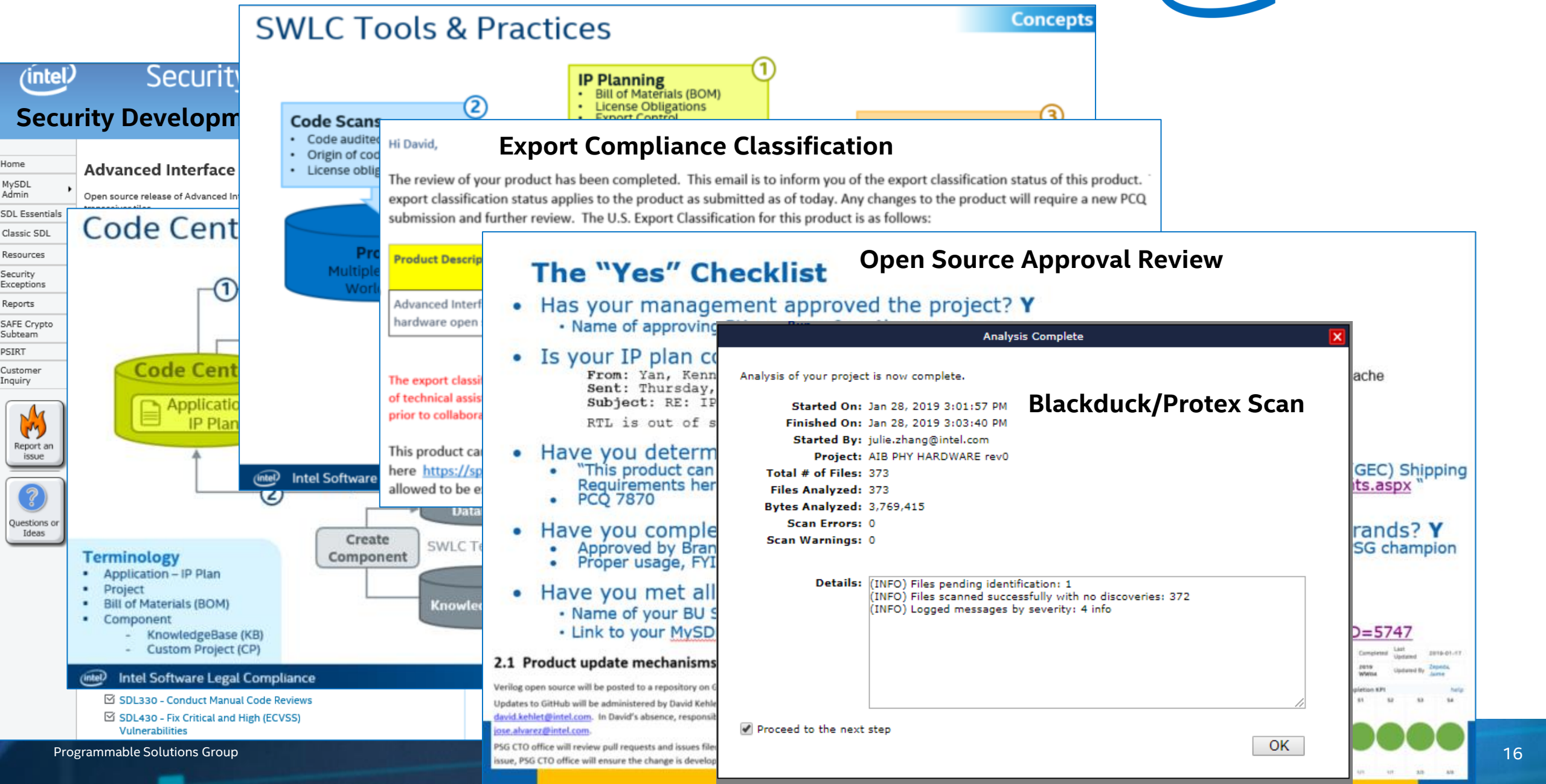


AIB Open Source Released January 2019

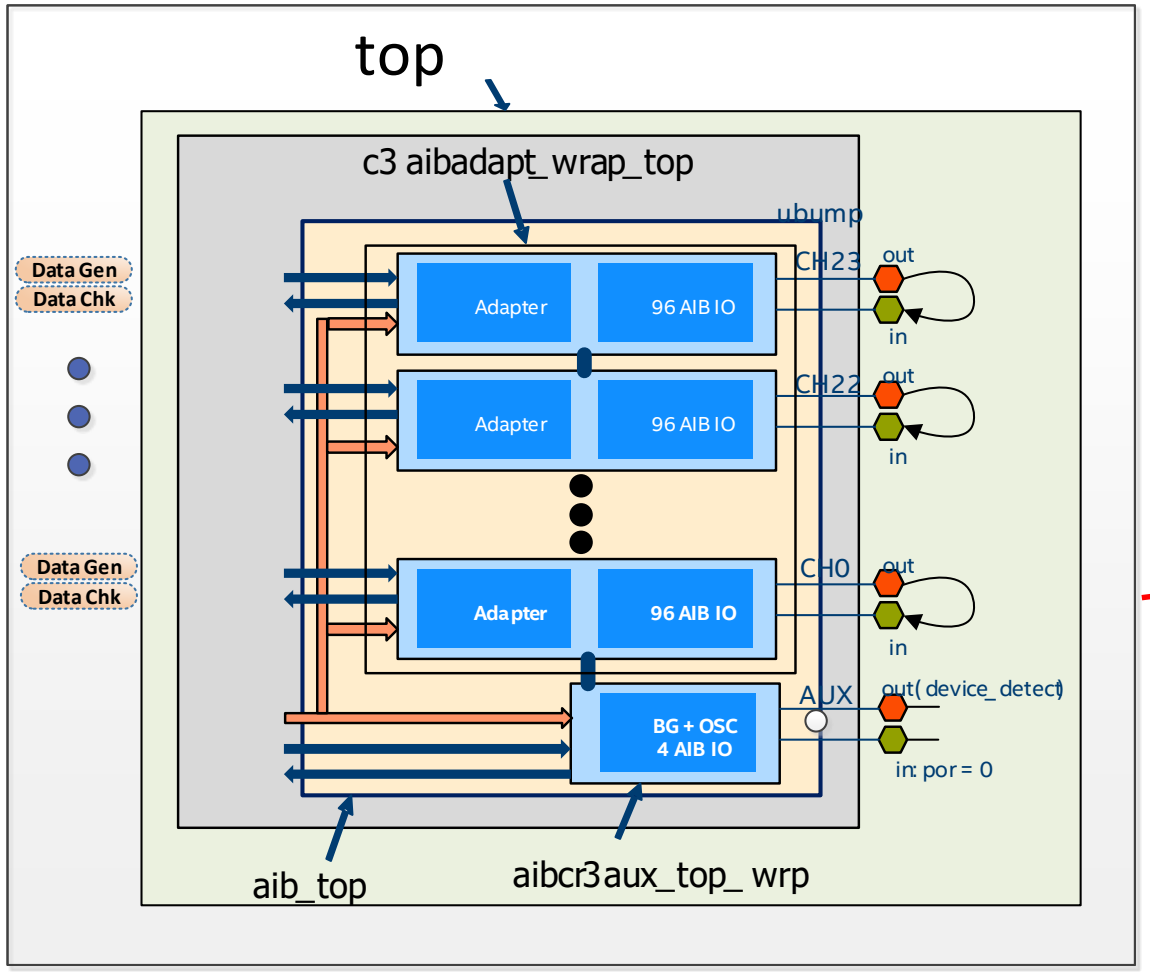
AIB Open Source on GitHub

- Register transfer level (RTL), netlists, generic cell library
- Available at https://github.com/intel/aib-phy-hardware
- Purpose: **reduce development cost**

Intel Open Source Process



Example of Testing 24 Channel AIB



intel / aib-phy-hardware

Code | Issues 0 | Pull requests 0 | Proj

Branch: master ▾ aib-phy-hardware / how2use /

xinyang2k added sim_modelsim under how2use directory. This is th

..

sim_aib_top	added how2use directory, ad
sim_aib_top_ncsim	added sim_aib_top_ncsim for
sim_dcc	added sim_dcc example test u
sim_modelsim	added sim_modelsim under h
sim_phasecom	added sim_phasecom simulat
README.txt	added sim_modelsim under h

Generic Cells

```
// SPDX-License-Identifier: Apache-2.0
// Copyright (C) 2019 Intel Corporation. All rights reserved
// ******************************************************************************
// ******************************************************************************
// Copyright © 2016 Altera Corporation. All rights reserved.  Altera products are
// protected under numerous U.S. and foreign patents, maskwork rights, copyrights and
// other intellectual property laws.
// ******************************************************************************
//  Module Name :  c3lib_and2_svt_4x
//  Date        :  Thu Sep 15 13:44:58 2016
//  Description :  2-input AND gate (SVT, 4x drive strength)
// ******************************************************************************

module c3lib_and2_svt_4x(

  in0,
  in1,
  out

  );

input           in0;
input           in1;
output          out;

  assign out = in0 & in1;

endmodule
```

Open Source has a behavioral model for this AND gate

A user should replace this with a PDK-specific cell

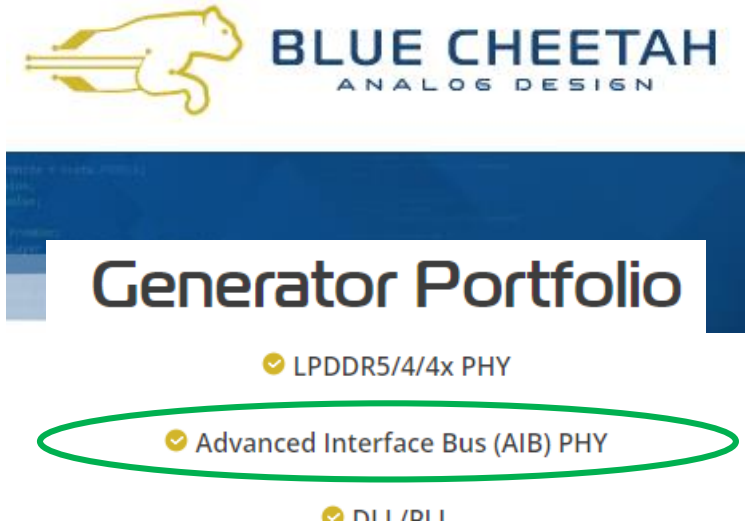
AIB IP Generation Project: Intel and Blue Cheetah

Technology and design flow to create physical designs from specifications and circuit generators

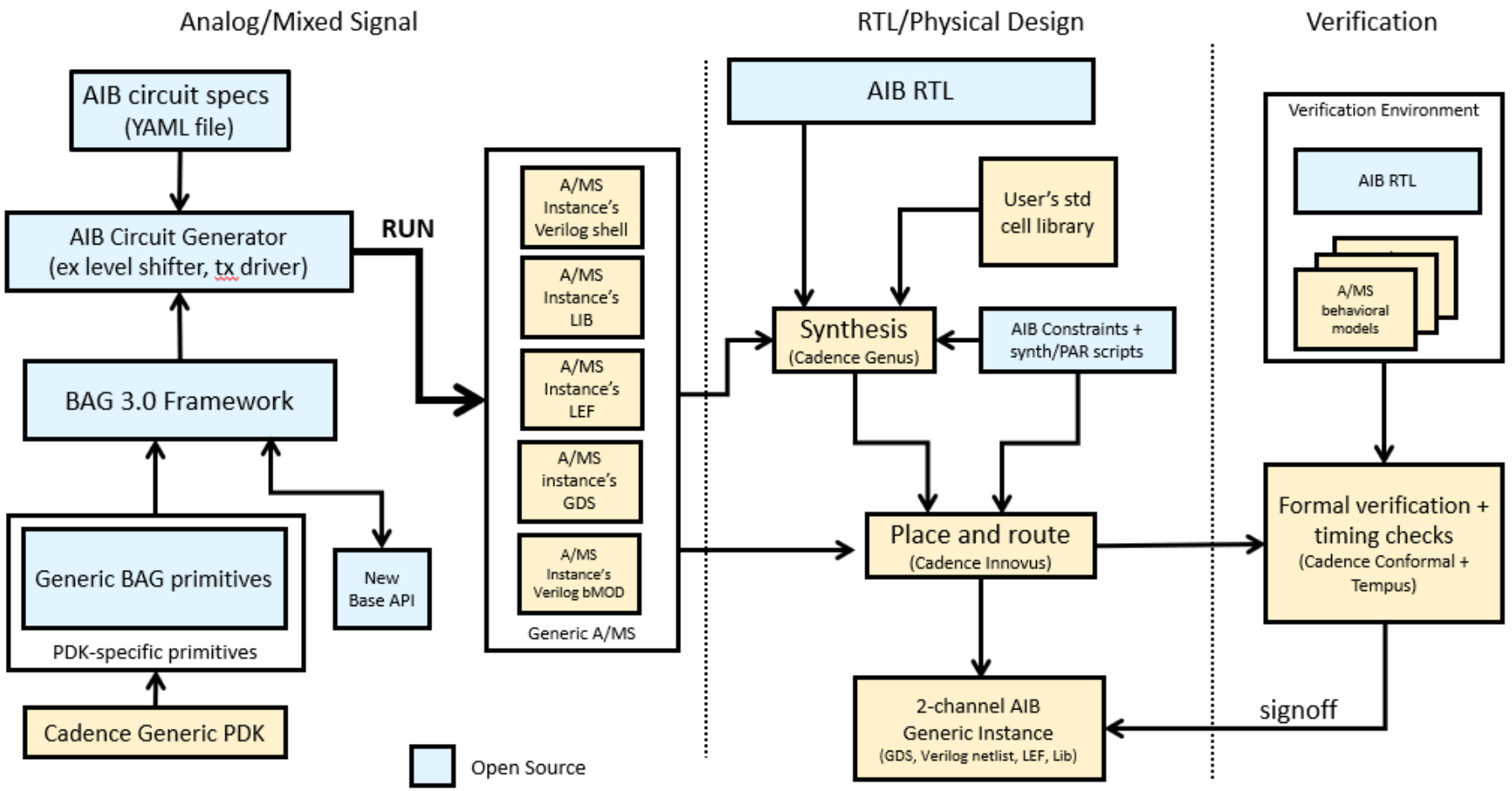
Uses Berkeley Analog Generator 3.0

Potential dramatic reduction in porting labor

Developed specifications and generators for AIB using Intel 22FFL PDK



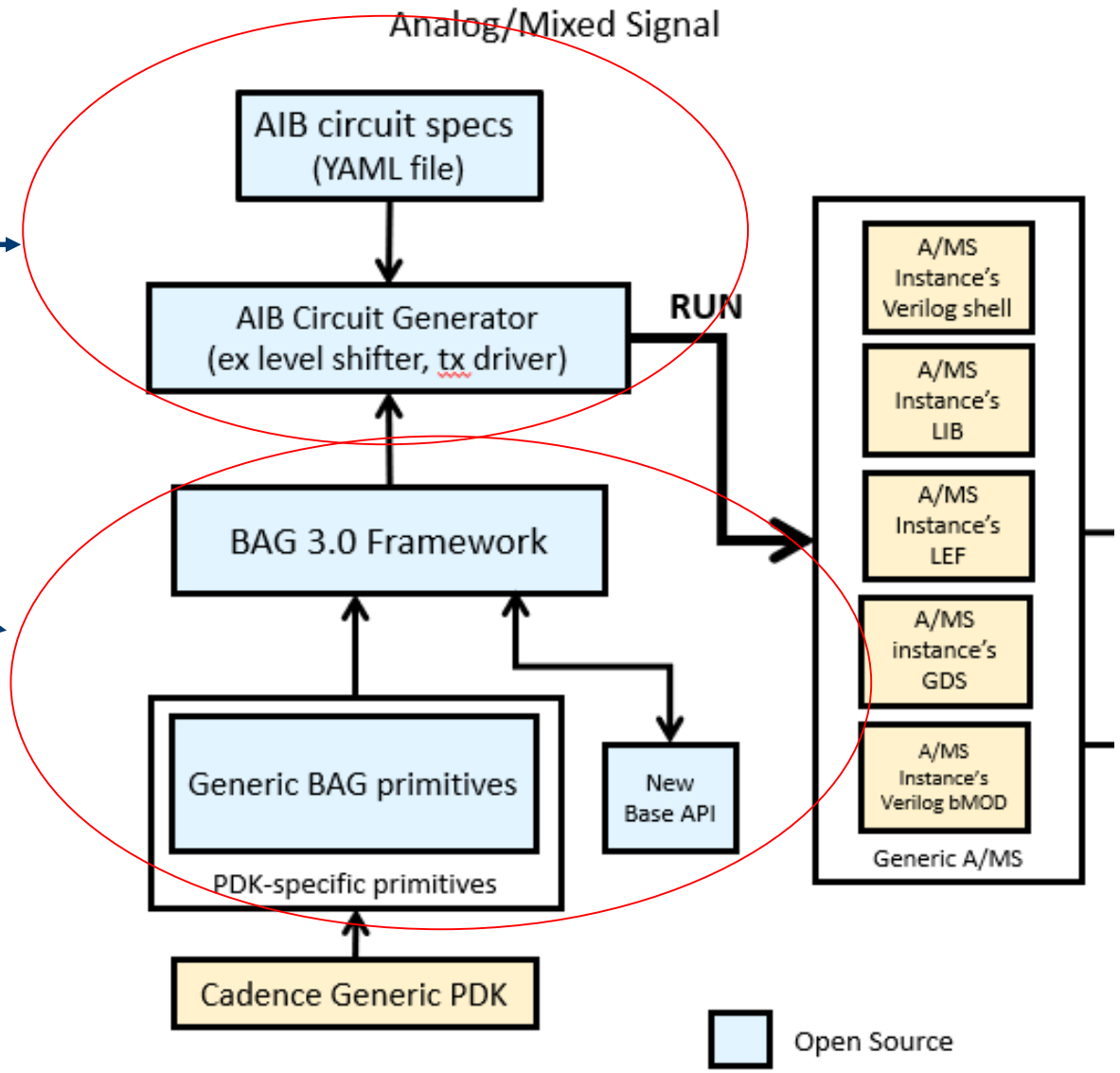
AIB Generator Design Flow with Generic PDK



AIB Generator

AIB specific: AIB Circuit Specs, AIB Circuit Generator

Generic: BAG 3.0 Framework, Generic BAG primitives, New Base API

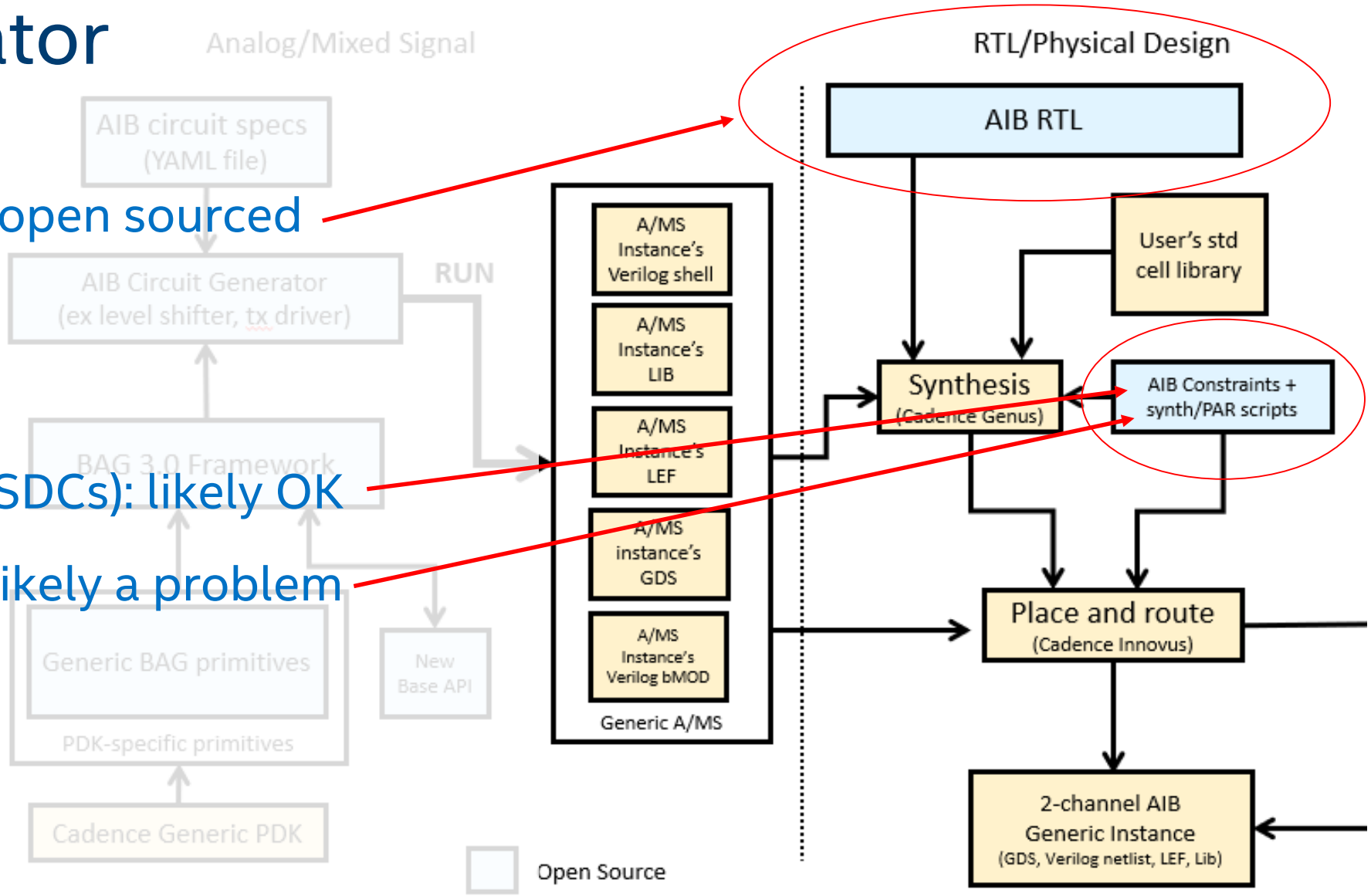


AIB Generator

AIB RTL: already open sourced

AIB Constraints (SDCs): likely OK

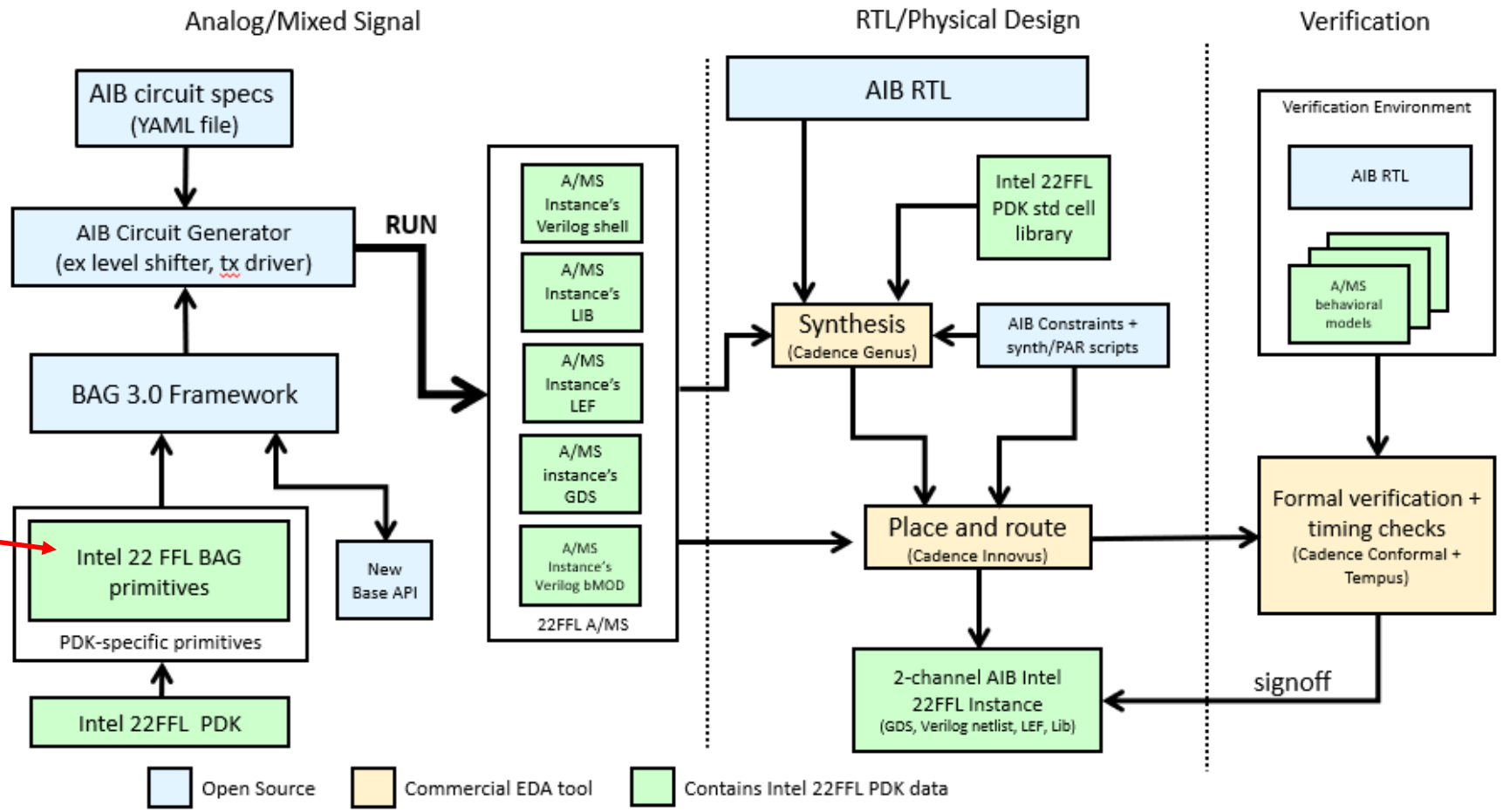
AIB PAR scripts: likely a problem



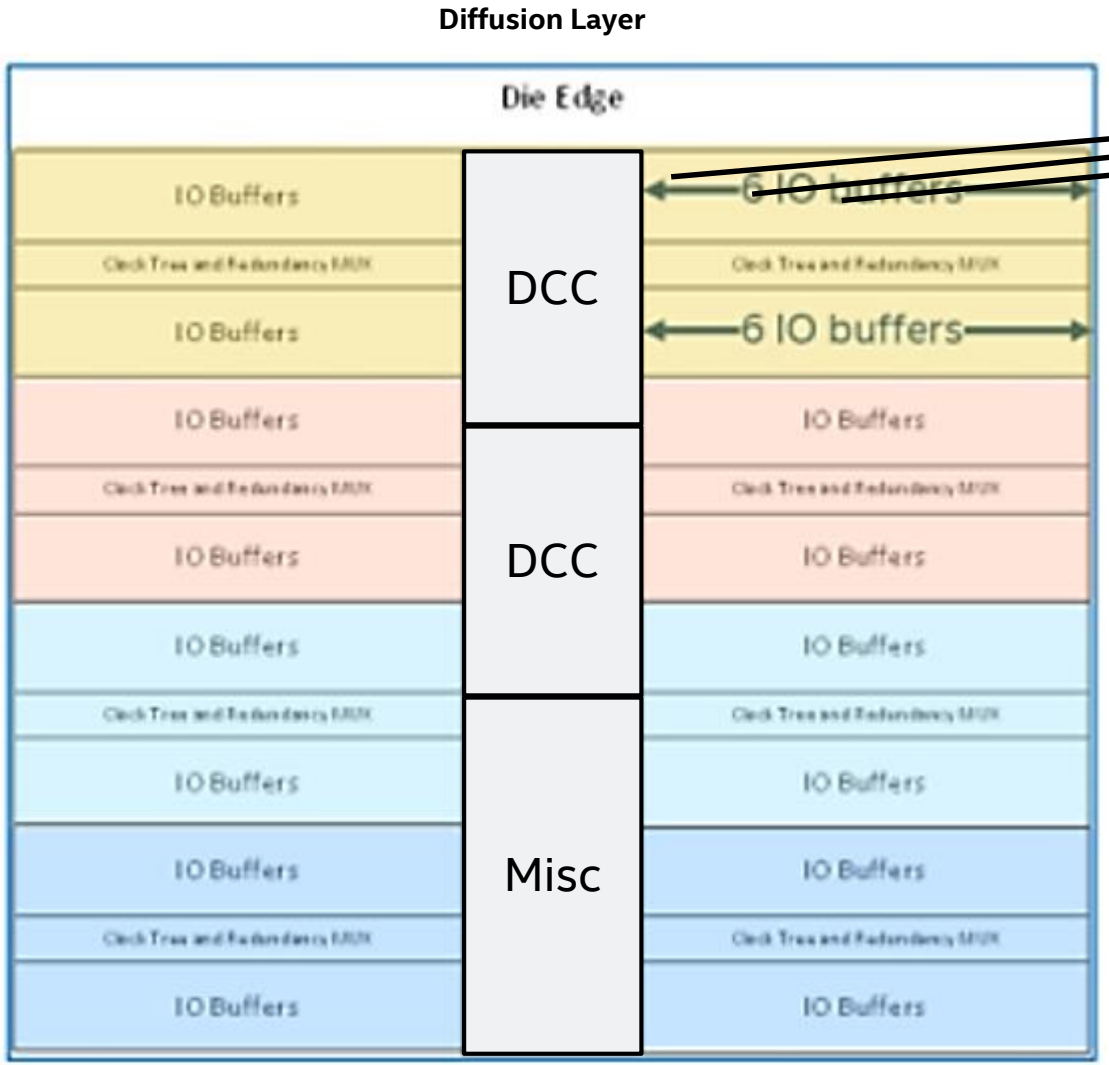
AIB Generator Design Flow with Intel 22FFL PDK

Open source flow works, even though we cannot open source anything with Intel PDK data

"Secret sauce" is in the "Intel 22FFL Bag primitives"



IO Cell Placement and Microbump Routing



	1	2	3	4	5	6
	Edge of Chiplet					
A	VCCIO		VCCIO		VCCIO	
B		VCCIO		VCCIO		VCCIO
C	VCCIO		VCCIO		VCCIO	
D		VCCIO		VCCIO		VCCIO
E	VSS		VSS		VSS	
F		VSS		VSS		VSS
G	AIB16		AIB41		AIB2	
H		AIB12		AIB8		AIB46
I	AIB17		AIB40		AIB3	
J		AIB13		AIB9		AIB47
K	AIB18		AIB10		AIB4	
L		AIB14		AIB6		AIB0
M	AIB19		AIB11		AIB5	
N		AIB15		AIB7		AIB1
O	AIB44		AIB30		AIB24	
P		AIB34		AIB43		AIB20
Q	AIB45		AIB31		AIB25	
R		AIB35		AIB42		AIB21
S	AIB38		AIB32		AIB26	
T		AIB36		AIB28		AIB22
U	AIB39		AIB33		AIB27	
V		AIB37		AIB29		AIB23
W	VSS		VSS		VSS	
X		VSS		VSS		VSS
Y	VCCD		VCCD		VCCD	
Z		VCCD		VCCD		VCCD
AA	AIB57		AIB87		AIB93	
AB		AIB64		AIB83		AIB66
AC	AIB59		AIB86		AIB92	
AD		AIB65		AIB82		AIB67
AE	AIB51		AIB78		AIB71	
AF		AIB80		AIB89		AIB68
AG	AIB52		AIB79		AIB70	
AH		AIB81		AIB88		AIB69

Redistribution to Microbumps

CHIPS Meets POSH&IDEA

Test Chip Using AIB IP Generator Technology

- 12/2019 AIB Generator test chip “tape in”
- Q1 2020 Intel 22FFL internal shuttle

We would like to thank **Mr. Andreas Olofsson** for his support.

This work is supported by the **DARPA MTO office.**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