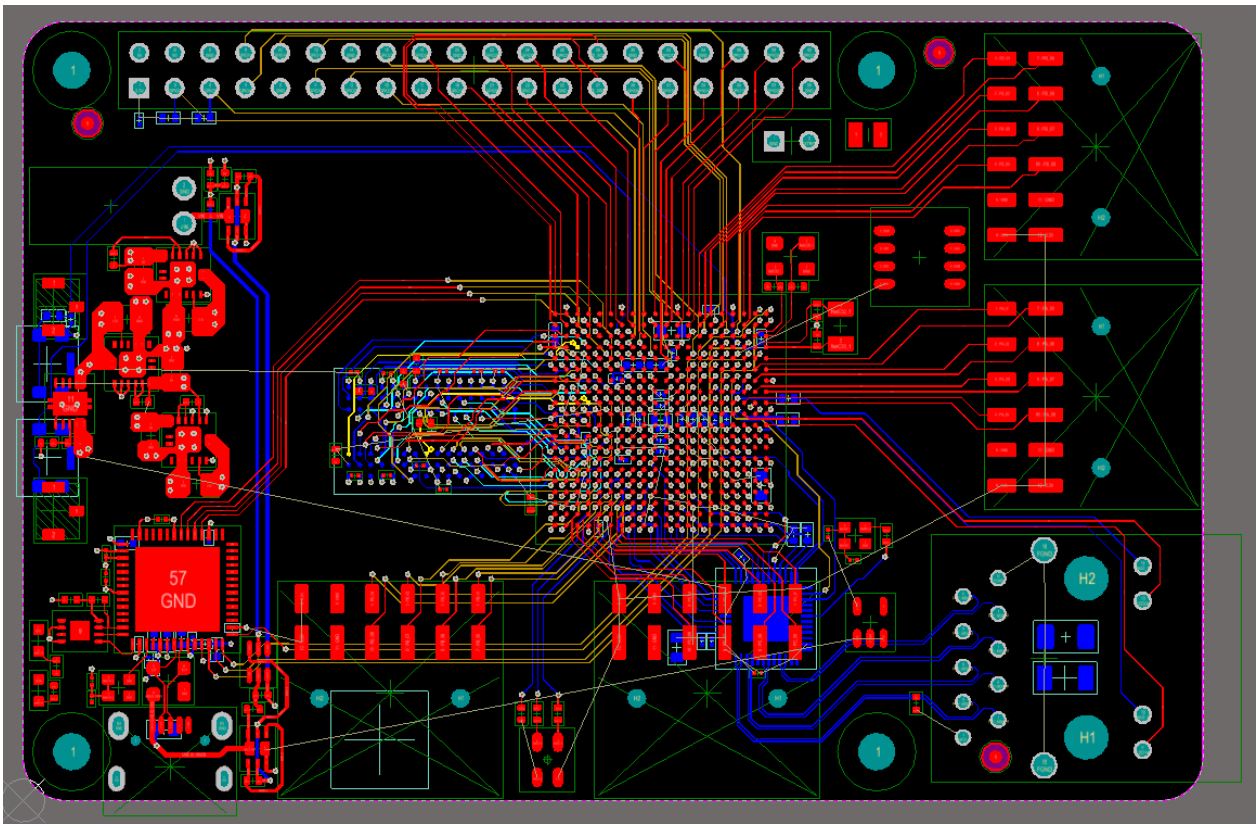
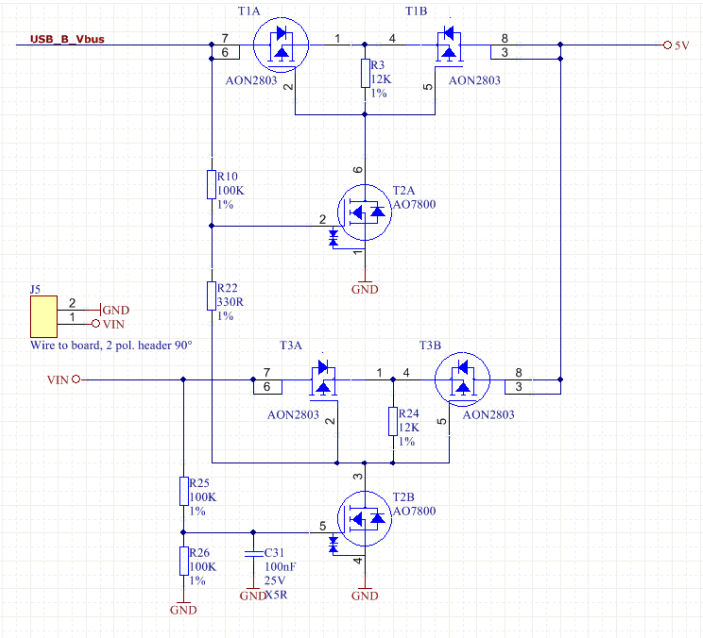
# PCB Design Review

PCB as received from PCB Engineer

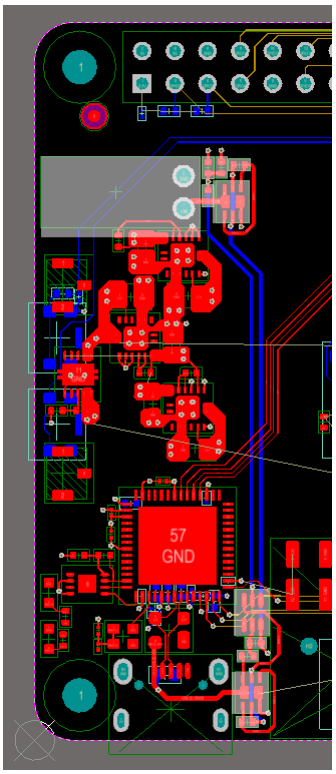


## Issue #1

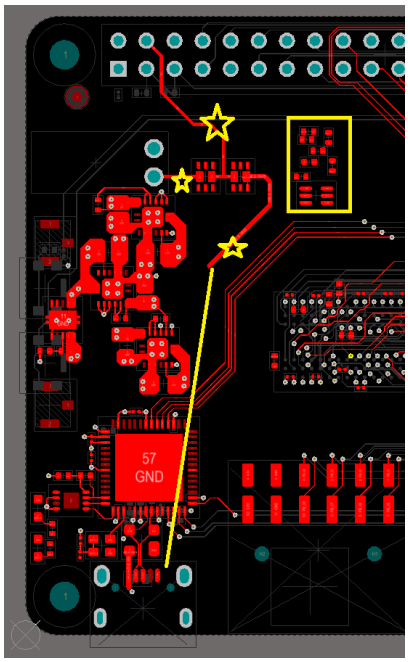
Placement and wiring of Power Switch components




Those components build a simple 2 to 1 Power select switch, two inputs and one output.



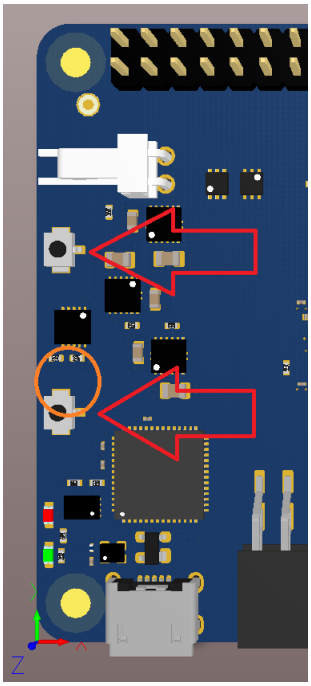

This is how the components are placed, notice the blue bottom side POWER traces!



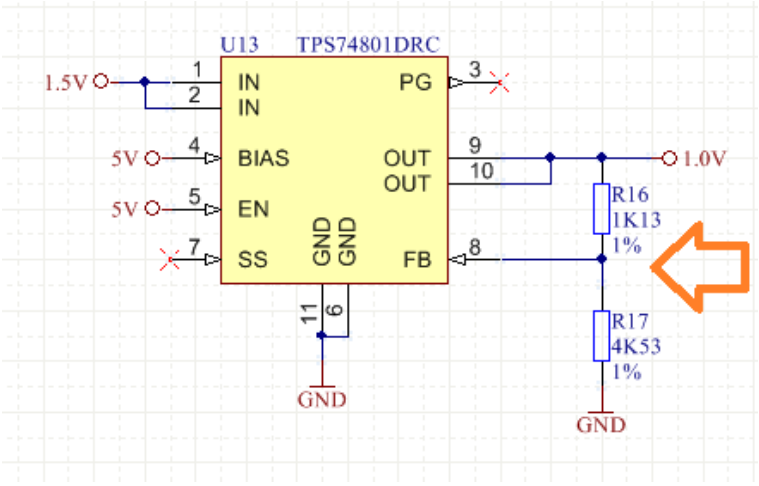

This is pre-placement for the two power switches, all wires carrying power are marked with yellow. In the yellow box are additional components that do not carry any current and are not as important as of placement and routing.

## Issue #2

Placement of components too close to user interface – there are two push-buttons, where it would be better to have more clearance so the fingertips would not touch any electronic components.



Marked with orange is “fingertip” pressing the button and touching LDO feedback resistors!

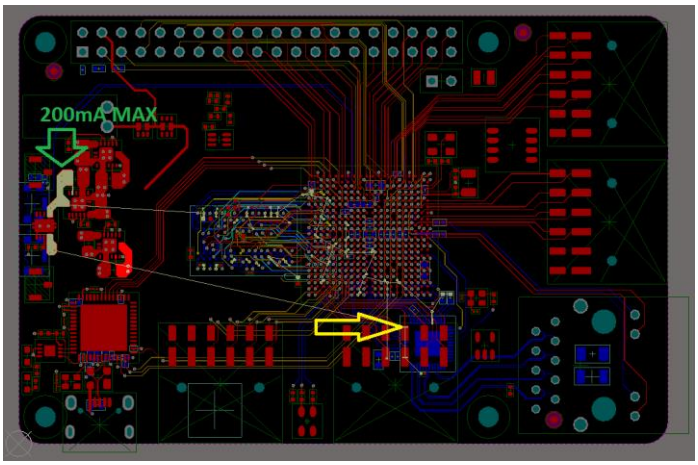



This is where you would touch the feedback pin of the LDO, the most sensitive pin that can cause the output voltage to change and potentially damage some more components.

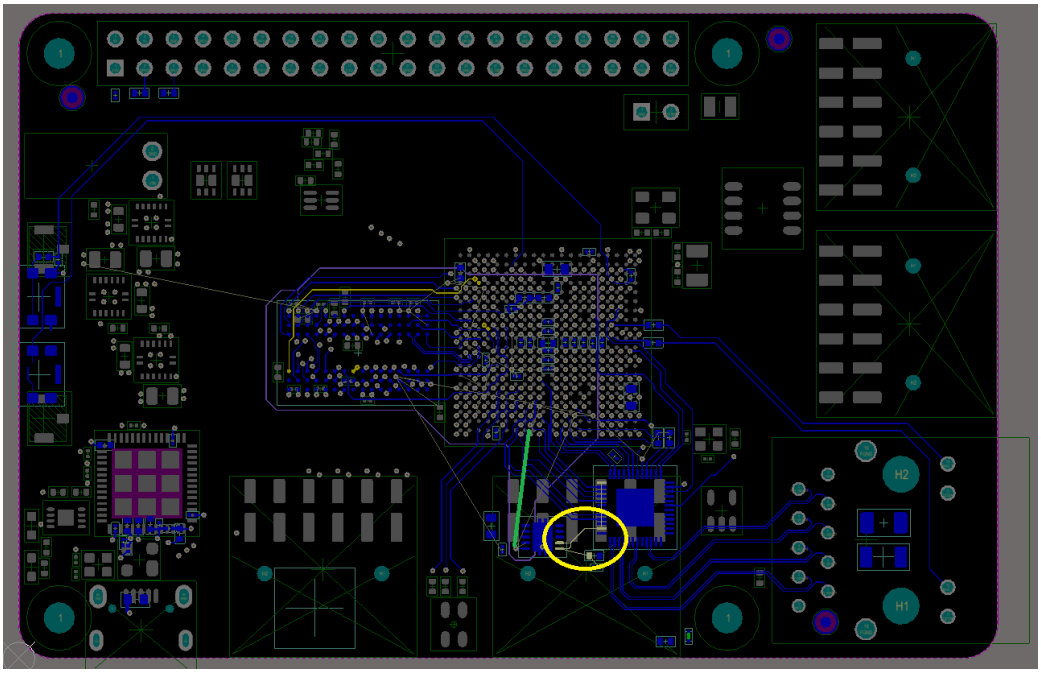
There was no need to place the LDO that close to the buttons!

## Issue 3#

Placement of 1.0V LDO



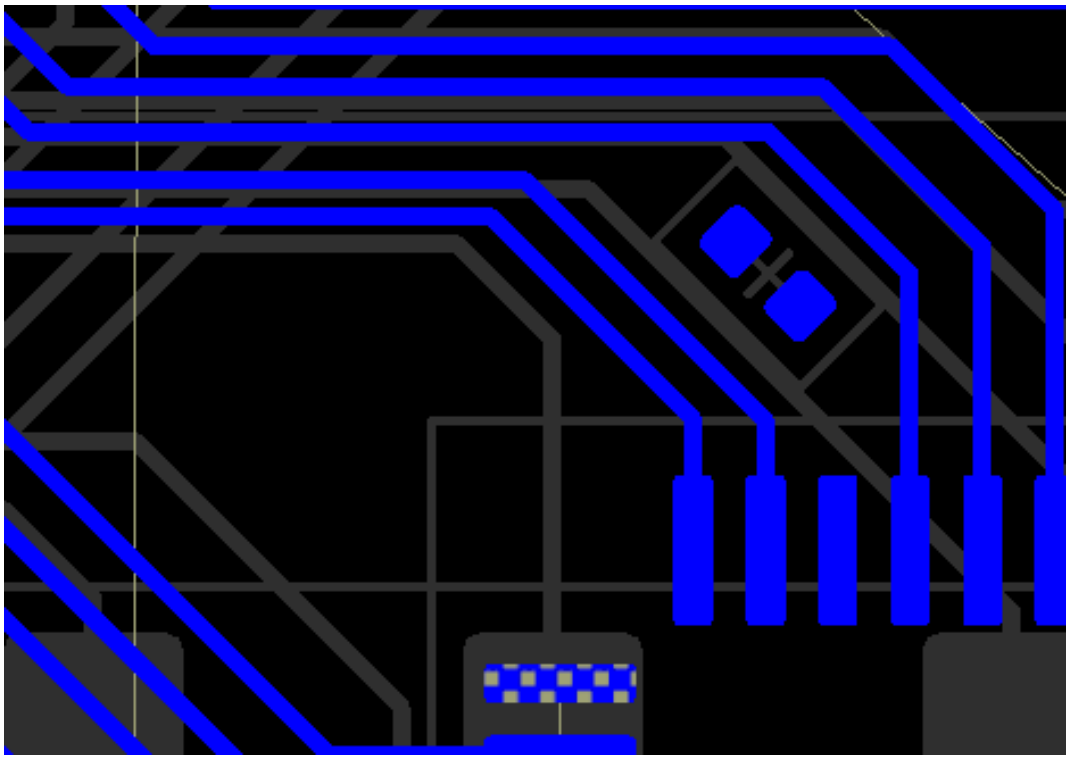

Yellow marks where the Ethernet PHY needs the 1.0V that is powering also sensitive analog circuits, so placing the LDO closer would be also better as of noise coupling. Green marks where the PCB designed did draw a POLYREGION for power signals that can carry maximum of 200mA (typical 95mA). There is no need for polygons for power nets that do not carry significant currents.




Changed Placement: the LDO is placed to the current consumer Ethernet PHY (1.0V connections inside the yellow marking). Green marks the additional current path from 1.5V polygon below the main IC in the middle of the PCB to the input of the LDO.

## Issue #4

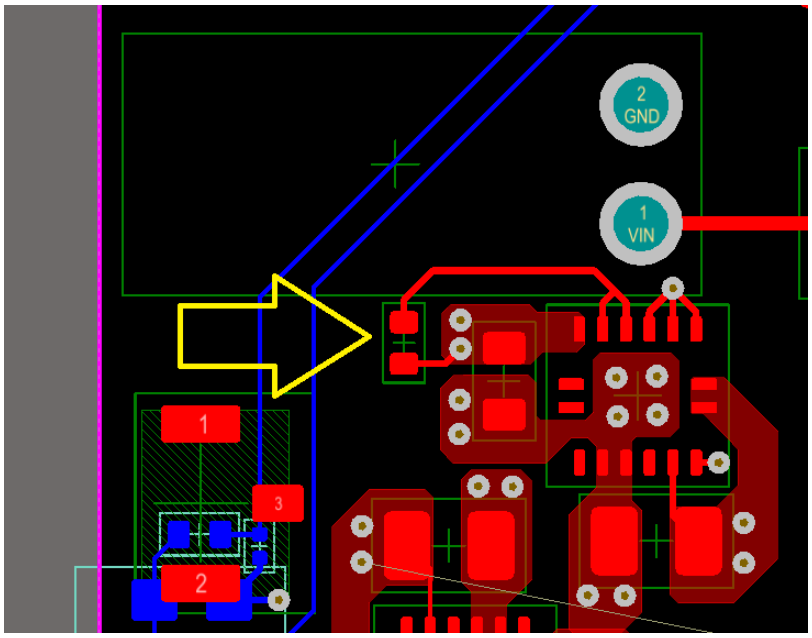
Rotation 45 degrees!?



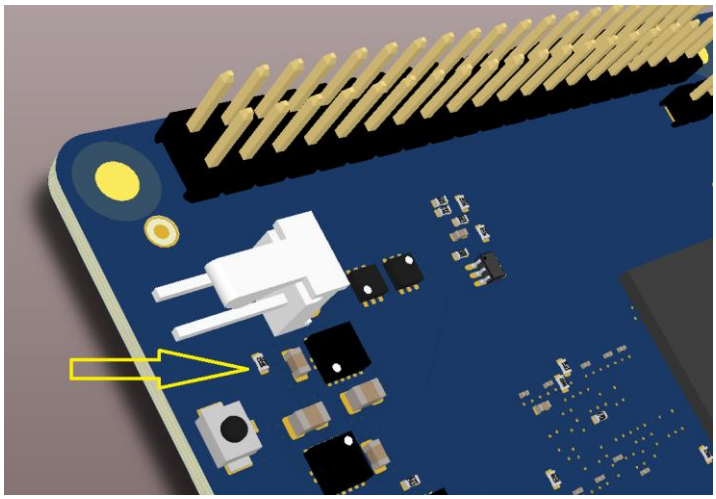
Only one single component has been rotated by 45 degrees. While assembly at 45 or any other angle is possible it should really if avoided if not really needed.

## Issue #5

SMD component too close to connector, potential damage when inserting cable/connector.




Component by arrow is moved to not collide with connector courtyard, so it looks like legal placement.

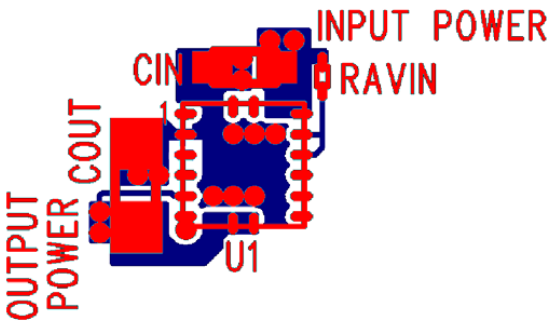


This is how it looks in 3D View, it is clear that there is a danger that connector when plugged in could damage the resistor! And there is absolutely no need to place that resistor so close to the connector.

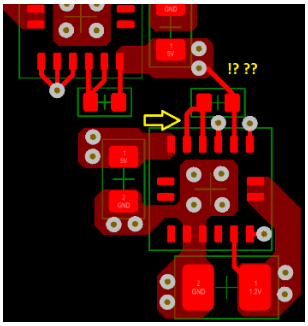
## Issue #6

AVIN routing issue #1

EP53A7 Datasheet gives recommendations and also recommended placement and routing.

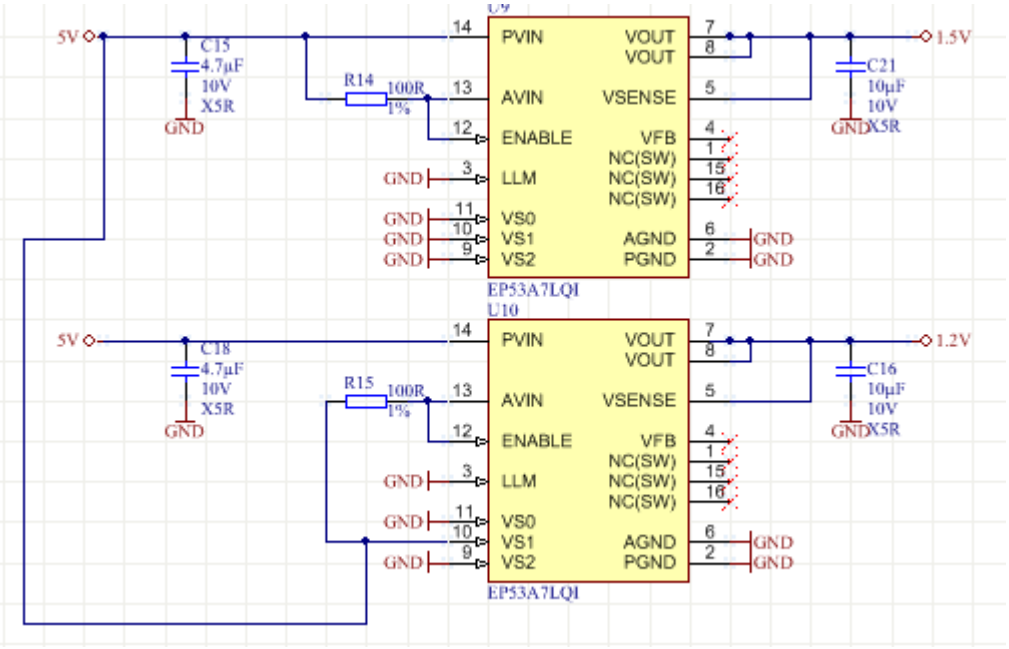



This is IC vendor recommended PCB layout.



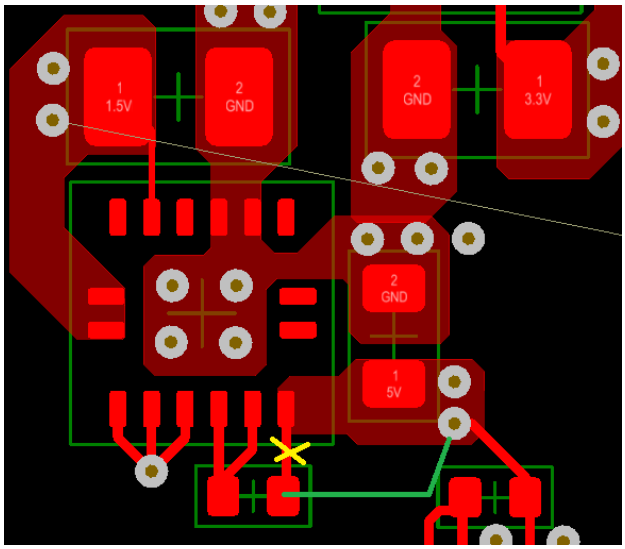

Marked yellow is AVIN input that as per recommendation has to be connected to VIN at Quiet point as visible in the recommended layout. The PCB designer however connected the AVIN first to VID1 and then to VIN of different DCDC converter!

This is how his work would be in “back annotated” schematic:



## Issue #7

AVIN routing issue #2

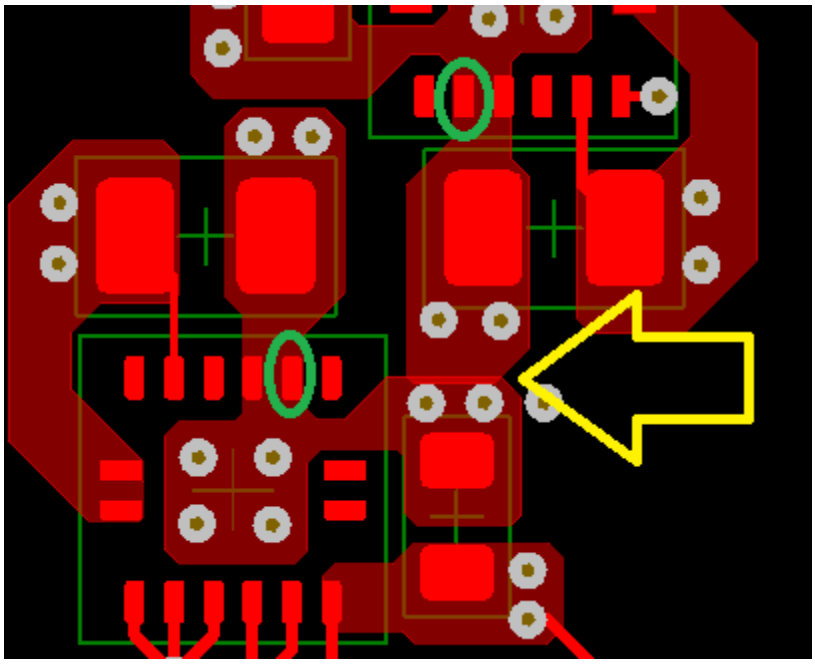



AVIN routing at second DCDC also incorrect, marked green is where the AVIN connection should be.

Third DCDC AVIN connection looks correct, but this is not because PCB engineer did know what or why he is doing, no he had to move the AVIN resistor to correct place because there was a connector that did not allow it to be at wrong place! So it was co-incidence that one AVIN from DCDC was wired correctly.

## Issue #8

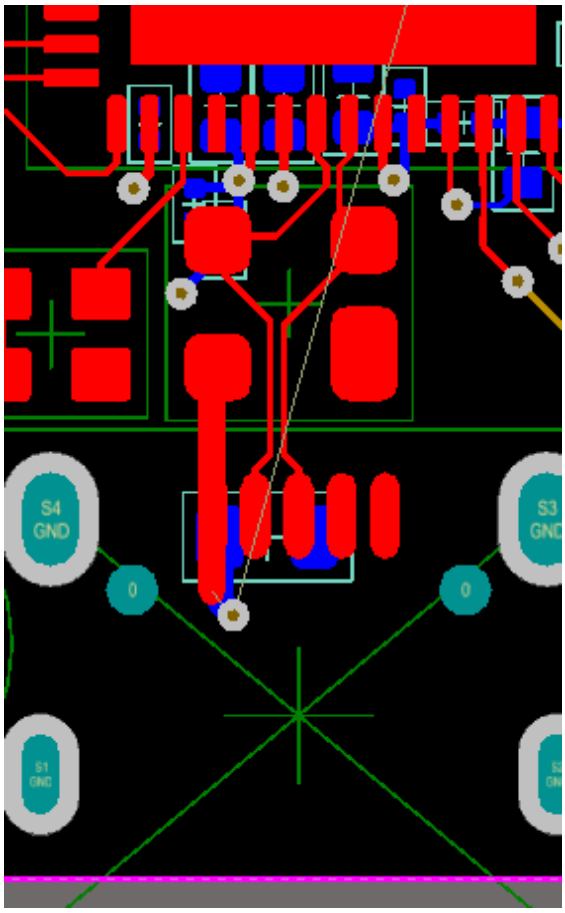
Incorrect GND connection



GND of VIN Capacitor from one DCDC is with direct top layer copper connected to GND point of VOUT capacitor of another DCDC. In datasheet: Input and output grounds should only connect at PGND pin (marked green).

## Issue #9

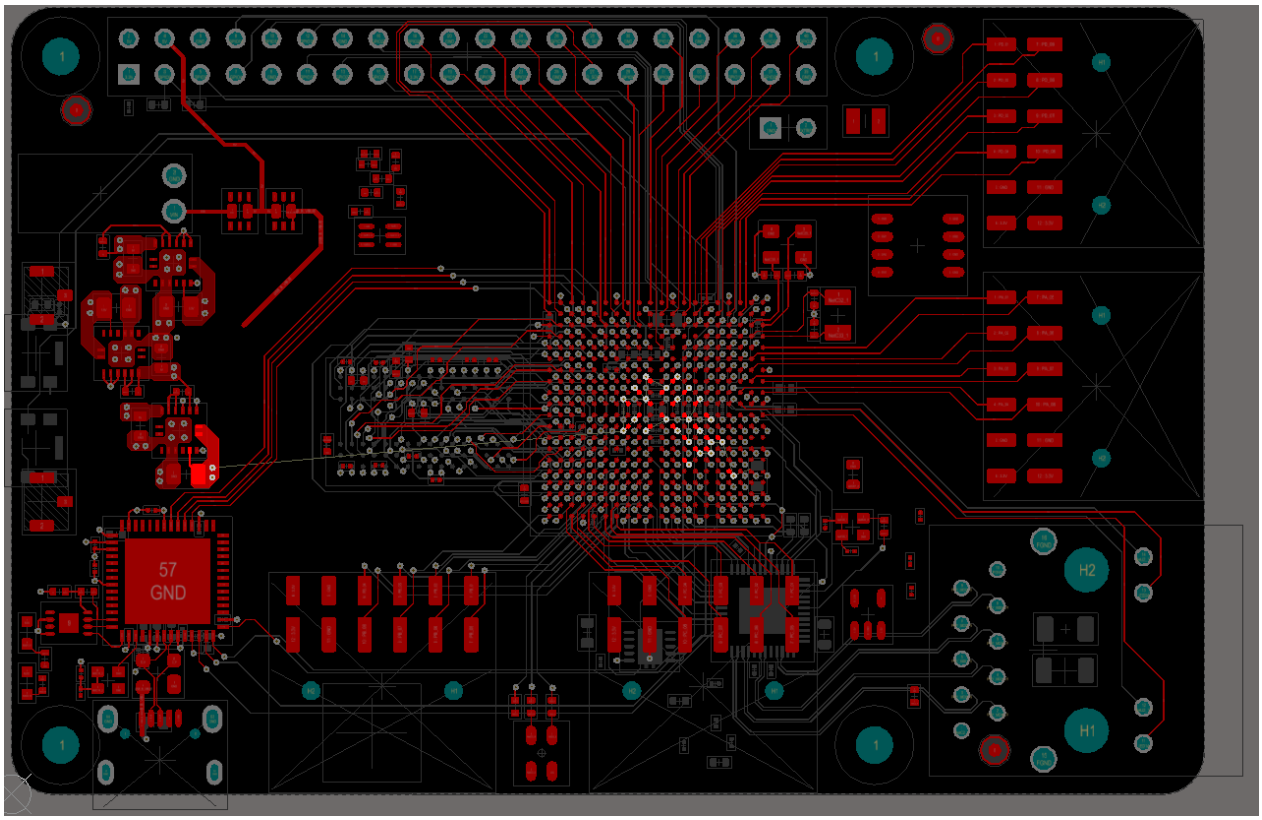
Differential routing




This looks nasty, could be improved.

## Issue #10

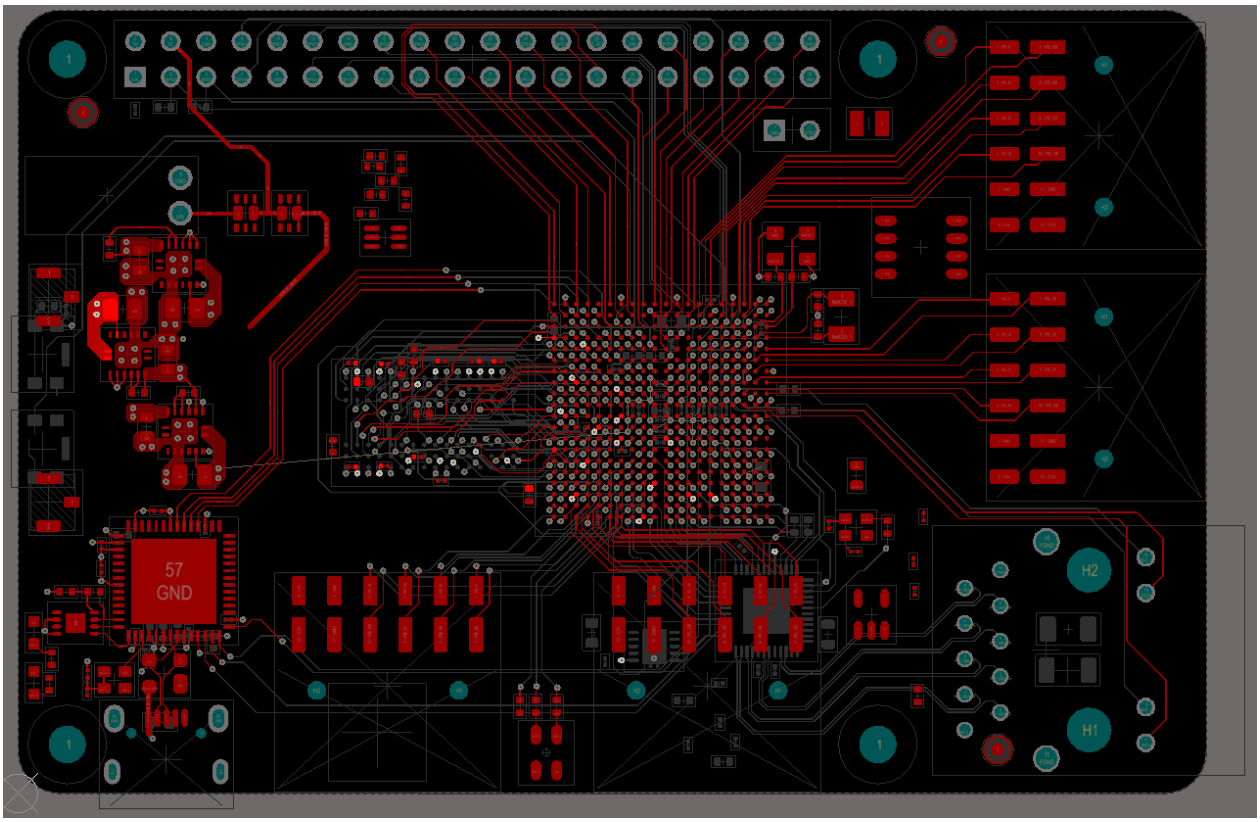
Bad placement for FPGA Core Voltage DCDC regulator.




DCDC Regulator could be placed much closer to where the current is needed, as is the 1.2V core supply current must go all the way below DDR3 memory to reach the middle of the FPGA BGA Package.

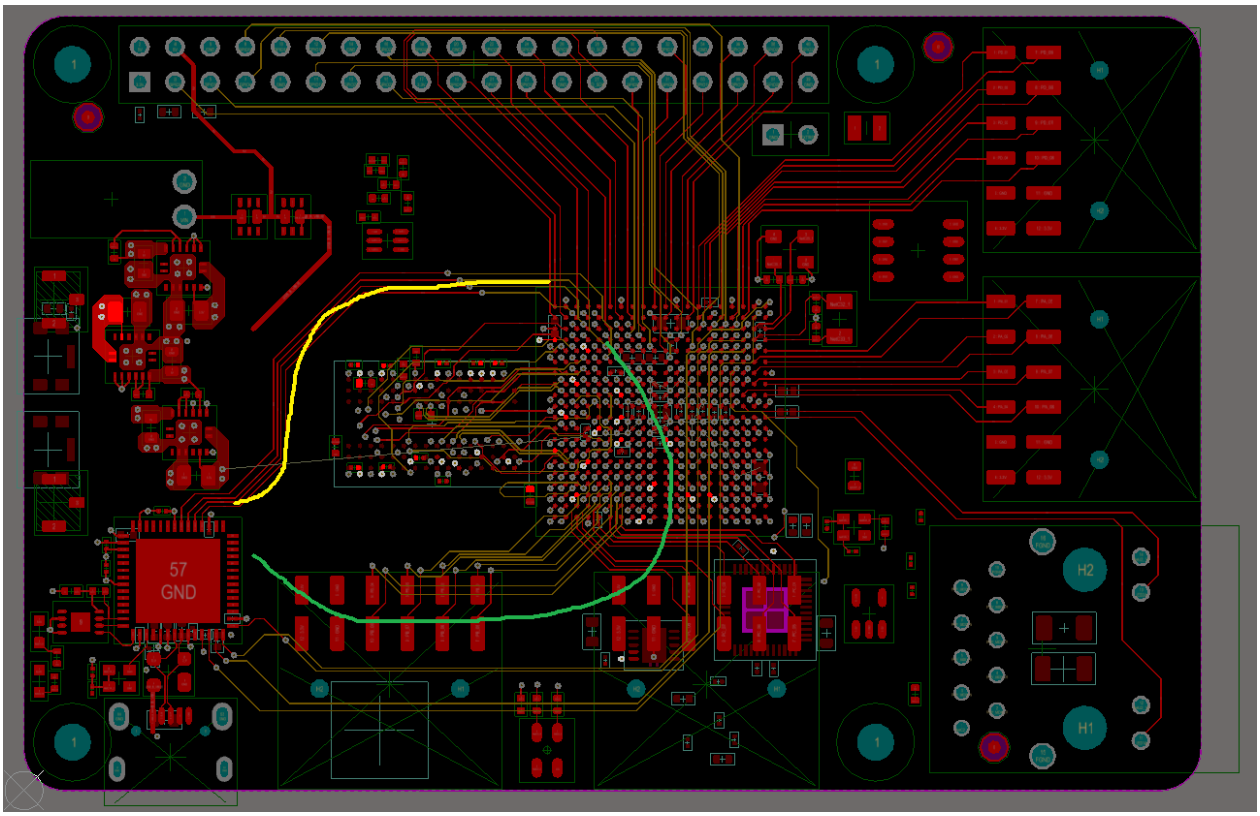
## Issue #11

Bad placement of 1.5V DCDC Regulator



## Issue #12

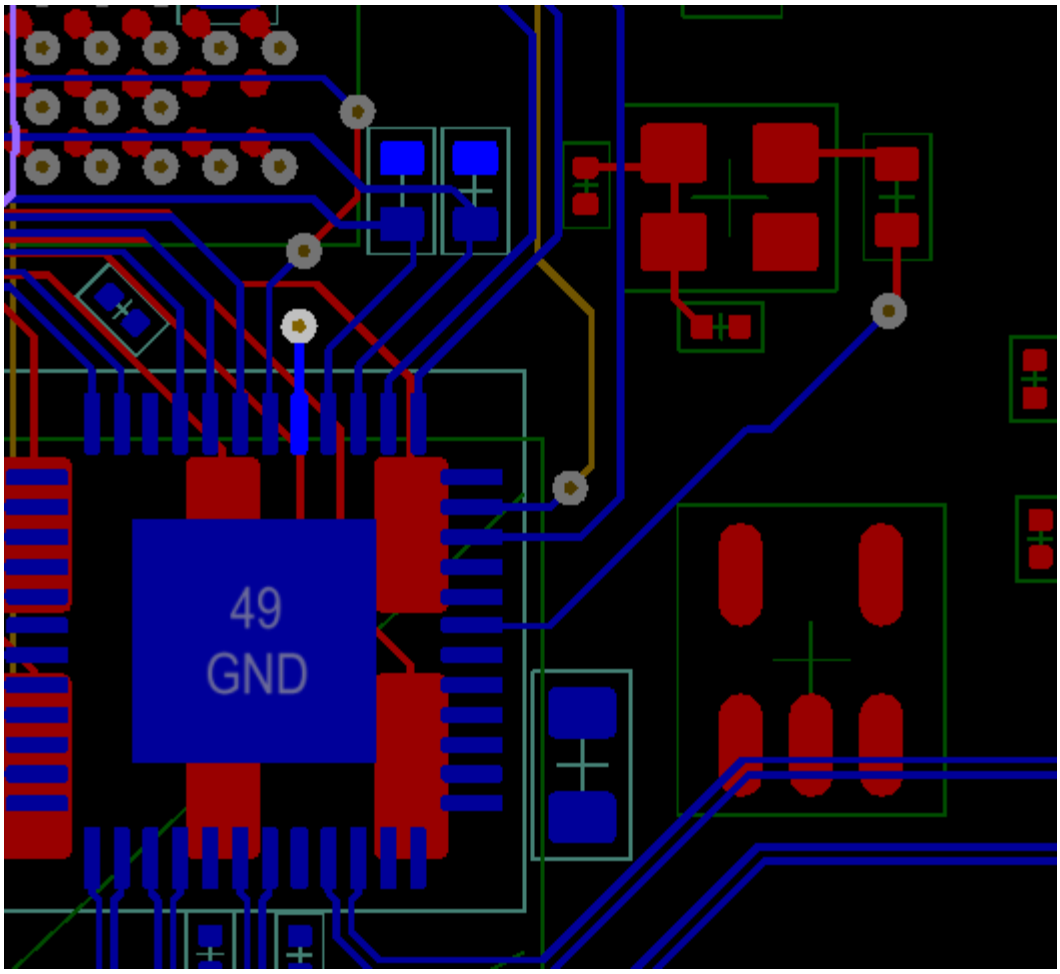
Routing priority, minor




Marked yellow are traces from PCB engineer, marked green are same traces in inner layer, leaving all the routing resources and TOP layer placement around the yellow line free.

## Issue #13

Placement/routing




Oscillator (the IC with 4 PADs in the top right corner) could be placed in the bottom layer