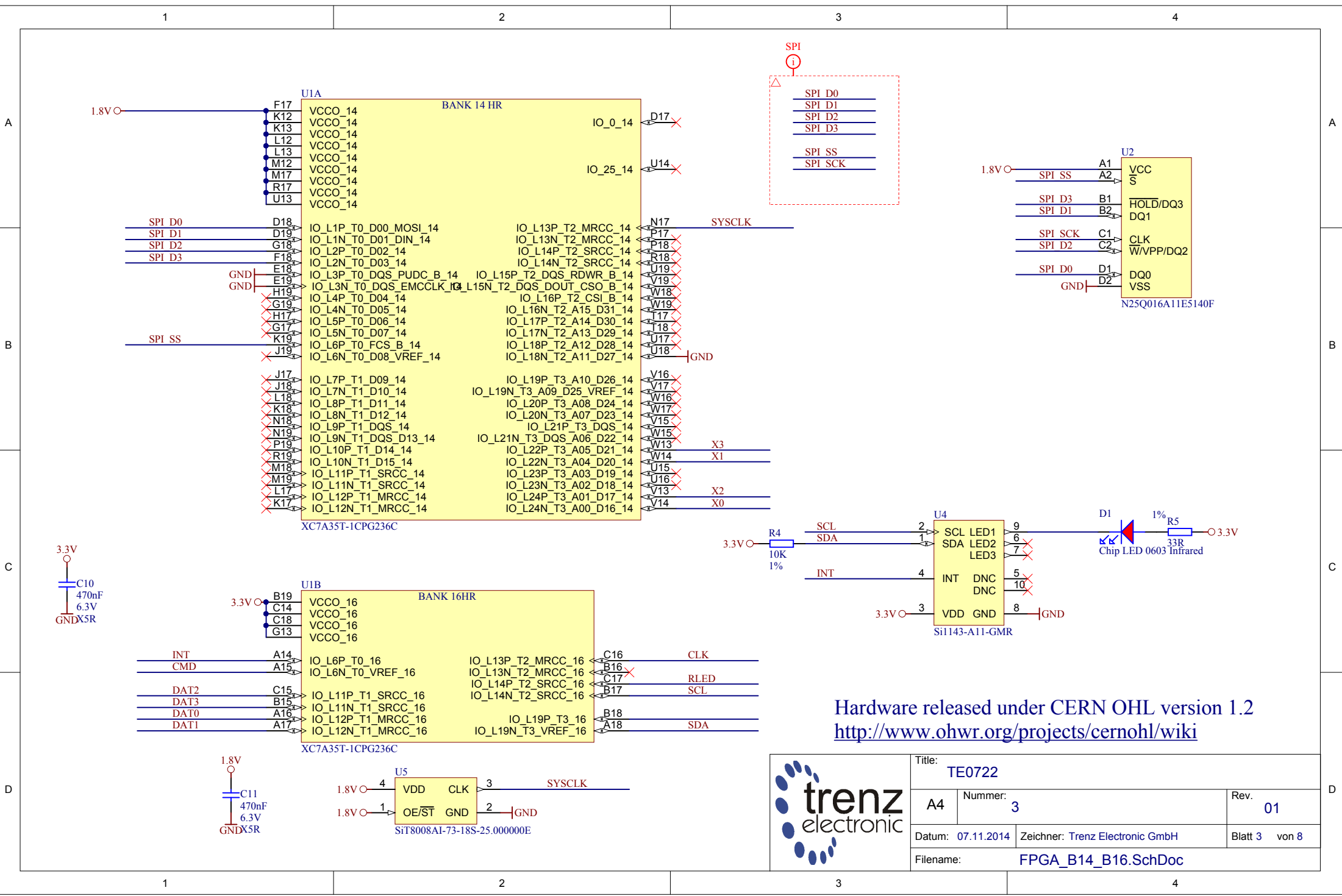

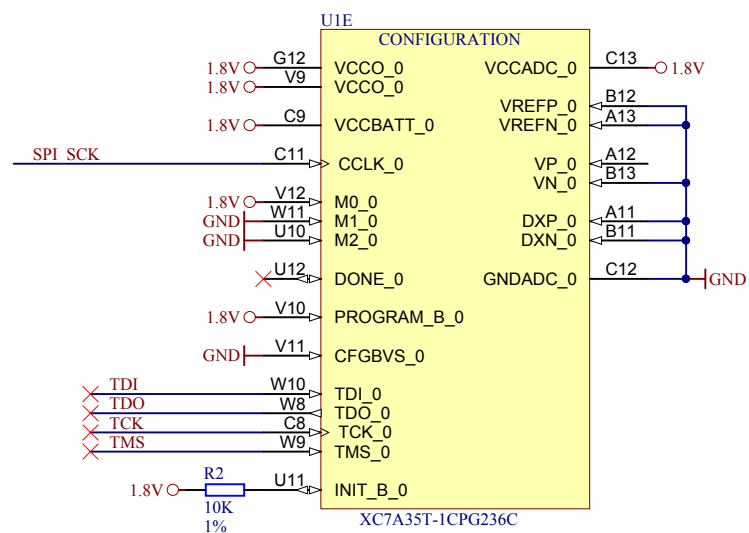


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	A4	Nummer: 2	Rev. 01
	Datum: 07.11.2014	Zeichner: Trenz Electronic GmbH	Blatt 2 von 8
	Filename: FPGA_B34_B35.SchDoc		




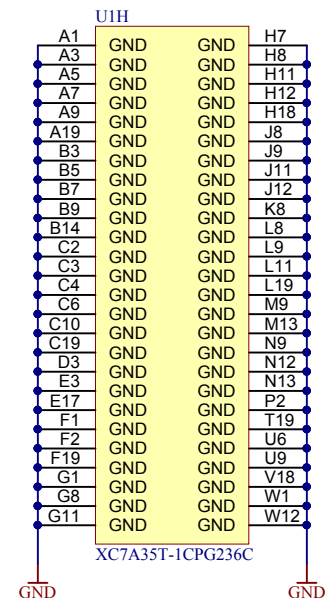
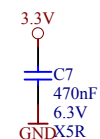
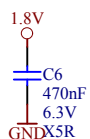
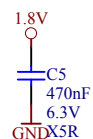
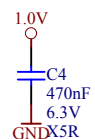
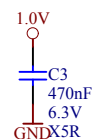
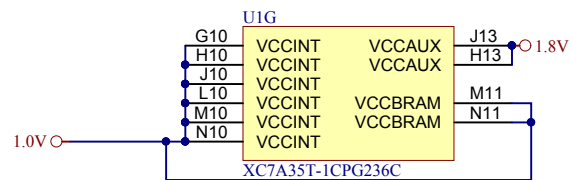
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		Title: TE0722	
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Datum: 07.11.2014		Zeichner: Trenz Electronic GmbH	Blatt 3 von 8
Filename: FPGA_B14_B16.SchDoc			




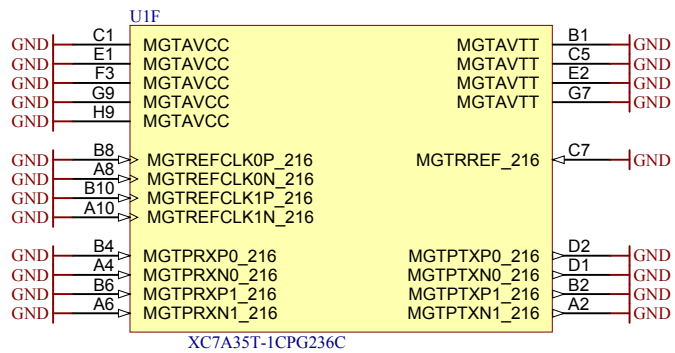
Hardware released under CERN OHL version 1.2
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	Filename: FPGA_CFG.SchDoc		




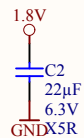
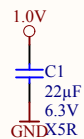
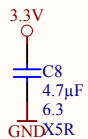
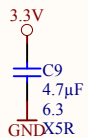
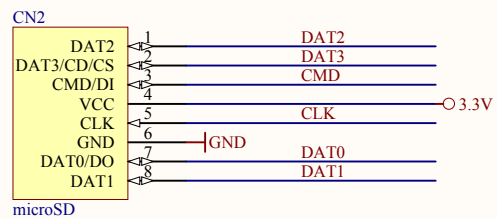
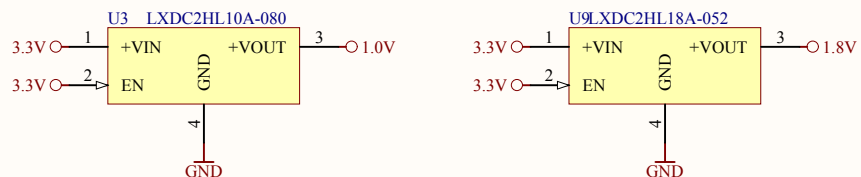
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	Title: TE0722		
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	Filename: FPGA_PWR.SchDoc		



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	Title: TE0723 - FPGA RAM		
	A4	Number: TE0723 [No Variations]	Rev. 01
	Date: 08.07.2015	Copyright: Trenz Electronic GmbH	Page6 of 12
	Filename: FPGA_GTP.SchDoc		



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Title		
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