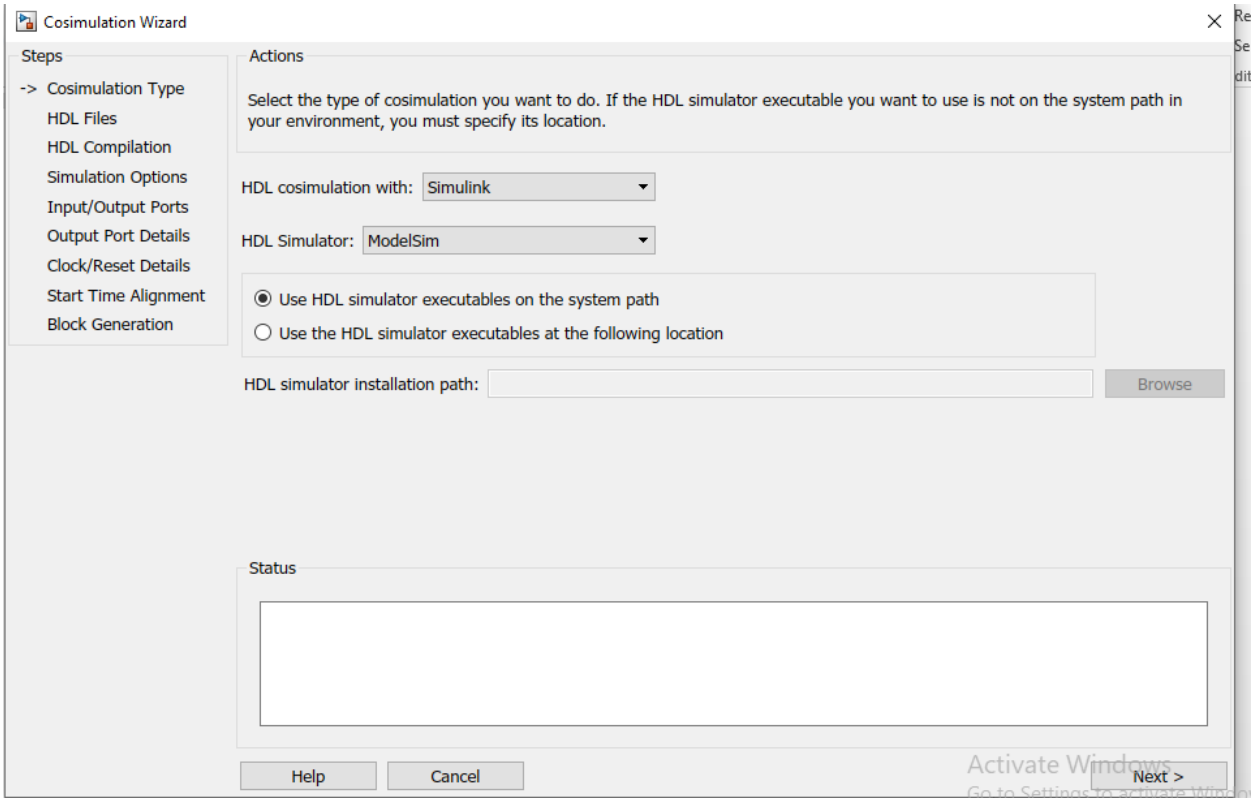
Hello everyone, due to covid-19 we can't perform simulation in labs, so to simulate circuits we are using Simulink. We want to simulate HDL modules and other Simulink blocks too so for that we are using Co-simulation which comes with HDL verifier add on. For using co-simulation, we need either of the two HDL simulators ModelSim/incisive HDL simulator.

How to get cracked version of ModelSim:

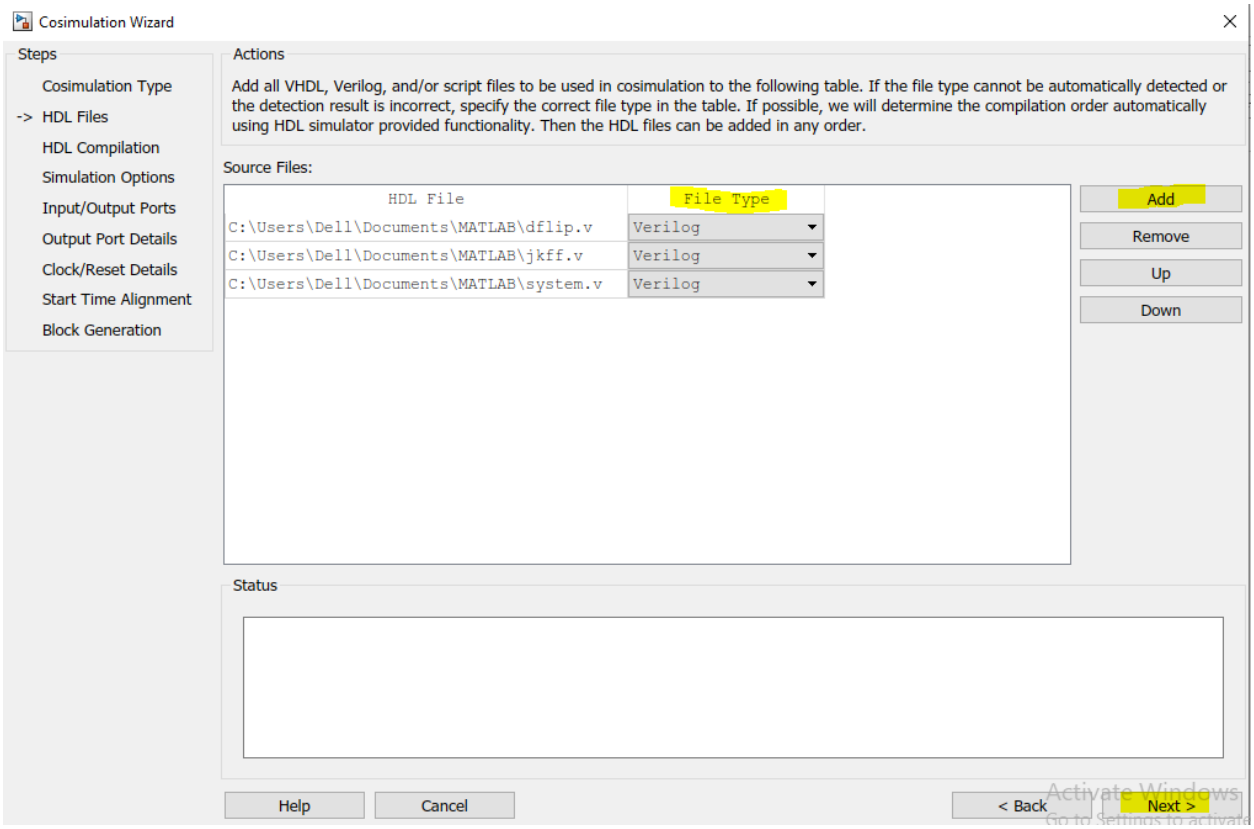
This is the download link:
https://downloadly.net/2020/15/5445/03/modelsim/19/?#/5445-mentor-g-132106054419.html
This video shows how to install:
https://www.youtube.com/watch?v=igPQ6mhbXnQ

How co-simulate HDL with Simulink:

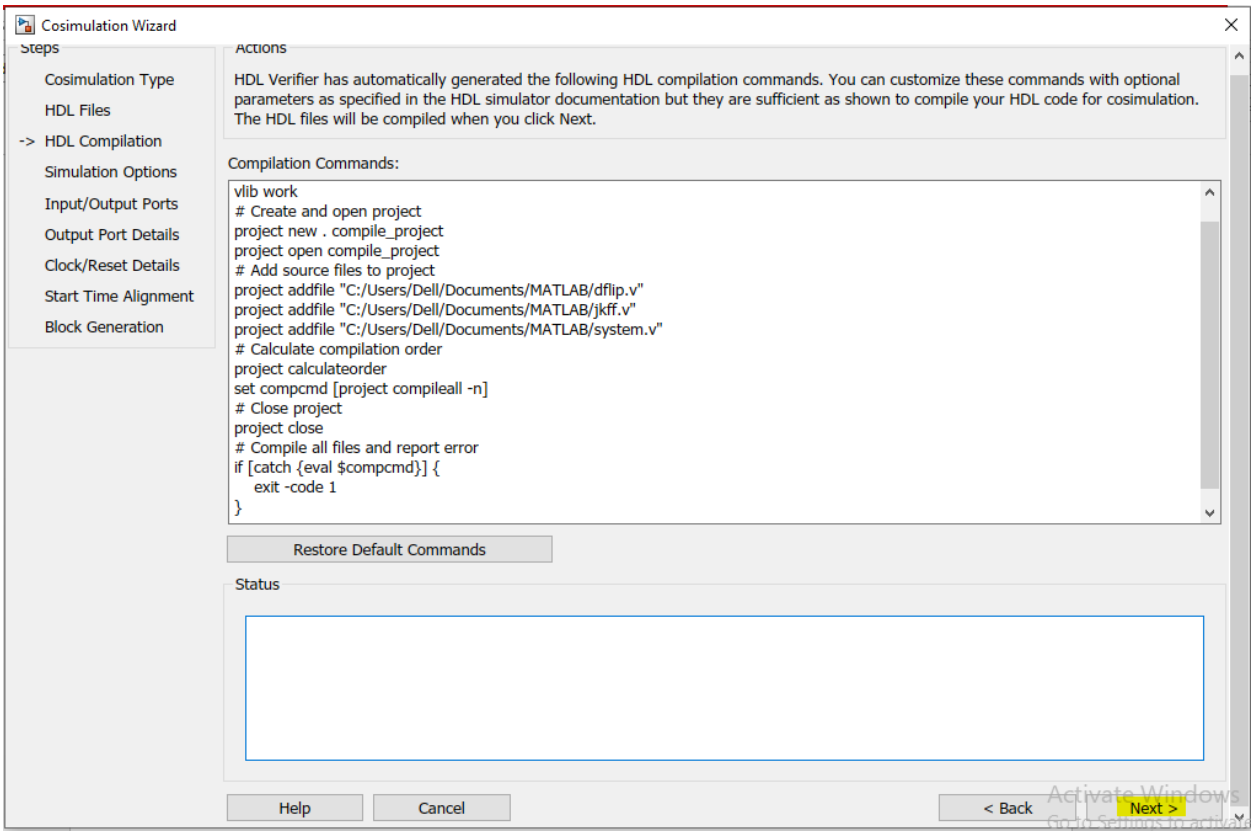
1. Open Matlab, and enter **cosimWizard** in command window.
2. Then this window will pop up:



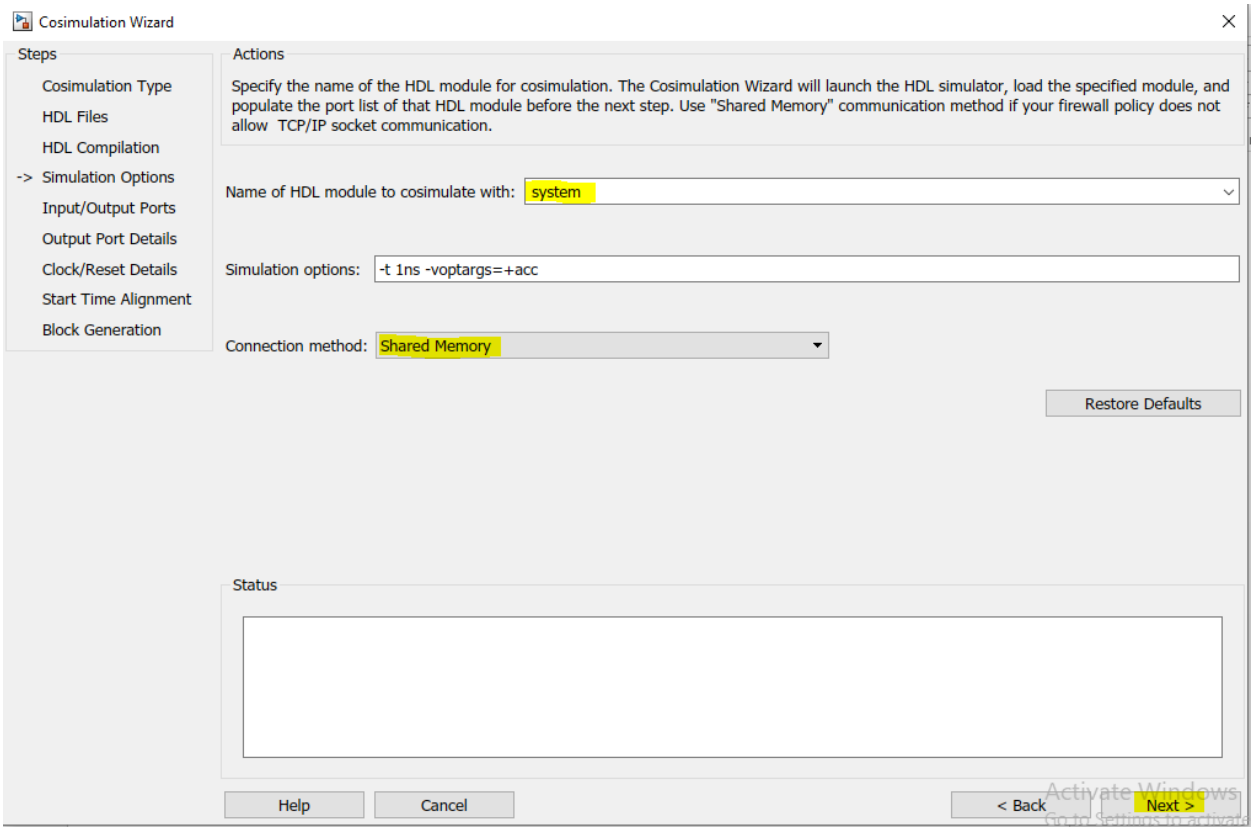
3. Specify simulator you want to use, if it's on your system path, select 1st option, or you can specify path in space given below by selecting 2nd option. And click next.



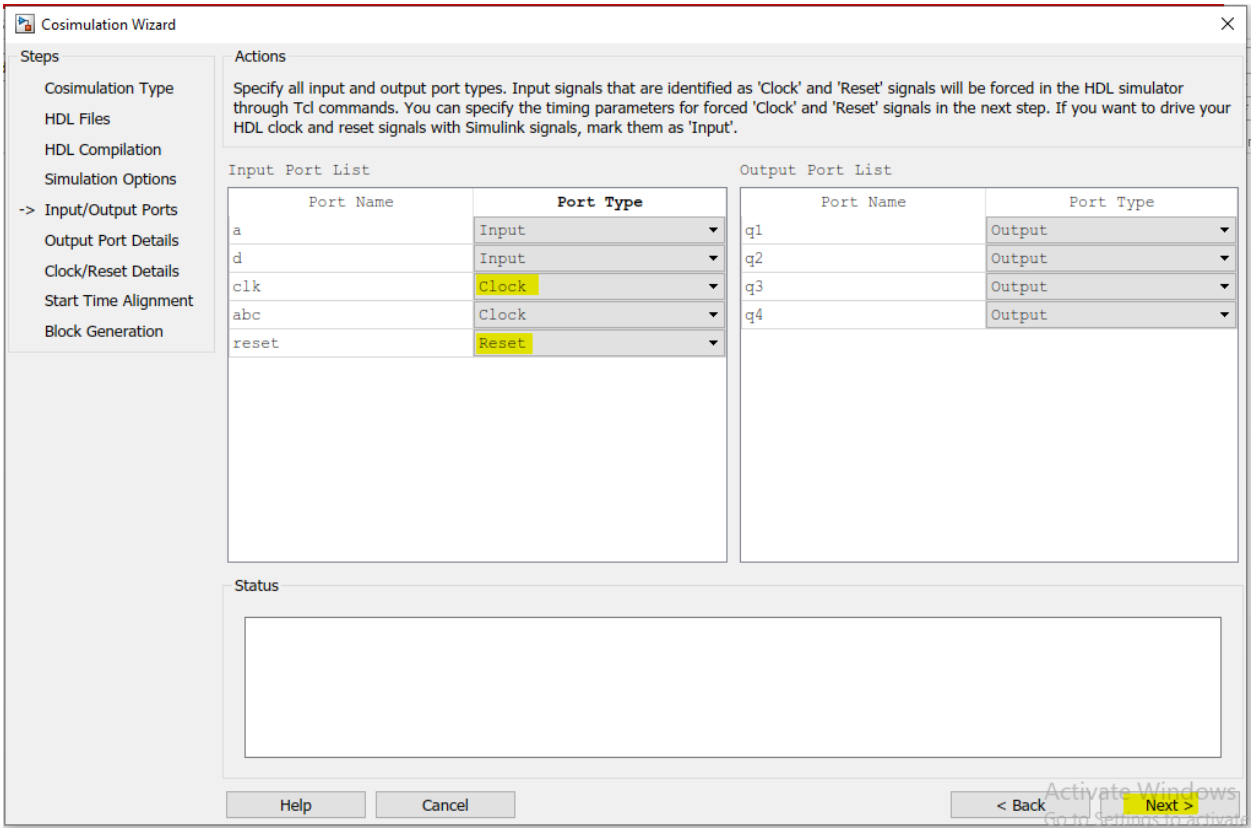
4. Click on add button, and select all files you want to add, wizard will identify file type automatically depending on file name extension, or you can change that manually. And click next after adding all files.



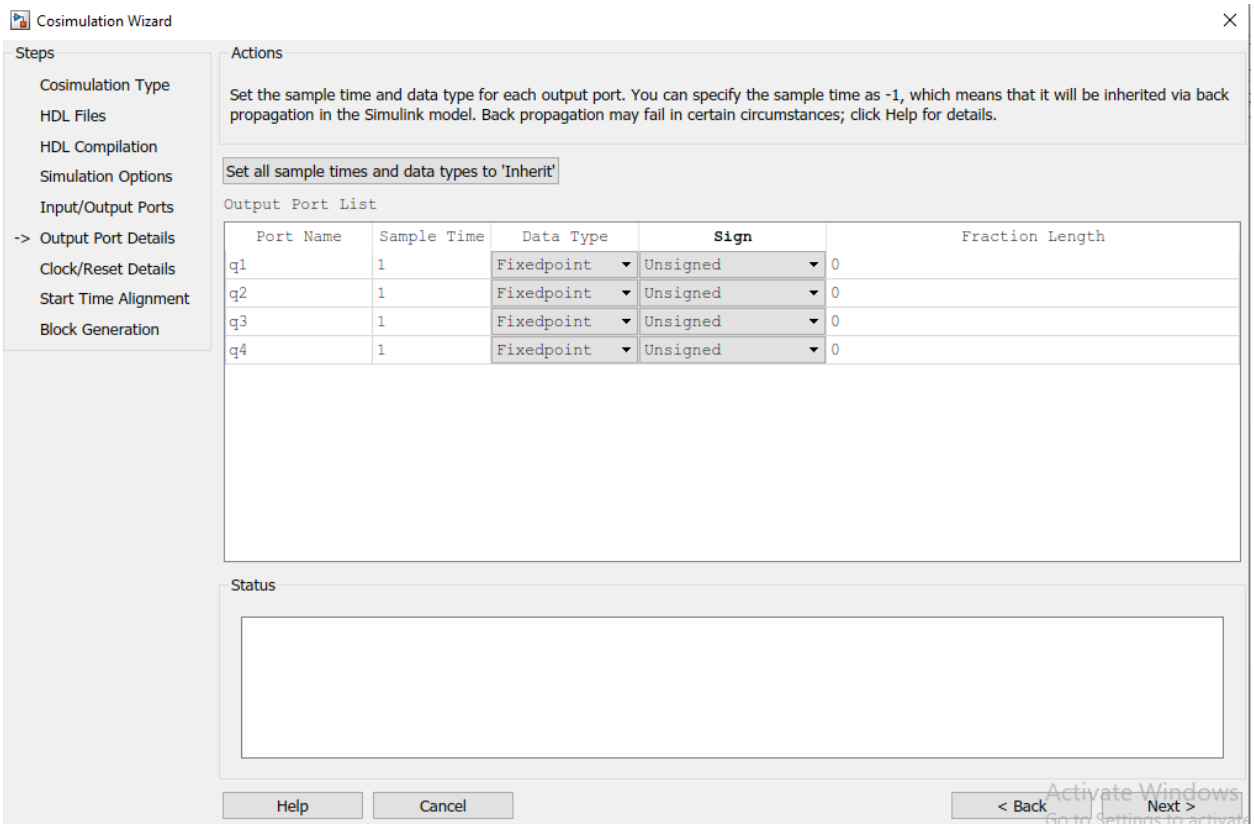
5. Click next. It will compile your all files.



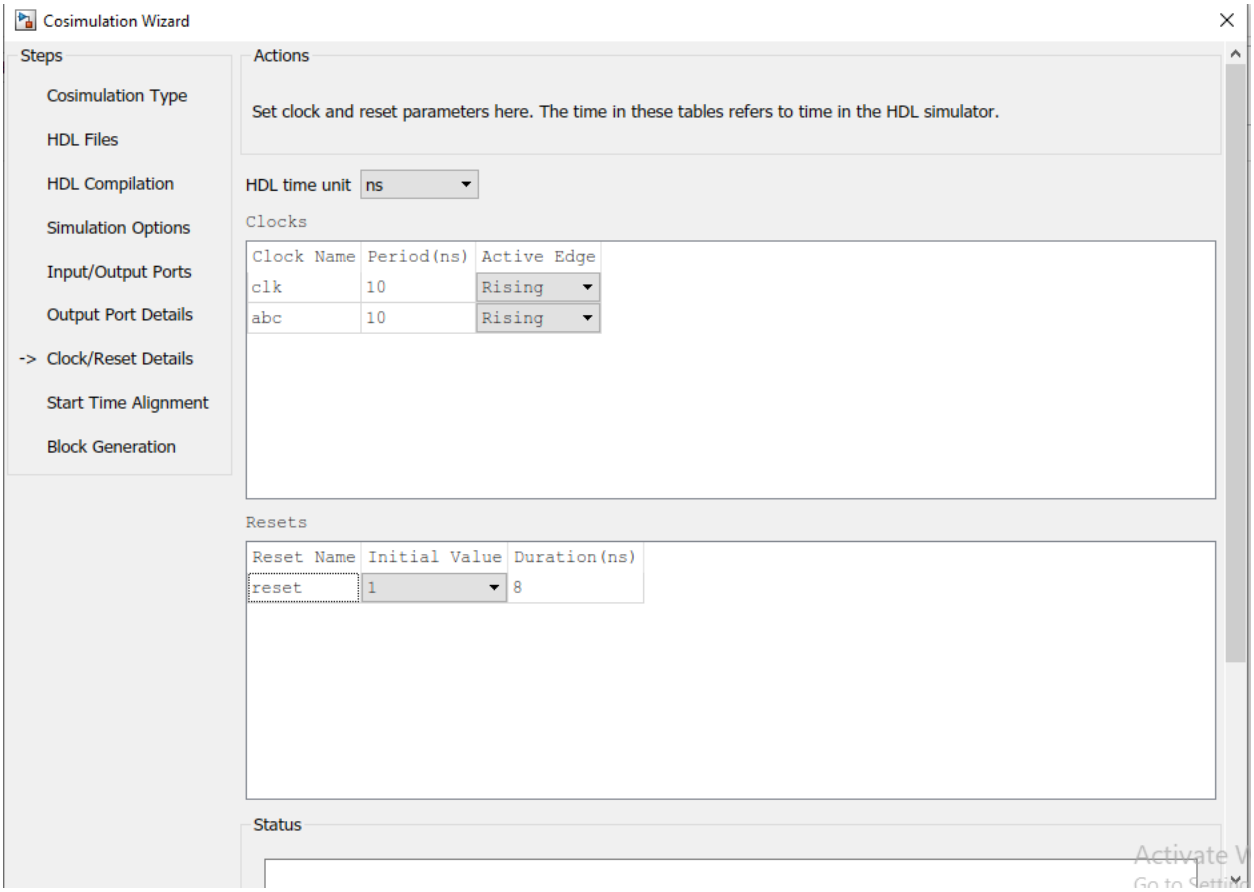
6. Here you can select top module which you want to use, simulation options, and connection method (select shared memory if you want to simulate it on your system only). And click next. (will load HDL modules in HDL simulator, and get port information).



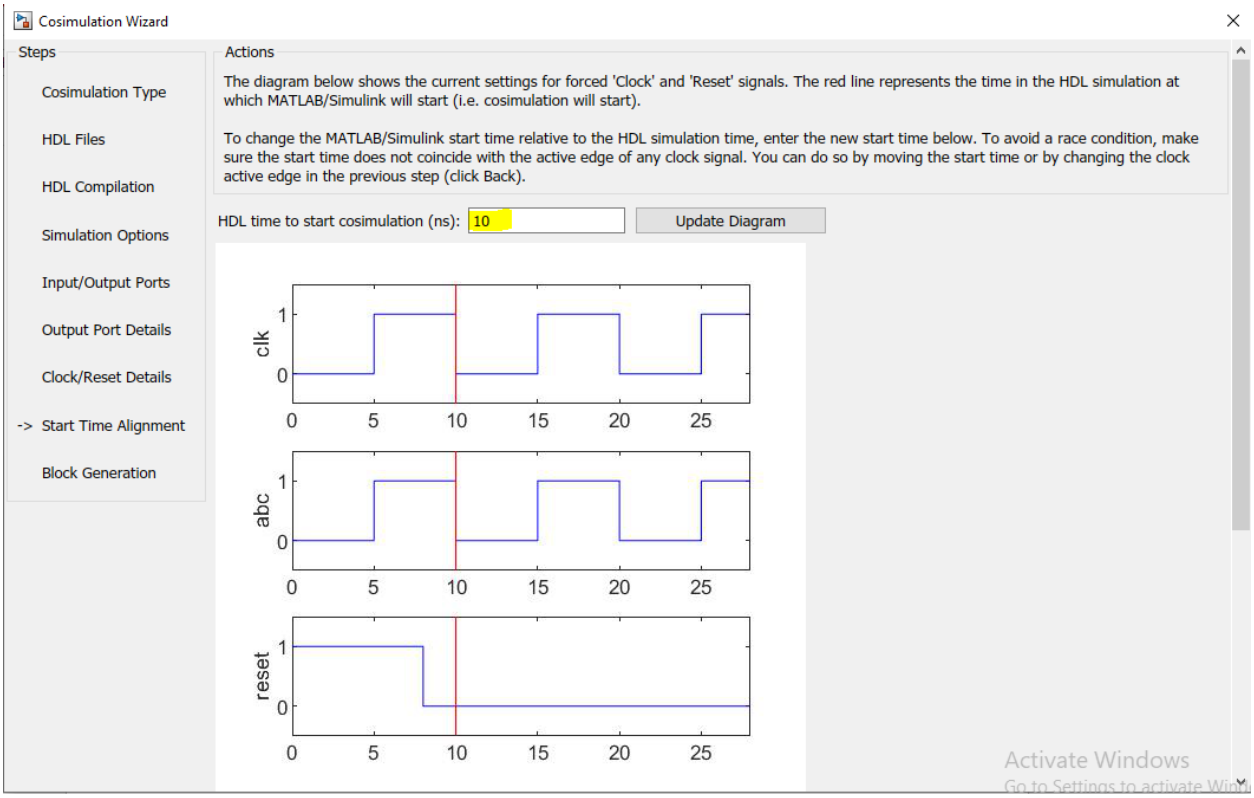
7. Here is information about input and output ports. “Clock” and “Reset” type of input signals will forced in HDL simulator through Tcl command, if we want to drive them through Simulink signal mark them “Input”. And click Next.



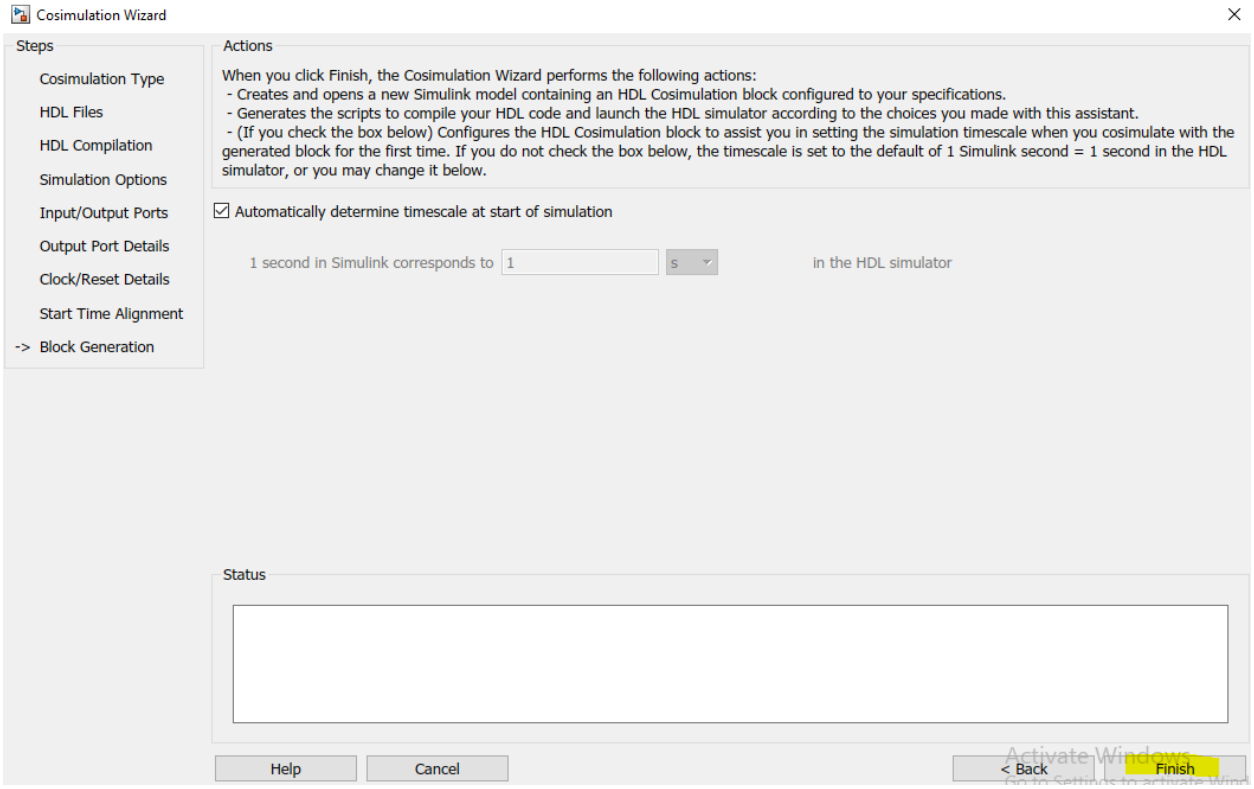
8. Here you can set data type and sampling time of output ports. After setting this click Next.



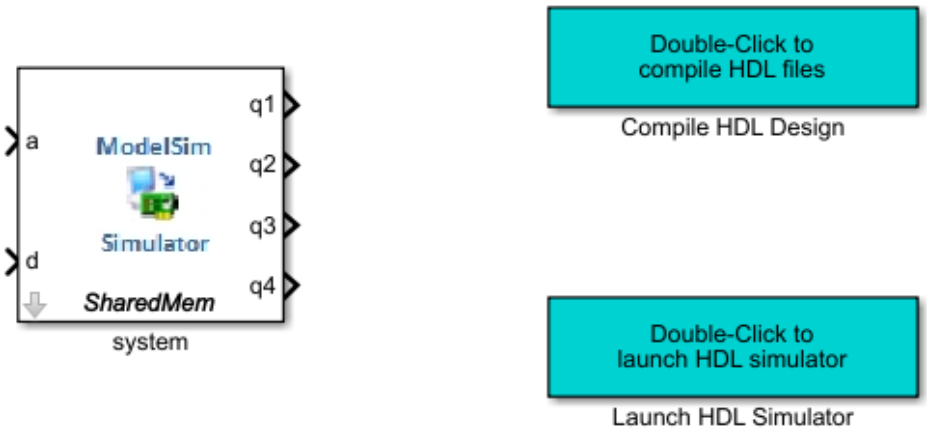
9. Here you can set time period, active edge and reset time of “clock” and “reset” signals which will be forced in HDL simulator through Tcl command. After this click Next. (it will generate clock and reset waveforms)



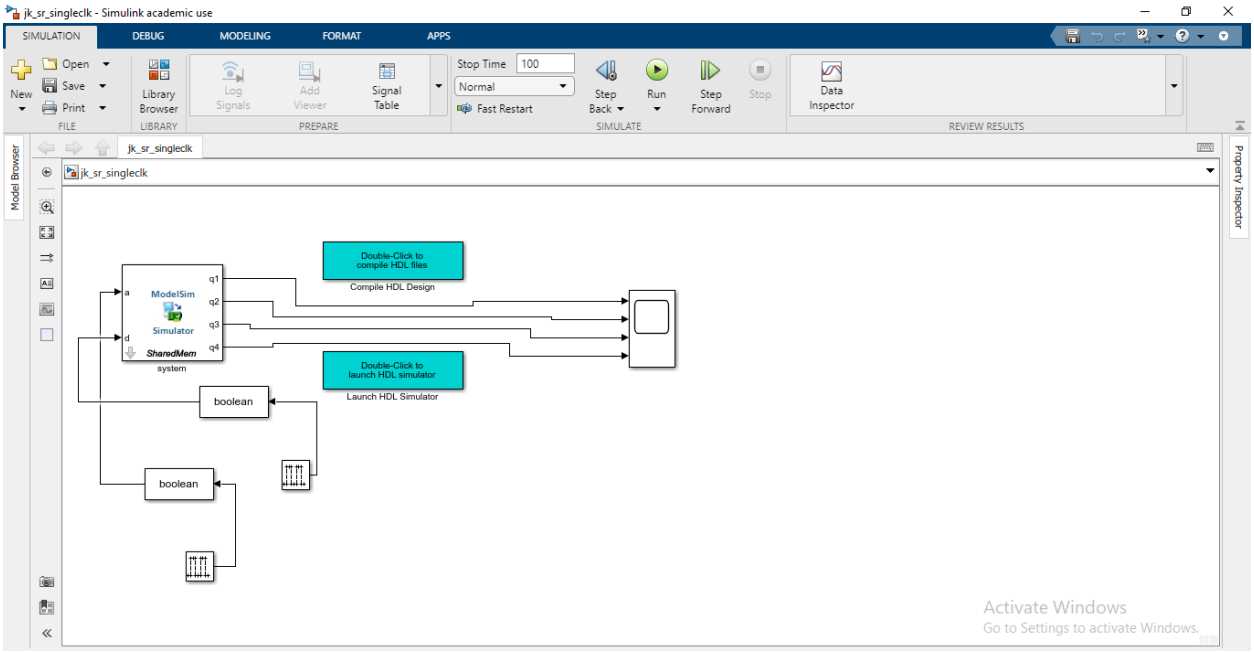
10. Set HDL time to start co-simulation, and click Next.



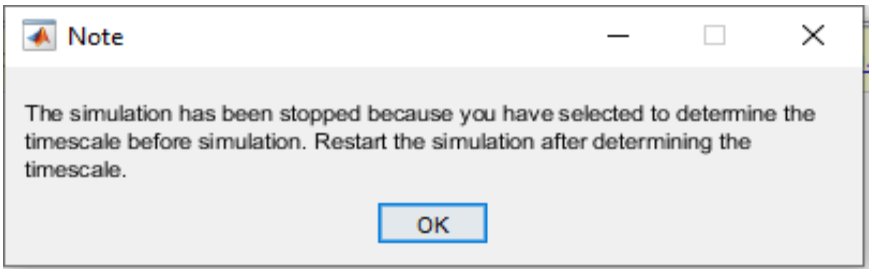
11. Click Finish.



This blocks will be generated. After connecting all the connections, 1st compile HDL design by double clicking “compile HDL files” block, then double click on “launch HDL simulator” to launch HDL simulator. And at the end run simulation.



This one note may come because we selected timescale before selection. Click ok. And select timescale and sampling time. and then run again.



Timescale Details

The timescale is currently set to:
1 second in Simulink corresponds to 1e-09 s in the HDL simulator

Based upon the current timescale, the relationships between Simulink sample times and HDL sample times are shown in the following table for port signals in your design. If this timescale does not satisfy your requirements, supply the desired sample time in one of the editable cells of the table. The other table cells and the current timescale will be updated accordingly.

HDL time unit: ns

Port List

Port Name	Simulink Sample Time (s)	**HDL Sample Time (ns)**
/system/clk	10	10
/system/abc	10	10
/system/a	1	1
/system/d	1	1
/system/q1	1	1
/system/q2	1	1
/system/q3	1	1
/system/q4	1	1

OK Cancel Help

Output on Modelsim will look like this: