Anubhav Bhatla

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Research Interests

Computer Systems and Architecture, Hardware Security

Education

Indian Institute of Technology Bombay *(Nov. 2020 - Present)*
Integrated B.Tech + M.Tech in Electrical Engineering (Electronic Systems) *CPI: 9.13/10*
Minor Degree in Computer Science and Engineering

Scholastic Achievements

- Awarded **Undergraduate Research Award** by IIT Bombay for excellence in research and development *(2023)*
- Secured **All India Rank 266** in *Joint Entrance Exam, JEE (Advanced)* among 160 thousand candidates *(2020)*
- Acquired an **All India Rank 490** in *Joint Entrance Exam, JEE (Mains)* among 1.1 million candidates *(2020)*
- Awarded the *Kishore Vaigyanak Protsahan Yojana* (**KVPY**) fellowship with **All India Rank 337** *(2018)*
- Secured **Top 250** rank among 300 thousand candidates in the *Bits Pilani* entrance examination *(2020)*
- Received **Certificate of Merit** for exemplary performance in Class XII CBSE Board examinations *(2020)*

Publication

A. Bhatla, *Navneet, B. Panda*, The Maya Cache: A Storage-efficient and Secure Fully-associative Last-level Cache
Accepted at the International Symposium on Computer Architecture (ISCA'24)

Research & Work Experience

Hardware-efficient Secure Cache Design *(Jan. 2023 - Nov. 2023)*
Prof. Biswabandan Panda, IIT Bombay *Research Project*

- Proposed Maya, a secure fully-associative last-level cache design which provides complete **security** against eviction-based cache attacks while **saving storage, power, energy, and area** compared to a non-secure baseline
- Designed and simulated a security model for the Maya cache to ensure **no set-associative evictions** occur in $\mathbf{10^{16}}$ **years**
- Implemented the Maya cache design on the **ChampSim** simulator to obtain a **2% performance gain** compared to a non-secure baseline, and performed analysis for sensitivity to the number of cores and cache size

Secure Cache-line Reallocation *(Jul. 2022 - Nov. 2022)*
Prof. Virendra Singh, IIT Bombay *EE691: R&D Project*

- Studied and implemented the **PASS-P**, Utility-based Dynamic Cache Partitioning (**UCP**), and static cache partitioning techniques for multi-core systems on the **Sniper** multi-core simulator & analyzed results for different cache configurations
- Conducted **thorough analysis** of performance, sensitivity, re-allocated blocks and dead blocks for different benchmarks
- Proposed & implemented **modifications to PASS-P** using Sniper simulator, reducing dead block percentage by over **10%**

Sliced-Out-of-Order Core Implementations *(Jul. 2023 - Nov. 2023)*
Prof. Virendra Singh, IIT Bombay *EE748: Advanced Topics in Computer Architecture*

- Reviewed literature on **sliced-OoO** cores which add minimal components on InO cores for MLP extraction
- Implemented the **backward dependency algorithm** and hardware structures proposed by the state-of-the-art **Load-Slice core** using the **Gem5** simulator and extended it to implement the modifications suggested by **Freeflow core**

Embedded Software Intern *(May 2023 - Jul. 2023)*
Texas Instruments India, Bangalore *Summer Internship*

- Created a **driver monitoring application** for the AM62Ax Sitara processor using the **GStreamer** media framework
- Modified the existing GStreamer pipelines to enable **stacking of multiple DNN models** required for the application
- Analyzed the **boot flow** of various processors and created a boot loader **porting guide** for the Sitara AM62x processor
- Reviewed existing documentation and Linux examples for the AM62x & suggested changes to **improve user experience**

Teaching

Teaching Assistant *(Jan. 2023 - Apr. 2023)*
Prof. Virendra Singh, IIT Bombay *EE309: Microprocessors*

- Served as an undergraduate teaching assistant for a batch of **200+** Electrical Engineering sophomores
- Tasked with the responsibility of conducting **doubt-solving sessions** and academically mentoring students

Academic Projects

Superscalar Processor Design *(Jul. 2022 - Nov. 2022)*
Prof. Virendra Singh, IIT Bombay *CS683: Advanced Computer Architecture*

- Designed **2-way OoO Superscalar** processor with a Turing-complete instruction set architecture of **17** instructions
- Implemented key components: Reservation Station, Reorder Buffer, Execution pipelines & Memory system in **VHDL**
- Conducted thorough software testing for all 17 instructions on **GHDL** and GTKWave simulations using a testbench
- Created an **assembler** and a **boot loader** in Python to dump user instructions into the memory of the processor

EEG Data Acquisition System *(Jan. 2023 - Nov. 2023)*
Prof. Siddharth Tallur, IIT Bombay *Supervised Research Exposition & EE344: Electronic Design Lab*

- Studied the datasheets for various ADCs, voltage regulators, microcontrollers, Wi-Fi modules, and other peripherals
- Designed a **24-channel** setup on a **4-layer PCB**, complete with the analog front-end, **daisy-chaining** for the ADCs, analog and digital power regulators, and peripheral interfacing using two **SPI** buses present on the microcontroller
- Implemented a **4-channel modular** signal acquisition setup along with a **3D-printed headgear** for demo purposes
- Received the **Best Project Award** out of **60+** teams for exemplary performance throughout the duration of the project

VLSI Circuit Design *(Jul. 2022 - Nov. 2022)*
Prof. Dinesh Sharma, IIT Bombay *EE671: VLSI Design*

- Designed **logic gates** using CMOS, pseudo-NMOS, CVSL and CPL design styles, and analyzed output characteristics
- Created a 16-bit **Brent Kung** logarithmic fast adder in **VHDL** and validated the design using **ModelSim** simulations
- Utilized the **Dadda Reduction Algorithm** to optimize the efficiency of a 16-bit **Multiply and Accumulate** circuit

Low Power OTA Design with RC Compensation *(Jul. 2023 - Nov. 2023)*
Prof. Rajesh Zele, IIT Bombay *EE618: CMOS Analog VLSI Design*

- Designed and implemented a **low-power** 2-stage Operational Transconductance Amplifier with **RC Compensation** using **Cadence** to attain 50 dB gain, unity gain frequency of 108MHz & phase margin of 67.4°
- Attained slew rate of 163 V/μs, 1% settling time of 6.84 ns and 69.1 dB CMRR, within 0.22mW power budget

VLSI Circuit Partitioning *(Jul. 2022 - Nov. 2022)*
Prof. Virendra Singh, IIT Bombay *EE677: Foundation of VLSI CAD*

- Studied and implemented graph partitioning algorithms and heuristics such as the **Kernighan-Lin Algorithm**, **Clustering Based Heuristic**, and **Hagen Kahng EIG Algorithm** used for efficient VLSI circuit partitioning
- Performed comparative performance analysis & visualization of the algorithms using matplotlib and **networkx** libraries

CMOS Implementation of Low Power Equi-Prop System *(Jul. 2023 - Nov. 2023)*
Prof. Udayan Ganguly, IIT Bombay *EE746: Neuromorphic Engineering*

- Modelled activity of spiking neurons like **Izhikevich** and **Hodgkin-Huxley** to determine energy cost of a spike
- Implemented the Spiking Equilibrium Propagation algorithm in **45nm CMOS** technology using **LTSpice**
- Achieved a total power consumption of 82.7μW with only 8.8μW power consumed by the synapse circuit

Pipelined Processor Design *(Jan. 2022 - Apr. 2022)*
Prof. Virendra Singh, IIT Bombay *EE309: Microprocessors*

- Designed and implemented a **16-bit, 6-stage pipeline** processor, capable of efficiently running a total of **17** instructions
- One of the few teams to optimize the processor using **Hazard mitigation**, **Forwarding** & **Branch prediction** techniques
- Performed software testing for all the instructions using **Intel Quartus** Environment and the **ModelSim** HDL simulator

Valet Parking Bot *(Jan. 2023 - Apr. 2023)*
Prof. Paritosh Pandya and Prof. Kavi Arya, IIT Bombay *CS684: Embedded Systems*

- Interfaced tracker sensors, proximity sensors, and position encoders using the **Arduino** board present on the **Alphabot**
- Implemented and tested algorithms for line following, obstacle avoidance, and parking using the **Heptagon** language
- Programmed the controller in **Embedded C** to set up sensors & motor drivers, and interface with the Heptagon code

Predicting the RUL of EV Batteries *(Jul. 2021 - Nov. 2021)*
Prof. Amit Sethi, IIT Bombay *DS203: Programming for Data Science*
- Achieved an **R2 score** of **98.09** for estimating the **RUL** of EV Lithium batteries using the **XGBoost** regression model
- Performed EDA on the charging, discharging and impedance cycles for Li-ion batteries using NASA's PCoE Datasets
- Understood and tested various models such as SVR, Multilayer Perceptron, LSTM, and various **Boosting Algorithms**

Digital Circuit Design *(Jul. 2021 - Nov. 2021)*
Prof. Maryam Shojaei Baghini, IIT Bombay *EE214: Digital Circuits Lab*
- Acquired the knowledge of **Finite-state machines** and the methodology for implementing them using D-FlipFlops
- Implemented a **4-bit Sequence Generator** with D-FlipFlops using sequential and behavioral modelling in **VHDL**
- Performed software testing using Quartus simulations and hardware testing using **Scanchain** on the **Krypton board**

Microprocessor Implementations *(Jan. 2022 - Apr. 2022)*
Prof. Saravanan Vijaykumaran, IIT Bombay *EE337: Microprocessors Lab*
- Designed and tested a two-party, password-secure ATM capable of taking action inputs from keyboard using **UART**
- Implemented a **reaction timer** in **Assembly** to display the time it takes for the user to respond to a stimulus (in ms)
- Developed a subroutine capable of generating voltage waveforms corresponding to **music note frequencies** using **timers**
- Interfaced LM35 sensor with μC using **serial peripheral interfacing** to monitor & display real-time ambient temperature

Reading Projects

General Purpose GPUs *(May 2022 - Jul. 2022)*
Prof. Virendra Singh, IIT Bombay *Research Project*
- Studied and reviewed the SIMT Core, Memory systems and the programming model related to **GP-GPU architecture**
- Reviewed literature about analyzing and leveraging a **Decoupled LLC** design and implementing it on GPGPU-Sim
- Performed various benchmark simulations on the **GPGPU-Sim** simulator and carefully analyzed the outputs received

Operating Systems *(May 2022 - Jul. 2022)*
Maths and Physics Club, IIT Bombay *Summer of Science*
- Studied various **Scheduling** policies, **Process APIs**, and **Context switching** used to facilitate **CPU Virtualization**
- Covered different **Memory APIs**, Segmentation, Paging, TLBs, and Swapping in context of **Memory Virtualization**

Technical Skills

Languages	C, C++, VHDL, Verilog, Python, Assembly, Heptagon
Software	Intel Quartus, Autodesk Fusion 360, GStreamer, Cadence Virtuoso, GHDL, Keil μVision, MATLAB, LTSpice, Ngspice, ArduinoIDE, GNU Radio, LaTeX, AutoCAD, Solidworks
Simulators	ChampSim, gem5, Sniper, GPGPU-Sim

Courses Undertaken

Computer Architecture: Advanced Topics in Computer Architecture, Advanced Computer Architecture, Microprocessors

Hardware Design: VLSI Design, Algorithmic Design of Digital Systems, RF Microelectronics Chip Design, Testing & Verification of VLSI Circuits, CMOS Analog VLSI Design, VLSI Design Lab, Electronic Design Lab, Neuromorphic Engineering, Foundation of VLSI CAD

Computer Science: Data Structure & Algorithms, Design & Analysis of Algorithms, Principles of Data & System Security, Embedded Systems, Discrete Structures

Electrical Engineering: Communication Networks, Nanoelectronics, Signal Processing, Control Systems

Miscellaneous: Intro to Machine Learning, Economics, Sociology, Quantum Physics & Application, Biology

Extracurriculars

- Completed one year of training under the **National Cadet Corps**, IIT Bombay *(2021)*
- Awarded **Special Mention** out of **82** students in LaTeX boot camp conducted by UGAC, IIT Bombay *(2021)*
- Designed & assembled remote-controlled plane for **RC Plane Competition** held by Aeromodelling Club *(2021)*
- Volunteered as a guide for the EE lab tour organized by Alumni & Corporate Engagement Assoc. *(2022)*