Anubhav Bhatla

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Research Interests

I am broadly interested in Computer Systems & Architecture and Hardware Security. This includes advanced topics such as secure and randomized caches, cache partitioning techniques, and branch predictor designs.

Education

Indian Institute of Technology Bombay *(Nov 2020 - Present)*
Integrated Bachelor and Master of Technology (Dual Degree) in Electrical Engineering *GPA: 9.13/10*
Minor Degree in Computer Science and Engineering

Publications

- A. Bhatla†, Navneet†, M. Qureshi, B. Panda. **"OASIS: Enabling Provably Secure Randomized Caches at Ultra-Low Cost."** *Under review at an A* computer architecture conference*
- A. Bhatla†, H. Bhavsar†, S. Saha, B. Panda. **"So, You Think You Know All About Randomized Caches?"** *Under review at an A* computer architecture conference*
- A. Bhatla†, Navneet†, B. Panda. **"The Maya Cache: A Storage-efficient and Secure Fully-associative Last-level Cache."** *Presented at the International Symposium on Computer Architecture* ***(ISCA'24)*** (Paper, Talk, Artifact)

†*denotes equal contribution*

Research Experience

Practical and Secure Randomized Cache Design at Ultra-Low Cost *(Jan 2023 - Present)*
Prof. Biswabandan Panda, IIT Bombay *Research Project*

1. **Maya Cache Design**
   - Thoroughly studied the Mirage cache design which provides security against conflict-based attacks at a high power, storage and area overhead, and observed that $>$**80%** of the entries brought into the last-level cache are dead
   - Utilized the idea of **Reuse Cache** to shrink the Mirage data store, along with a reuse-based smart insertion policy which only inserts an entry into the data store on its second cache access, for **efficient utilization** of the data store
   - Designed a security model for Maya, based on **Markov chains**, and simulated it for 1 trillion cache accesses, along with a mathematical proof to show that no set-associative evictions occur in over 10^{32} cache accesses (**10^{16} years**)
   - Modelled the Maya cache in the **ChampSim** simulator and **PCACTI** 7nm FinFET to show savings in storage (2%), power (5%), energy (13%), and area (28%), compared to a traditional non-secure set-associative cache
   - Used the **CacheFX** simulator to show that Maya performs similar to a fully-associative cache against **occupancy-based attacks**, by estimating the number of encryptions required to break AES and modular exponentiation
2. **Oasis Cache Design** *(Collaborator: Prof. Moinuddin Qureshi, Georgia Tech)*
   - Analyzed the practicality and **design complexity** of various state-of-the-art secure LLC designs such as Mirage and Maya, with the aim of designing a simpler and more practical LLC design with very little overheads
   - Observed that **increasing the cache associativity** along with **invalidation** of a fraction of cache lines helps provide security against conflict-based attacks without using any tag store-data store decoupling or storage of pointers
   - Provided **"security-on-demand"** by providing the user with the option of security in the BIOS. If the user opts for no security, Oasis operates as a traditional non-secure set-associative cache, operating at **zero overheads**
   - Performed extensive simulations using a modified version of the Mirage **bucket-and-balls model**, simulated for 1 trillion cache accesses, along with mathematical proofs to show **complete security** in a system's lifetime
   - Implemented the Oasis design on the **ChampSim** multi-core simulator and **PCACTI** 7nm FinFET to show a $<$0.2% performance overhead, a 2% power overhead, 0.9% storage overhead when operating in the secure mode
3. **Demystifying Randomized Caches** *(Collaborators: Intel India | Prof. Sayandeep Saha, IIT Bombay)*
   - Performed a thorough security analysis of various state-of-the-art secure cache designs such as Mirage, Maya, and Oasis to understand the **minimal set** of **necessary and sufficient additions** required to make the LLC secure
   - Analyzed the effect of various features such as the use of skews, load-balancing insertion policy, tag store-data store decoupling, extra invalid tag ways, and a global random eviction policy on the security guarantee
   - Working on a **secure** & **morphable** LLC design which requires minimal changes on top of a traditional cache to make it secure by going back to older and simpler cache designs such as **CEASER** and **CEASER-S**

Branch Predictor Partitioning for Performance *(Apr 2024 - Present)*
Prof. Dean Tullsen, University of California, San Diego *Research Project*

- Studied the **Half&Half** branch predictor partitioning technique and how partitioning the branch predictor between threads can help improve performance for certain application pairs running in **SMT** mode
- Used the **perf** tool to identify application pairs from the **SPEC2017** benchmark suite which have high conditional branch mis-prediction rates when running in SMT mode on the same core
- Implemented the **branch-alignment algorithm** suggested in Half&Half on top of the **LLVM** compiler to align conditional branches to the appropriate program counter values to ensure that only half of the conditional branch predictor is used
- Working on identifying **prediction-critical workloads** that don't perform well when running concurrently with another process in SMT mode, and will benefit from using a partitioned conditional branch predictor

Secure Cache-line Reallocation in Partitioned Caches (Report) *(Jul 2022 - Nov 2022)*
Prof. Virendra Singh, IIT Bombay *Research Project*

- Studied and implemented the **UCP** and static cache partitioning technique on the **Sniper** multi-core simulator, along with **PASS-P**, which provides security against side-channel attacks for dynamic cache-partitioning techniques
- Conducted a thorough performance analysis on **SPEC2006** benchmark pairs, sensitivity to cache associativity and cache size, number of clean re-allocated blocks and the number of dead blocks in the cache
- Proposed and **implemented modifications** to PASS-P, based on observing a high dead block percentage, to **preferentially reallocate dead blocks** on every phase change instead of dirty blocks, thereby reducing dead blocks by over **10%**

Honours & Awards

- Awarded the **Intel India Research Fellowship** 2024-25 with a total grant of INR 800,000 ($9500) *(2024)*
- Ranked $\mathbf{5^{th}}$ among **99** students enrolled in the Electrical Department Dual Degree program *(2024)*
- Scored a perfect **10 SPI** (Semester Performance Index) in the 8^{th} academic semester *(2024)*
- Sanctioned a **grant** of INR 420,000 ($5000) for presenting at **ISCA'24**, Argentina, as an undergraduate *(2024)*
- Awarded **Undergraduate Research Award** by IIT Bombay for excellence in research and development *(2023)*
- Acquired the **Best Project Award** for our extensive analysis & experimentation with NIPIN in EE724 *(2023)*
- Received the **Best Project Award** for our design of the 24-channel EEG acquisition system in EE344 *(2023)*
- Secured **All India Rank 266** in Joint Entrance Exam, JEE (Advanced) among 160,000 candidates *(2020)*
- Acquired an **All India Rank 490** in Joint Entrance Exam, JEE (Main) among 1.1 million candidates *(2020)*
- Awarded the Kishore Vaigyanak Protsahan Yojana (**KVPY**) fellowship with **All India Rank 337** *(2018)*

Teaching & Mentorship Experience

Department Academic Mentor *(May 2024 - Present)*
Student Mentorship Program, IIT Bombay *Mentorship*

- Selected as part of a **54**-member team handpicked after a rigorous process of meticulous interviews and peer reviews
- Appointed to personally mentor **6 sophomores** with their academics, extra-curricular activities, career paths, and research journeys during the rigorous second year in Electrical Engineering at IIT Bombay
- Contributed to the department website blog and collected course feedback, providing academic help to **1300+** students

Teaching Assistant
Served as a TA for Electrical Engineering and Computer Science students in the following courses:

- CS683: Advanced Computer Architecture (110+ students) Instructor: *Prof. Biswabandan Panda* *(2024)*
- EE229: Signal Processing (90+ students) Instructor: *Prof. Preeti Rao* *(2024)*
- EE309: Microprocessors (200+ students) Instructor: *Prof. Virendra Singh* *(2022)*

Responsible for creating **assignment problems**, conducting **doubt-solving sessions** to help academically weak students, creating **tutorial solutions**, helping with the **course evaluation**, and academically mentoring students

Professional Experience

Embedded Software Intern *(May 2023 - Jul 2023)*
Texas Instruments India, Bangalore *Internship*

- Created a **driver-monitoring application** for the AM62Ax Sitara MPU, capable of detecting **driver-drowsiness** and **gaze-detection** to ensure that the driver is attentive towards the road which helps reduce the risk of accidents
- Used the **GStreamer** media framework to create a new media pipeline which enables **stacking of multiple DNN models**, required for using multiple DNN models to efficiently and correctly make classifications using just the driver's face
- Analyzed and documented the **boot flow** of various microprocessors and created a boot loader **porting guide** for the Sitara AM62x MPU which makes it easier to port user applications from a different microprocessor to the AM62x

Selected Academic Projects (Full list)

Sliced-Out-of-Order Core Implementations (Report) *(Jul 2023 - Nov 2023)*
Prof. Virendra Singh, IIT Bombay *EE748: Advanced Topics in Computer Architecture*

- Reviewed literature on sliced-OoO cores, such as **Load-Slice** core, **Freeflow** core, and **Freeway** core, which use minimal additional components on top of in-order cores to extract **memory-level parallelism**
- Implemented the **backward dependency algorithm** and additional hardware structures proposed by the state-of-the-art Load-Slice core using the **gem5** simulator and extended it to implement the modifications suggested by Freeflow core

2-way OoO Superscalar Processor Design (Repository) *(Jul 2022 - Nov 2022)*
Prof. Virendra Singh, IIT Bombay *CS683: Advanced Computer Architecture*

- Designed a **2-way** Out-of-Order Superscalar processor with a Turing-complete ISA comprising of **17 instructions**
- Implemented key components: Reservation Station, Reorder Buffer, execution pipelines and memory system in **VHDL**, along with an **assembler** and a **boot loader** in Python to dump user instructions into the memory of the processor
- Conducted thorough software testing for all 17 instructions on **GHDL** and GTKWave simulations using a testbench

General Purpose GPUs (Report) *(May 2022 - Jul 2022)*
Prof. Virendra Singh, IIT Bombay *Summer Project*

- Reviewed **GP-GPU architecture** as well as literature on leveraging a **Decoupled LLC** design for dynamically switching the LLC between private and shared modes, and implemented this design on the GPGPU-Sim simulator
- Performed various benchmark simulations on the **GPGPU-Sim** simulator and carefully analyzed the outputs received

24-channel EEG Data Acquisition System (Report, Code) *(Jan 2023 - Nov 2023)*
Prof. Siddharth Tallur, IIT Bombay *Research Exposition & EE344: Electronic Design*

- Designed a **24-channel** EEG data-acquisition setup on a **4-layer PCB** using **daisy-chained** ADCs, analog front-end, voltage regulators, and interfacing with the Wi-Fi module, accelerometer, SD Card reader, using **SPI**
- Implemented an additional **4-channel modular** signal acquisition setup with **3D-printed headgear** for demo purposes

Optimal Device Design for NIPIN Memory Selector (Report) *(Jan 2024 - Apr 2024)*
Prof. Udayan Ganguly, IIT Bombay *EE724: Nanoelectronics*

- Performed pen-paper analysis for **NIPIN** device & verified it using **TCAD** simulations on **Synopsys Sentaurus Workbench**
- Optimized the idealty factor to **1.33** by introducing different ratios of **Germanium** in the p-regions instead of pure Si

CMOS Implementation of Low Power Equi-Prop System (Report) *(Jul 2023 - Nov 2023)*
Prof. Udayan Ganguly, IIT Bombay *EE746: Neuromorphic Engineering*

- Implemented **Spiking Equilibrium Propagation** real-time learning algorithm in **45nm CMOS** technology using **LTSpice**
- Achieved an **energy-efficient** circuit with 82.7μW total power and only 8.8μW consumed by the synapse circuit

Voltage-Controlled Oscillator Design (Report) *(Jan 2024 - Apr 2024)*
Prof. Rajesh Zele, IIT Bombay *EE619: RF Microelectronics Chip Design*

- Designed and implemented a **low-power cross-coupled** voltage-controlled oscillator using **Cadence Virtuoso**
- Achieved a frequency of 6GHz, phase noise of -117dBc/Hz, tuning range of 28MHz, and a power budget of **3mW**

Technical Skills

Languages	C, C++, VHDL, Verilog, Python, Assembly (8085), Algorithmic assembly (Aa), Heptagon
Software	Intel Quartus, Vivado, Fusion360, Cadence Virtuoso, Synopsys Sentaurus, LTSpice
Simulators	ChampSim, gem5, Sniper, GPGPU-Sim, CacheFX, PCACTI

Courses Undertaken (Full list)

Computer Systems: Advanced Computer Architecture - I, Advanced Computer Architecture - II, Operating Systems, High-Performance Scientific Computing, Microprocessors[§]

Hardware Design: VLSI Design[§], Algorithmic Design of Digital Systems, RF Microelectronics Chip Design, Testing & Verification of VLSI Circuits, CMOS Analog VLSI Design, Electronic Design, Neuromorphic Engineering, Foundation of VLSI CAD, Nanoelectronics

Computer Science: Data Structure & Algorithms, Design & Analysis of Algorithms, Principles of Data & System Security, Embedded Systems, Discrete Structures

Electrical Engineering: Digital Systems[§], Analog Circuits[§], Communication Networks, Wireless & Mobile Communication, Information Theory & Coding, Electronic Devices[§], Signal Processing[§], Control Systems[§]

[§]*along with a lab component*