# **Anubhav Bhatla**

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# Research Interests

Computer Architecture, Microarchitectural Security, Digital Design, Microprocessors

# Education

### **Indian Institute of Technology Bombay**

Bachelor of Technology in Electrical Engineering with Honours Minor in Computer Science and Engineering (Jul. 2020 - Present) CPI: 9.03/10

# **Scholastic Achievements**

<ul> <li>Secured All India Rank 266 in JEE Advanced, 2020 among 160 thousand candidates</li> </ul>	(2020)
o Acquired an All India Rank 490 in JEE Mains, 2020 among 1.1 million candidates	(2020)
o Awarded the Kishore Vaigyanak Protsahan Yojana (KVPY) fellowship with All India Rank 337	(2018)
<ul> <li>Qualified for Indian National Olympiad (INO) in Astronomy, Chemistry &amp; Physics</li> </ul>	(2019)
<ul> <li>Bagged a position among the Top 1% students nationally in NSEP &amp; NSEA</li> </ul>	(2019)
o Secured <b>399 marks out of 450</b> in the <i>BITSAT</i> examination ( <b>Top 250</b> in 300 thousand candidates)	(2020)

• Recipient of Merit Certificate for being among the top 0.1% of successful candidates in *Physics* (2020)

# **Research Experience**

#### Hardware-efficient Secure Cache Design

Prof. Biswabandan Panda

(Jan. 2023 - Present)

Research Project

- O Extensively analyzed side-channel attacks and state-of-the-art cache designs which are secure against such attacks
- o Proposed modifications to the MIRAGE cache design aiming to reduce hardware overhead while retaining security
- $\circ$  Simulated the proposed cache design to ensure no Set-Associative Eviction occurs in  $10^{13}$  years of system lifetime
- Implementing the proposed cache design on **ChampSim** simulator to estimate performance overhead compared to a baseline non-secure cache design

#### **Secure Cache-line Reallocation**

Prof. Virendra Singh

(Jul. 2022 - Dec. 2022) EE691: R&D Project

- O Covered literature on multi-core processors, cache replacement policies, side channel attacks and their mitigation
- Implemented the PASS-P, Utility-based DCP (UCP), and static cache partitioning techniques on the SNIPER multi-core simulator and carefully analyzed results for different cache configurations
- O Performed extensive analysis of performance, sensitivity, re-allocated blocks and dead blocks for different benchmarks
- Proposed and implemented a modification to PASS-P using SNIPER simulator to preferentially re-allocate dead blocks with the aim to improve performance

# **Professional Experience**

### **Embedded Software Intern**

(May 2023 - Jul. 2023)

Texas Instruments India

Summer Internship

- Created a driver monitoring application for the AM62Ax Sitara processor using the GStreamer media framework
- Modified the existing GStreamer pipelines to enable stacking of multiple DNN models required for the application
- O Analyzed the boot flow of a competitor processor and created a boot loader porting guide for the AM62x processor
- o Extensively analyzed the existing documentation and Linux examples on the AM62x and suggested improvements

# **Key Projects**

#### Superscalar Processor Design

(Jul. 2022 - Nov. 2022)

Prof. Virendra Singh

CS683: Advanced Computer Architecture

- O Designed a 2-way OOO Superscalar processor with a Turing-complete instruction set architecture of 17 instructions
- O Implemented key components: Reservation station, Reorder Buffer, Execution pipelines, & Memory system in VHDL
- O Performed extensive software testing for all 17 instructions on GHDL and GTKWave simulations using a Testbench
- o Implemented an Assembler and a Bootloader in Python to dump user instructions into the memory of the processor

### **EEG Data Acquisition System**

(Jan. 2023 - Apr. 2023)

Prof. Siddharth Tallur and Prof. Laxmeesha Somappa

EE344: Electronic Design Lab

- o Extensively analyzed datasheets for various ADCs, regulators, microcontrollers, Wi-Fi modules and other peripherals
- Designed a 24-channel setup on a 4-layer PCB complete with the analog front-end, daisy-chaining for the ADCs, analog and digital power regulators, and peripheral interfacing using the 2 available SPI buses on the Microcontroller
- o Implemented a 4-channel easy-to-replicate modular design along with a 3D printed headgear for demo purposes
- O Bagged the Best Project Award out of 70+ teams for exemplary performance in the final demo and presentation

#### **VLSI Circuit Design**

(Jul. 2022 - Nov. 2022)

Prof. Dinesh Sharma

EE671: VLSI Design

- O Designed logic gates using CMOS, pseudo-NMOS, CVSL, and CPL design styles, and analyzed output characteristics
- o Implemented a 16-bit Brent Kung logarithmic fast adder in VHDL and validated design using ModelSim simulations
- O Used the Dadda Reduction Algorithm to optimize efficiency of a 16-bit Multiply and Accumulate circuit in VHDL

#### **RISC Processor Design**

(Jan. 2022 - Apr. 2022)

Prof. Virendra Singh

EE309: Microprocessors

- Designed and implemented the 16-bit IITB RISC-22 Microprocessor, capable of running a total of 17 instructions using both 6-stage Pipelining and Multicycle implementations
- $\circ$  One of the few teams to optimize the pipelined processor using **Hazard mitigation**, **Forwarding** & Branch prediction
- O Performed software testing for all instructions using Intel Quartus Environment and the ModelSim HDL simulator

### Valet Parking Bot

(Jan. 2023 - Apr. 2023)

Prof. Paritosh Pandya and Prof. Kavi Arya

CS684: Embedded Systems

- O Interfaced the tracker sensors, proximity sensors, and position encoders using the Arduino present on the Alphabot
- O Implemented and tested algorithms for Line following, Obstacle avoidance, and Parking in the Heptagon language
- O Wrote the controller in Embedded C to set up the sensor and motor drivers and interfacing with the Heptagon code

#### **VLSI Circuit Partitioning**

(Jul. 2022 - Nov. 2022)

Prof. Virendra Singh

EE677: Foundation of VLSI CAD

- Studied and implemented graph partitioning algorithms and heuristics such as the Kernighan-Lin Algorithm,
   Clustering Based Heuristic, and Hagen Kahng EIG Algorithm
- O Visualized the algorithms using the plotting tools of matplotlib and networkx libraries and compared their performance

# Digital Circuit Design

(Jul. 2021 - Nov. 2021)

Prof. Maryam Shojaei Baghini

EE214: Digital Circuits Lab

- O Acquired the knowledge of Finite-state machines and the methodology for implementing them using D-FlipFlops
- o Implemented a 4-bit Sequence Generator with D-FlipFlops using Sequential and Behavioral modelling in VHDL
- O Performed software testing using Quartus simulations and hardware testing using Scanchain on the Krypton board

#### **Microprocessor Implementations**

(Jan. 2022 - Apr. 2022)

Prof. Saravanan Vijaykumaran

EE337: Microprocessors Lab

- Designed and tested a two-party, password-secure ATM capable of taking action inputs from keyboard using UART
- o Implemented a reaction timer in Assembly to display the time it takes for the user to respond to a stimulus (in ms)
- O Developed a subroutine capable of generating voltage waveforms corresponding to different music note frequencies
- Interfaced an LM35 sensor with the microcontroller using an ADC, through serial peripheral interfacing, to monitor and display real-time ambient temperature

# Other Projects

#### Predicting the RUL of EV Batteries

(Jul. 2021 - Nov. 2021)

Prof. Amit Sethi

DS203: Programming for Data Science

- O Achieved an R2 score of 98.09 for estimating the RUL of EV Lithium batteries using an XGBoost regression model
- o Performed EDA on the Charging, Discharge and Impedance cycles for Li-ion batteries using NASA's PCoE Datasets
- O Understood and tested various models such as SVR, Multilayer Perceptron, LSTM, Random Forest as well as various Boosting Algorithms

#### **General Purpose GPUs**

(May 2022 - Jul. 2022)

Prof. Virendra Singh

Research Project

- o Reviewed literature about analyzing and leveraging a Decoupled LLC design and implementing it on GPGPU-Sim
- Studied and reviewed the SIMT Core, Memory systems and the programming model related to GPU architecture
- o Performed various benchmark simulations on the GPGPU-Sim simulator and carefully analyzed the outputs received

**Operating Systems** 

(May 2022 - Jul. 2022)

Maths and Physics Club, IIT Bombay

Summer of Science

- O Studied various Scheduling policies, Process APIs, and Context switching used to facilitate CPU Virtualization
- O Covered different Memory APIs, Segmentation, Paging, TLBs, and Swapping in context of Memory Virtualization

# Postitions of Responsibility

Served as an undergraduate teaching assistant for a batch of 200+ students, with the responsibility of conducting doubt-solving sessions, and academically mentoring students over the duration of the following course: o EE309: Microprocessors (Jan. 2023 - Apr. 2023)

# **Technical Skills**

Languages C, C++, VHDL, Verilog, Python, Assembly, Heptagon

Intel Quartus, Autodesk Fusion 360, GStreamer, Keil µVision, GHDL, MATLAB, Ngspice, **Software** 

ArduinoIDE, AutoCAD, Solidworks, GNU Radio, LATEX

Simulators ChampSim, Sniper, GPGPU-Sim

#### Courses Undertaken

VLSI Design, Foundation of VLSI CAD, Microprocessors, Electronic Design Lab,

Digital Systems, Analog Circuits, Communication Networks, Information Theory & **Electrical Engineering** 

Coding, Probability & Random Processes, Electronic Devices & Circuits, Control

Systems, Power Engineering, Electromagnetic Waves

Advanced Computer Architecture, Embedded Systems, Principles of Data and **Computer Science** 

System Security, Computer Programming & Utilization

Mathematics Calculus, Linear Algebra, Differential Equations, Complex Analysis Miscellaneous Economics, Sociology, Quantum Physics and Application, Biology

# **Extracurriculars**

 Completed one year of training under the National Cadet Corps, IIT Bombay (2021)

o Awarded a Special Mention out of a total of 82 students in the LATEX bootcamp conducted by the Under-Graduate Academic Council, IIT Bombay (2021)

o Designed and assembled a remote-controlled plane and participated in the RC Plane Competition conducted by the Aeromodelling Club, IIT Bombay (2021)