Anubhav Bhatla

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Research Interests

I am broadly interested in Computer Systems & Architecture and Hardware Security. This includes advanced topics such as secure and randomized caches, cache partitioning techniques, and branch predictor designs. I am also interested in VLSI circuit design.

Education

Indian Institute of Technology Bombay *(Nov 2020 - Present)*

Integrated Bachelors and Masters of Technology (Dual Degree) in Electrical Engineering *GPA: 9.13/10*

Minor Degree in Computer Science and Engineering

Publications

- A. Bhatla*, Navneet*, M. Qureshi, B. Panda. **OASIS: Enabling Provably Secure Randomized Caches at Ultra-Low Cost**. *Under review at the International Symposium on High-Performance Computer Architecture* ***(HPCA'25)***
- A. Bhatla*, Navneet*, B. Panda. **The Maya Cache: A Storage-efficient and Secure Fully-associative Last-level Cache**. *Presented at the International Symposium on Computer Architecture* ***(ISCA'24)***

Scholastic Achievements

- Awarded **Undergraduate Research Award** by IIT Bombay for excellence in research and development *(2023)*
- Ranked $\mathbf{4^{th}}$ among **85** students enrolled in the Electrical Department Dual Degree program *(2024)*
- Scored a perfect **10 SPI** (Semester Performance Index) in the $\mathbf{8^{th}}$ academic semester *(2024)*
- Secured **All India Rank 266** in *Joint Entrance Exam, JEE (Advanced)* among 160 thousand candidates *(2020)*
- Acquired an **All India Rank 490** in *Joint Entrance Exam, JEE (Mains)* among 1.1 million candidates *(2020)*
- Qualified for **Indian National Olympiad (INO)** in *Astronomy, Chemistry & Physics* *(2019)*
- Awarded the *Kishore Vaigyanak Protsahan Yojana* (**KVPY**) fellowship with **All India Rank 337** *(2018)*

Research & Work Experience

Practical and Secure Cache Design at Ultra-Low Cost *(Dec 2023 - Present)*

Prof. Biswabandan Panda, IIT Bombay & Prof. Moinuddin Qureshi, Georgia Tech *Research Project*

- Designed **Oasis**, a secure and practical last-level cache design which provides complete **security** against eviction-based cache attacks at an **ultra-low cost** and with **minimal changes** compared to a traditional non-secure cache
- Performed extensive simulations using the **bucket-and-balls model** to show complete security in a system lifetime
- Implemented the cache design on the **ChampSim** multi-core simulator to obtain performance normalized to the baseline

Hardware-efficient Secure Randomized Cache Design *(Jan 2023 - Jul 2024)*

Prof. Biswabandan Panda, IIT Bombay *Research Project*

- Proposed **Maya**, a secure fully-associative last-level cache design which provides complete **security** against eviction-based cache attacks while **saving 2% storage**, **5% power**, **13% energy**, and **28% area** compared to a non-secure baseline cache
- Designed and simulated a security model for the Maya cache to ensure **no set-associative evictions** occur in $\mathbf{10^{16}}$ **years**
- Modelled the Maya cache in the **CacheFX** simulator to showcase performance against **occupancy-based attacks**

Branch Predictor Partitioning for Performance *(Apr 2024 - Present)*

Prof. Dean Tullsen, University of California, San Diego *Research Project*

- Studying how the **Half&Half** branch predictor partitioning can improve performance for certain application pairs
- Used **perf** to identify application pairs from **SPEC2017** suite which are critical in terms of conditional branch misses
- Implementing the modifications suggested in Half&Half on top of the **LLVM** compiler to partition the branch predictor

Understanding the Security of Secure Randomized Caches *(Apr 2024 - Present)*

Prof. Biswabandan Panda & Prof. Sayandeep Saha, IIT Bombay *Masters' Thesis Project*

- Performing a thorough **security analysis** of various state-of-the-art secure cache designs such as Mirage, Maya, and Oasis to understand the **minimal set** of **necessary and sufficient additions** required to make a traditional cache secure
- Working on a secure & morphable LLC which requires **minimal changes** on top of a traditional cache to make it secure

Secure Cache-line Reallocation in Partitioned Caches *(Jul 2022 - Nov 2022)*
Prof. Virendra Singh, IIT Bombay *Research Project*
- Studied and implemented the **PASS-P**, **UCP** & static cache partitioning for multi-core systems on the **Sniper** simulator
- Conducted **thorough analysis** of performance, sensitivity, re-allocated blocks and dead blocks for different benchmarks
- Implemented **modifications to PASS-P** using Sniper to preferentially **reallocate dead blocks**, reducing them by over **10%**

Embedded Software Intern *(May 2023 - Jul 2023)*
Texas Instruments India, Bangalore *Internship*
- Created a **driver monitoring application** for the AM62Ax Sitara processor using the **GStreamer** media framework
- Modified the existing GStreamer pipelines to enable **stacking of multiple DNN models** required for the application
- Analyzed the **boot flow** of various processors and created a boot loader **porting guide** for the Sitara AM62x processor

Teaching & Mentorship Experience

Department Academic Mentor *(May 2024 - Present)*
Student Mentorship Program, IIT Bombay *Mentorship*
- Selected as part of a **54**-member team handpicked after a rigorous process of meticulous interviews and peer reviews
- Appointed to mentor **6** sophomore students with their academics, extra-curriculars, career paths and research journey
- Contributed to the department website blog and collected course feedback, providing academic help to **1300+** students

Teaching Assistant
CS683: Advanced Computer Architecture, EE229: Signal Processing, EE309: Microprocessors
- Served as an undergraduate teaching assistant for **100+** Electrical Engineering and Computer Science students
- Responsible for creating **assignment problems**, conducting **doubt-solving sessions**, and helping with the **course evaluation**

Academic Projects

Computer Architecture Projects

Sliced-Out-of-Order Core Implementations *(Jul 2023 - Nov 2023)*
Prof. Virendra Singh, IIT Bombay *EE748: Advanced Computer Architecture - II*
- Reviewed literature on **sliced-OoO** cores which add minimal components on top of InO cores to extract **MLP**
- Implemented the **backward dependency algorithm** and hardware structures proposed by the state-of-the-art **Load-Slice core** using the **gem5** simulator and extended it to implement the modifications suggested by **Freeflow core**

2-way OoO Superscalar Processor Design *(Jul 2022 - Nov 2022)*
Prof. Virendra Singh, IIT Bombay *CS683: Advanced Computer Architecture - I*
- Designed a **2-way Out-of-Order Superscalar** processor with a Turing-complete ISA comprising of **17** instructions
- Implemented key components: Reservation Station, Reorder Buffer, execution pipelines & memory system in **VHDL**
- Conducted thorough software testing for all 17 instructions on **GHDL** and GTKWave simulations using a testbench

6-stage Pipelined Processor Design *(Jan 2022 - Apr 2022)*
Prof. Virendra Singh, IIT Bombay *EE309: Microprocessors*
- Designed and implemented a **16-bit, 6-stage pipeline** processor, capable of efficiently running a total of **17** instructions
- One of the few teams to optimize the processor using **Hazard mitigation**, **Forwarding** & **Branch prediction** techniques
- Performed software testing for all the instructions using **Intel Quartus** Environment and the **ModelSim** HDL simulator

General Purpose GPUs *(May 2022 - Jul 2022)*
Prof. Virendra Singh, IIT Bombay *Reading Project*
- Reviewed **GP-GPU architecture** for leveraging a **Decoupled LLC** design and implementing it on GPGPU-Sim simulator
- Performed various benchmark simulations on the **GPGPU-Sim** simulator and carefully analyzed the outputs received

VLSI Design Projects

FPGA Accelerator for Spiking Neural Networks *(Jan 2024 - Apr 2024)*
Prof. Sachin Patkar, IIT Bombay *EE705: VLSI Design Lab*
- Implemented a **hardware-efficient** accelerator for an **IF neuron**-based SNN, capable of classifying **MNIST** images
- Utilized **BRAM** IP blocks in **Vivado** to store model weights for **800+** neurons and the spike-encoded input images

Efficient VLSI Circuit Partitioning *(Jul 2022 - Nov 2022)*
Prof. Virendra Singh, IIT Bombay *EE677: Foundation of VLSI CAD*
- Studied and implemented VLSI circuit partitioning algorithms such as **Kernighan-Lin** and **Hagen Kahng EIG**
- Performed comparative performance analysis & visualization of the algorithms using matplotlib and **networkx** libraries

CMOS Implementation of Low Power Equi-Prop System *(Jul 2023 - Nov 2023)*
Prof. Udayan Ganguly, IIT Bombay *EE746: Neuromorphic Engineering*
- Implemented **Spiking Equilibrium Propagation** real-time learning algorithm in **45nm CMOS** technology using **LTSpice**
- Achieved an **energy-efficient** circuit with $\mathbf{82.7\mu W}$ total power and only $\mathbf{8.8\mu W}$ consumed by the synapse circuit

Voltage-Controlled Oscillator Design *(Jan 2024 - Apr 2024)*
Prof. Rajesh Zele, IIT Bombay *EE619: RF Microelectronics Chip Design*
- Designed and implemented a **low-power cross-coupled** voltage-controlled oscillator using **Cadence Virtuoso**
- Achieved a frequency of 6GHz, phase noise of -117dBc/Hz, tuning range of 28MHz, and a power budget of 3mW

Digital VLSI Circuit Design *(Jul 2022 - Nov 2022)*
Prof. Dinesh Sharma, IIT Bombay *EE671: VLSI Design*
- Created a 16-bit **Brent Kung** logarithmic fast adder in **VHDL** and validated the design using **ModelSim** simulations
- Utilized the **Dadda Reduction Algorithm** to optimize the efficiency of a 16-bit **Multiply-and-Accumulate** circuit

Low-Power OTA Design with RC Compensation *(Jul 2023 - Nov 2023)*
Prof. Rajesh Zele, IIT Bombay *EE618: CMOS Analog VLSI Design*
- Designed a **low-power 2-stage** Operational Transconductance Amplifier with **RC Compensation** using **Cadence Virtuoso**
- Attained 50dB gain, unity gain frequency of 108MHz & phase margin of 67.4°, within a 0.22mW power budget

High-Level Synthesis Design *(Jul 2023 - Nov 2023)*
Prof. Madhav Desai, IIT Bombay *EE789: Algorithmic Design of Digital Systems*
- Designed various digital systems in **Algorithmic assembly**, automatically generating VHDL & verified using GHDL
- Optimized matrix multiplication using **loop-unrolling** & **parallel computations** with additional hardware instances

Other Projects

24-channel EEG Data Acquisition System *(Jan 2023 - Nov 2023)*
Prof. Siddharth Tallur, IIT Bombay *Supervised Research Exposition & EE344: Electronic Design Lab*
- Designed a **24-channel** setup on a **4-layer PCB** using **daisy-chained** ADCs and peripheral interfacing using **SPI**
- Implemented an additional **4-channel modular** signal acquisition setup with **3D-printed headgear** for demo purposes
- Received the **Best Project Award** out of **60+** teams for exemplary performance throughout the duration of the project

Optimal Device Design for NIPIN Memory Selector *(Jan 2024 - Apr 2024)*
Prof. Udayan Ganguly, IIT Bombay *EE724: Nanoelectronics*
- Performed pen-paper analysis for **NIPIN** device & verified it using **TCAD** simulations on **Synopsys Sentaurus Workbench**
- Optimized the **idealty factor** to **1.33** by introducing different ratios of **Germanium** in the p-regions instead of pure Si
- Recognized as the **best project** out of **10+** groups for our extensive analysis and experimentation with NIPIN

Arduino-based Valet Parking Bot *(Jan 2023 - Apr 2023)*
Prof. Paritosh Pandya & Prof. Kavi Arya, IIT Bombay *CS684: Embedded Systems*
- Interfaced tracker sensors, proximity sensors, and position encoders using the **Arduino** board present on the **Alphabot**
- Implemented the controller in **Embedded C** & line following, obstacle avoidance, and parking algorithms using **Heptagon**

Technical Skills

Languages	C, C++, VHDL, Verilog, Python, Assembly (8085), Algorithmic assembly (Aa), Heptagon
Software	Intel Quartus, Vivado, Autodesk Fusion360, GStreamer, Cadence Virtuoso, Synopsys Sentaurus, Keil μVision, MATLAB, LTSpice, Ngspice, ArduinoIDE, GNU Radio, AutoCAD, Solidworks
Simulators	ChampSim, gem5, Sniper, GPGPU-Sim, CacheFX

Courses Undertaken

Computer Systems: Advanced Computer Architecture - I, Advanced Computer Architecture - II, Operating Systems, High-Performance Scientific Computing, Microprocessors

Hardware Design: VLSI Design, Algorithmic Design of Digital Systems, RF Microelectronics Chip Design, Testing & Verification of VLSI Circuits, CMOS Analog VLSI Design, VLSI Design Lab, Electronic Design Lab, Neuromorphic Engineering, Foundation of VLSI CAD, Nanoelectronics

Computer Science: Data Structure & Algorithms, Design & Analysis of Algorithms, Principles of Data & System Security, Embedded Systems, Discrete Structures

Electrical Engineering: Communication Networks, Nanoelectronics, Signal Processing, Control Systems