IQ Modulator and Practical Considerations

EE340: Prelab Reading Material for Lab 5

AUTUMN 2022

Any arbitrary passband signal $s_p(t)$ with center frequency f_c can be written as

$$s_p(t) = Re\{s(t)e^{j2\pi f_c t}\} = s_I(t)cos(2\pi f_c t) - s_Q(t)sin(2\pi f_c t)$$

where $s(t) = s_I(t) + js_Q(t)$ is is a complex baseband signal consisting of the two independent real baseband signals $s_I(t)$ and $s_Q(t)$. The signal s(t) is also called the complex envelope of $s_p(t)$. Therefore, an IQ modulator is typically used for upconverting a complex baseband signal to a passband IF (intermediate frequency) or RF (radio frequency) signal, as shown in Fig. 1a. In a similar way, an IQ demodulator is used for downconverting a passband RF or IF signal to the complex baseband signal, as shown in Fig. 1b.

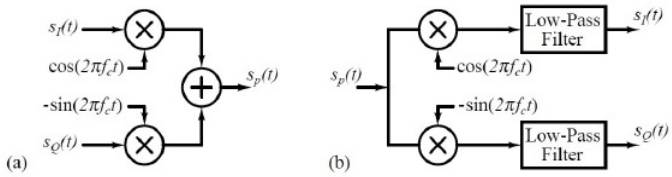

Figure 1: Flowgraph of (a) an IQ modulator, and (b) an IQ demodulator

Among the hardware used in your experiments, the RTL-SDR dongle basically implements an IQ demodulator, which finally gives out the digitized versions (obtained using analog-to-digital converters) of the baseband signals to the computer through the USB port. For implementing the IQ modulator, the printed circuit board shown in Fig. 2 has been developed in-house (i.e. in the Wadhwani Electronics Lab). In this experiment, you will be using this board for carrying out complex multiplication in hardware to obtain arbitrary passband signals.

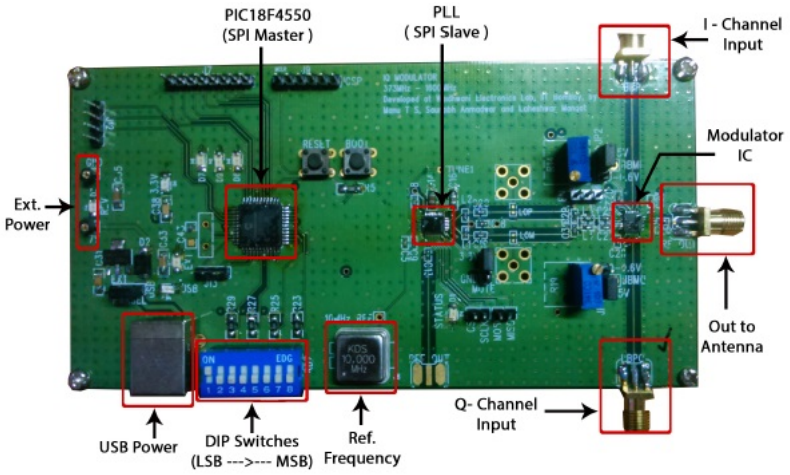

Figure 2: The IQ modulator board developed at the Wadhwani Electronics Lab.

1 The IQ Modulator Board

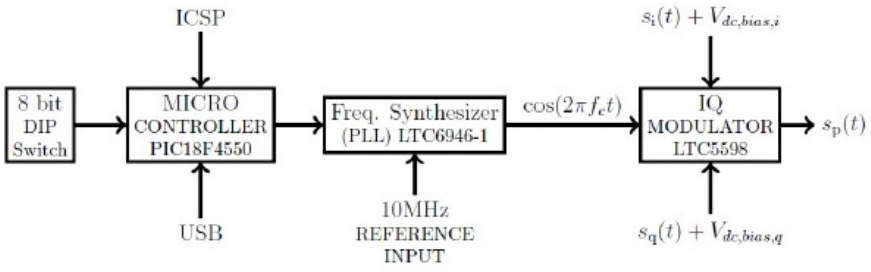

Figure 3: The block diagram of the IQ modulator board.

The block diagram of the IQ modulator board is shown in Fig. 3. It consists of several components, among which, the following ones are worth mentioning:

(a) **The IQ Modulator IC**: In these experiments, the role of this IC is to upconvert the analog baseband I and Q signals to the passband signal $s_p(t)$ at the carrier frequency. The local oscillator (LO) signal, i.e. the carrier frequency here, is generated by an on-board frequency synthesizer (or a phase locked loop). Internally, the IQ modulator IC uses a poly-phase filter to generate 0^o and 90^o phases of the carrier frequency from the LO signal. These two phases are then multiplied with the analog baseband I and Q signals s_I (t) and $s_Q(t)$, and the resulting outputs are combined to obtain the desired passband signal $s_p(t)$ at the output port, as shown in Fig. 3.
Caution: For proper biasing of the internal IQ modulator circuitry, the baseband I and Q signals also have to include DC biases, which should NOT exceed 0.6V (the nominal DC bias voltage is around 0.45 V).

(b) **The Phase Locked Loop (PLL)** for Frequency Synthesis: The on board PLL generates the LO signal for modulation or upconversion of the baseband signals. The input to the PLL is a fixed 10MHz clock (also known as the reference frequency f_{ref}) coming from an on-board crystal oscillator. The PLL IC has a voltage controlled oscillator (VCO) followed by a configurable frequency divider of division ratio N; as shown in Fig. 4. The feedback loop in the PLL ensures that the frequency divider output phase (and hence frequency) exactly matches the reference clock phase (and frequency). The phase error is basically determined by the time difference between the rising edges of the reference clock and the frequency divider output, and should be practically zero when the PLL is locked. For a given fref and N; the VCO output frequency in the locked PLL is $f_{out} = \mathrm{N}.f_ref$ (prove it yourself). The frequency division factor N is always >1, but it is possible to achieve effectively a non-integer value of N using some tricks (discussion on which is beyond the scope of this material).

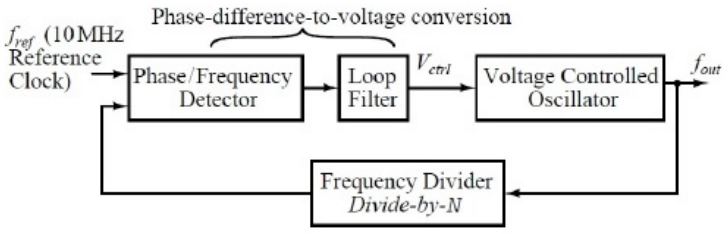

Figure 4: The block diagram of a PLL used as a frequency synthesizer.

Various parameters of the PLL, such as the loop bandwidth, the loop settling behaviour and the frequency division ratio are decided by configuration register bits, which are programmed

by an on-board micro- controller. There is also a lock-bit in the PLL. The red "STATUS" LED on the board glows when this lock-bit is "HIGH", i.e. the PLL is locked.

(c) **The Micro-Controller:** The micro-controller (PIC18F) on the board configures the twelve 8-bit registers of the PLL at the start-up or when the controller is reset. All the 96 bits corresponding to these twelve registers have to be set individually for setting various parameters of the PLL on the board. The controller talks with the PLL through an SPI link, in which, the PLL is the slave and the micro-controller is the master (you will be studying the SPI interface in EE337).

(d) The DIP Switch: The role of this switch is to set the PLL register bits so as to change the carrier frequency going to the IQ modulator IC. Each group has to use a distinct DIP switch setting so that different groups are using different frequency channels. The DIP switch sets various frequency divider ratios in the PLL, which decides the PLL output frequency. For your group, you will be using the following setting:

$$DIP - switch - value = 2x < YourGroupNo. >$$

which gives the carrier frequency in the form: $f_c = f_{c0} + f_{step}$ x $< DIP - switch - value >$.

2 Non-Idealities in a Practical IQ Modulator

(a) **Carrier Feedthrough:**The baseband inputs s_I (t) and s_Q(t) are supposed to carry some DC biases $V_{dc,bias,i}$ and $V_{dc,bias,q}$, respectively, so that they nullify the effects of on-chip DC-reference bias voltages (with DC offsets) for these inputs $V_{dc,ref,i}$ and $V_{dc,ref,q}$. The combined output at the IQ modulator, after accounting for these biases and offsets is

$$s_p(t) = s_I(t)cos(2\pi f_c t) + [V_{dc,bias,i} - V_{dc,ref,i}] \times cos(2\pi f_c t)$$
$$-s_Q(t)sin(2\pi f_c t) - [V_{dc,bias,q} - V_{dc,ref,q}] \times sin(2\pi f_c t)$$

If the carrier has to be suppressed at the output perfectly, it must be ensured that $V_{dc,bias,i} - V_{dc,ref,i} = 0$ and $V_{dc,bias,q} - V_{dc,ref,q} = 0$, by independently adjusting controls for $V_{dc,bias,i}$ and $V_{dc,bias,q}$ on the board. Due to imperfect adjustment, unmodulated carrier leaks to the output , this phonemenon is also known as LO or carrier feedthrough.

(b) **I-Q Imbalance Resulting in Finite Image Rejection Ratio:**If our message signal is $\cos(2\pi f_{mt})$ and we wish to carry out single sideband (SSB) modulation, we can use the signals $s_I(t) = cos(2\pi f_{mt})$ and $s_Q(t) = sin(2\pi f_m t)$, as inputs for the I and Q channels of the IQ modulator, respectively. This should ideally generate the signal $s_p(t) = cos(2\pi(fm + fc)t)$ at the output of the modulator.
However, due to mismatches (or circuit imperfections), the phase differences between the I and Q channel inputs and the two carrier components are not exactly 90^o. Similarly, the amplitudes of I and Q channel inputs and the two carrier components do not match exactly. To account for these relative mismatches, the Q channel input can be rewritten as $s_Q(t) = (1 + \delta)sin(2\pi f_m t + \phi)$, if $s_I(t)$ is unchanged. As a result, in addition to the desired signal at the frequency $f_c + f_m$, an undesired signal component is also present at $f_c - f_m$, as shown in Fig. 5b. This component is called the image component. The ratio of power in the desired signal component to the power in the image component is called Image Rejection Ratio (IRR). If $\delta << 1$ and $\phi << 1$ where ϕ is expressed in radians, prove yourself that

$$\text{IRR (in dB)} = 10\log[\frac{4}{\delta^2 + \phi^2}]$$

Independent adjustment of the relative phase and amplitude levels may be able to reduce the IRR in your experiments to around 40 dB.

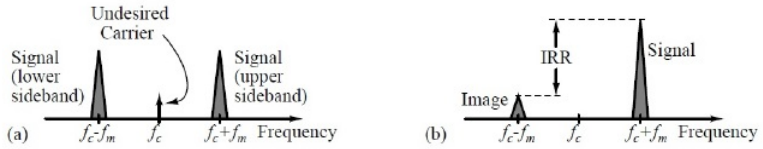

Figure 5: The block diagram of a PLL used as a frequency synthesizer.