EE324 : Controls Lab
Experiment - 3 : Noise Cancellation in Headphones

Batch 4

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1 Aim of the experiment

To design and implement an analog circuit for noise cancellation in headphones

2 Objectives

1. To achieve an attenuation of $20dB$ when a noise of $100Hz$ frequency is applied.
2. To design an analog compensator for the system such that the compensated system has a gain margin of atleast $5dB$ and a phase margin of atleast $30°$

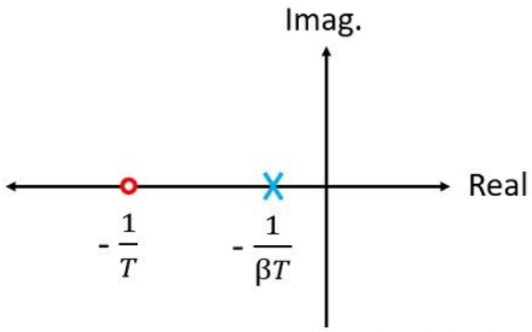
3 Theory

We are required to implement a lag compensator to stabilise our system and achieve required parameters. For a lag compensator, the general transfer

function is as follows:

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{\beta}\frac{[s+\frac{1}{T}]}{[s+\frac{1}{\beta T}]} \tag{1}$$

where $\beta > 1$.
The pole lies at the location -1/βT and the zero at -1/T, thus the pole is more dominating than the zero. Due to this, a negative phase angle is introduced called the lag.



4 Code

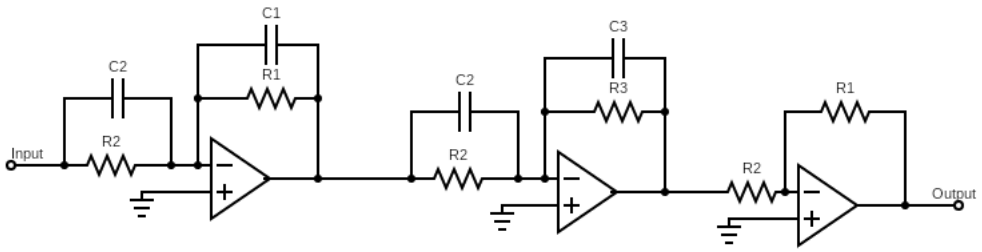
The code for the design of the lag compensator is as follows:

```
freq_sys = [40,50,60,70,80,90,100,120,140,200,280,450,
600,700,800,900,1000,1320,1400,1700,2000,2500,3180,3400,
3500,3600,3800,4000,4230,4500,4730,4900,5000,5300,5590,
6000,6310,6500,6970,7400];

vin = [0.592,0.616,0.584,0.584,0.616,0.624,0.664,0.68,
0.616,0.584,0.576,0.576,0.568,0.568,0.576,0.552,0.552,
0.552,0.552,0.584,0.552,0.584,0.632,0.616,0.624,0.616,
0.8,0.616,0.96,0.96,0.98,1.06,1.08,0.8,0.8,0.82,0.8,
0.8,0.82,0.78];

vout = [0.7,1.22,1.84,2.68,3.56,4.92,5.76,7.76,8.8,7,
6.16,5.52,6.56,6.96,5.2,3.76,5.28,6.32,6.96,4.4,3.28,
2.4,1.92,1.84,1.28,0.62,0.5,0.42,1.12,2.8,1.5,0.98,
1.36,2.36,2.76,3.72,4.46,4.16,2.32,1.22]

```

```
amp_sys = vout./vin;

phase_sys = [153.6122,156.4218215,180,170.4059318,
160.5287794,144.3146653,132.8334281,90,58.99728087,
16.6015496,0,-9.594068227,-25.37693353,-41.8103149,
-53.13010235,-51.05755873,-41.8103149,-90,-112.6198649,
-160.5287794,-180,-240,-270,-340.5287794,-360,
-383.5781785,-450,-513.6122,-540,-531.7867893,-630,
-581.4096221,-540,-588.1896851,-630,-681.3178125,-720,
-746.3878,-810,-953.1301024];

s = tf('s')

p1 =10
z1 =3000
p2 =10
z2 =2000

gain = 4.3e3;
comp = gain*(s/z1 + 1)*(s/z2 + 1)/((s/p1 + 1)*(s/p2 + 1));
bode(comp)
[gainplot, phaseplot, w_plot] = bode (comp, 2*pi*freq_sys);

gain_total = reshape(gainplot, 1,40).*amp_sys';
phase_total = reshape(phaseplot, 1,40)+phase_sys';

plot(log10(freq_sys),phase_total' )
hold on
plot(log10(freq_sys),phase_sys )
legend(["Comp", "Init"])
title("Phase Plot")
hold off
plot(log10(freq_sys),20*log10(gain_total') )
hold on
plot(log10(freq_sys),20*log10(amp_sys) )
legend(["Comp", "Init"])
title("Gain Plot")
hold off
```

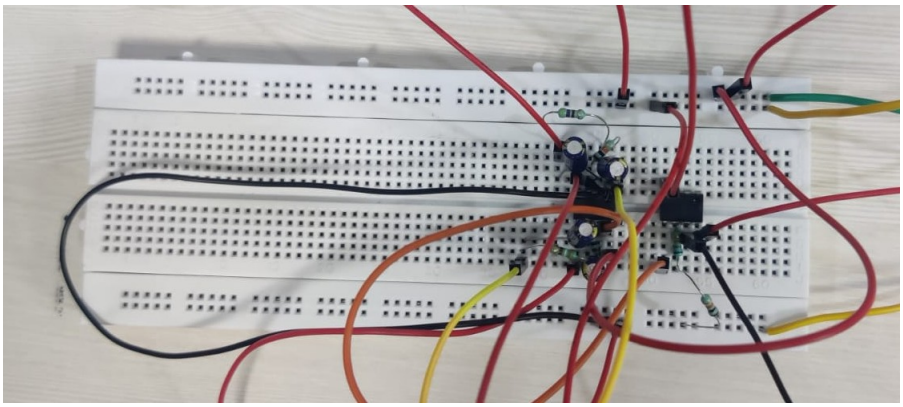
5 Hardware Design

Given below is the circuit diagram we used for designing the compensator:



The first and the second opamps are responsible for implementing a first-order lag compensator and their combined effect gives us the required second-order compensator. The third opamp is responsible for setting the final gain of the compensator.

Given below is the final circuit diagram for the implementation of the designed compensator on hardware:



6 Challenges Faced

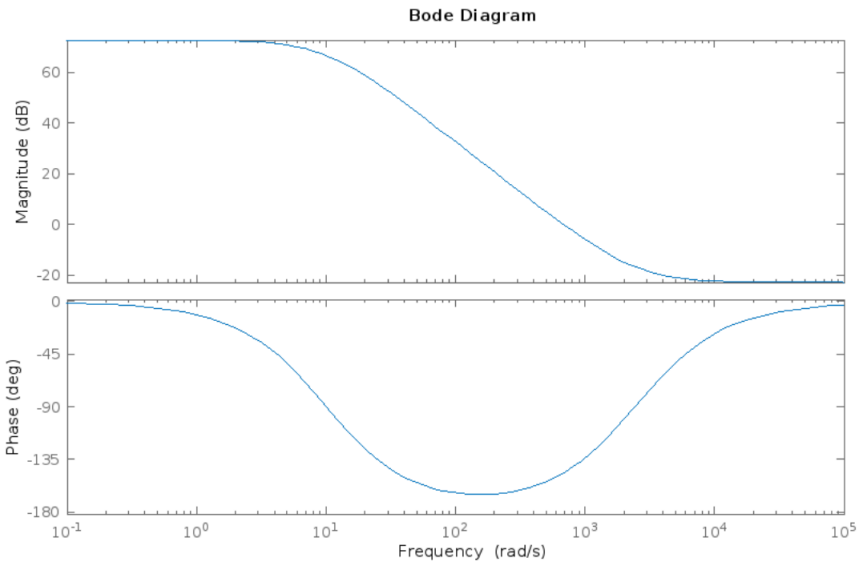
- Initially, we were trying to design the compensator using a 1^{st} order system but the problem was that we needed a roll-off of atleast $25dB$ per decade but a 1^{st} order is limited to $20dB$ per decade. So, we decided to use a 2^{nd} order system.

- For our compensator design on hardware, we required an RC value equal to 0.1 for the two poles at $10Hz$. For this we needed extremely large values of R and C at the order of Mega Ohms and Micro Farad respectively, which we were eventually able to find. We also had to use approximate values for the resistances and capacitances as the exact values weren't available to us in the lab.

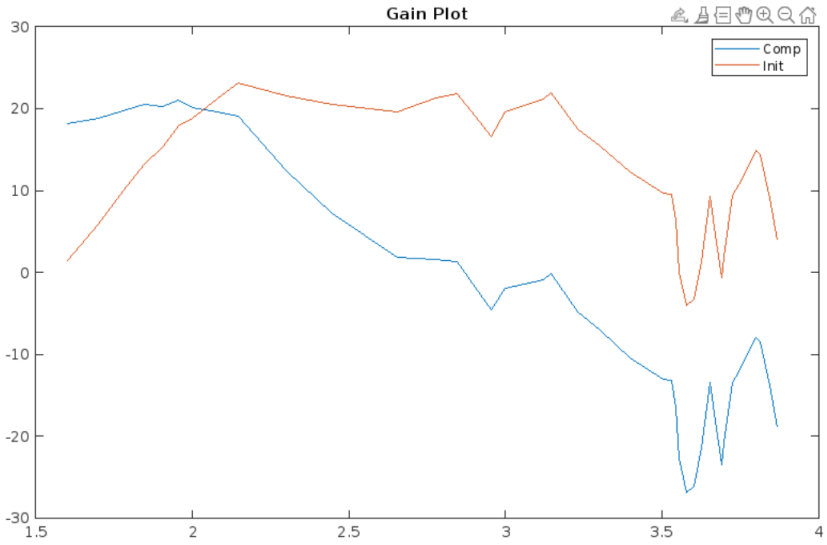
- We took the readings using the prescribed method but our phase plot had an increasing trend with frequency. Even after multiple attempts to find the problem, we couldn't resolve the issue. In the end, our TA provided us the readings using which we proceeded with the design of the compensator.

7 Observations

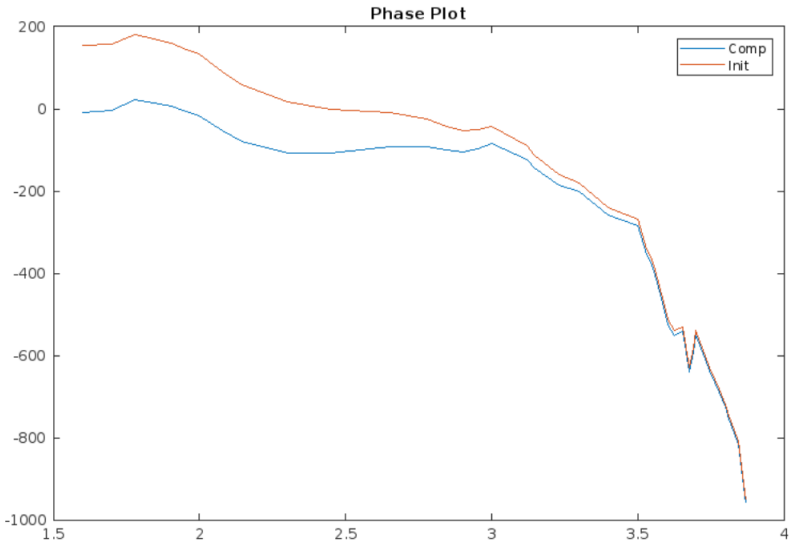
Given below are the bode plots for the above designed compensator:



Given below is the gain plot for the uncompensated and the compensated systems:



Given below is the phase plot for the uncompensated and the compensated systems:



8 Results and Conclusion

Given below are locations of the poles and zeroes used:

p_1	10 Hz
p_2	10 Hz
z_1	2000 Hz
z_2	3000 Hz

Given below are the final obtained parameters for the compensated system:

Attenuation at $100Hz$	$20.02dB$
Gain Margin	$4.8dB$
Phase Margin	78°

To conclude, we were able to successfully design a lag compensator for our unstable system which satisfies the required design specification of gain, phase margins and noise attenuation.