EE236 Endsem Exam

Endsem Hands-on (50 marks) Date: November 6, 2022

Instructions:

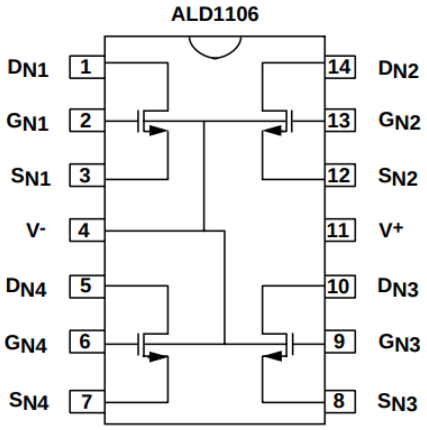
i This document is for the hands-on part of the exam.

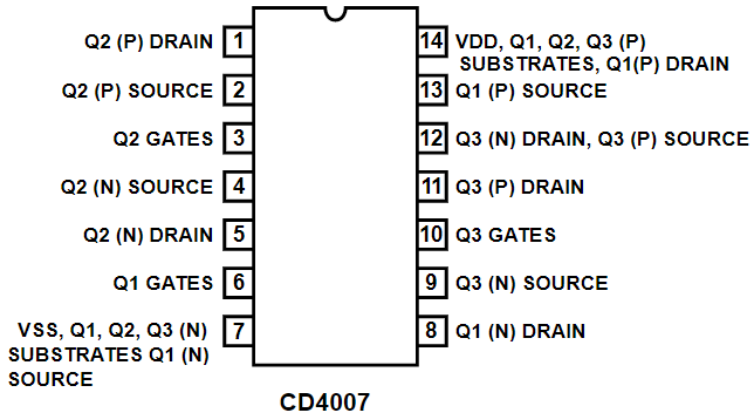
ii You may use previous handouts, supporting documents, your own net-lists and reports. Using the internet is prohibited. Mobile phones must be **switch off**.

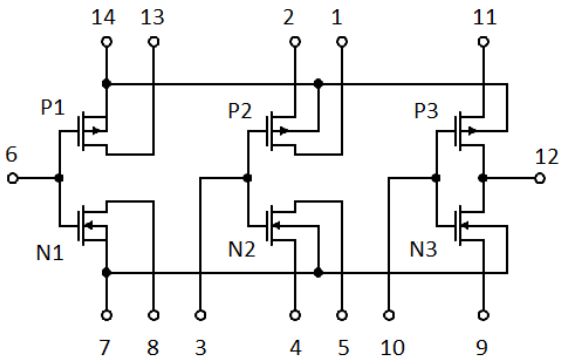
iii Make one document consisting of your observations, plots, results and answers. You will need to submit this document as your response.

iv You don't need a voltage greater than $5V$ for any part of the circuit. Hence, derive all voltages using constant $5V$ supply and potentiometers.

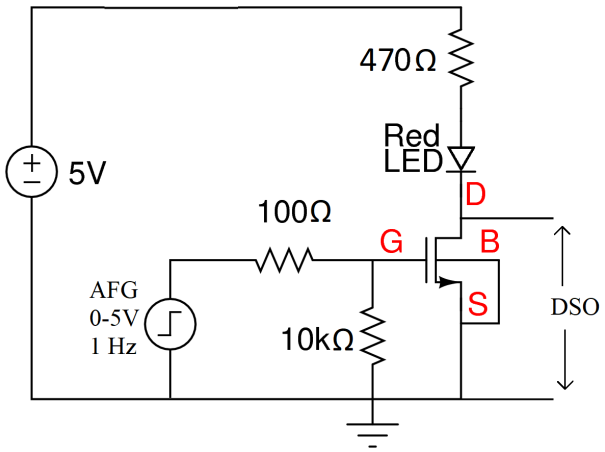
You are provided with ALD1106 CMOS IC and CD4007 CMOS IC.
The pin diagrams are given here.







1. **Testing the equipment and devices** : Before you start, make sure you test the NMOS of ALD1106 you want to use by following the given circuit.



Apply square pulse of $5V$ amplitude, 1 Hz frequency as input to the gate. Tap the output from drain terminal on the DSO. This circuit will test the function generator (AFG), power supply and oscilloscope (DSO).
Test your DMM by measuring the current through a $10k\Omega$ with $5V$ supply.
Show the output to your TA after (or within) 20 minutes to confirm that your equipment and device are working. 5 *marks*

2. In the first part, you will characterize an NMOS in ALD1106 IC. Choose the first NMOS in ALD1106 (pin numbers 1,2,3,4). Measure the output (I_D vs V_{DS}) characteristics and the transfer (I_D vs V_{GS}) characteristics in saturation region.

   a Obtain the output characteristics I_D vs V_{DS} for 3 different values of V_{GS} ($1V,\ 2V,\ 3V$) and plot them on the same graph. Extract the output resistance r_o in saturation region for $V_{GS} = 2V$. 5 *marks*

   b Now bias the NMOS in saturation region by applying a large V_{DS} (say $5V$) and plot I_D vs V_{GS}. From the plot, extract the threshold voltage V_T and maximum trans-conductance g_m. (Keep the body terminal at $0V$) 5 *marks*

   c Finally, apply body bias to the NMOS by changing V_{BS}. Find I_D vs V_{GS} (for a fixed V_{DS} of $5V$) for 2 different body bias voltages of $V_{BS} = 0.5V$ and $V_{BS} = -0.5V$; find out the threshold voltages in these 2 cases.
   Plot all 3 transfer characteristics ($V_{BS} = 0V,\ 0.5V, -0.5V$) together.
   Explain the effect of body bias on the operation of the NMOS.
   5 *marks*

   d You need to report the 2 plots, V_T (3 values), g_m and r_o for the NMOS. 5 *marks*

3. In the second part, you will characterize a CMOS Inverter.

   i Connect a CMOS inverter circuit using CD4007 IC (NMOS N1, PMOS P1). Refer to the circuit diagram if necessary. 10 *marks*

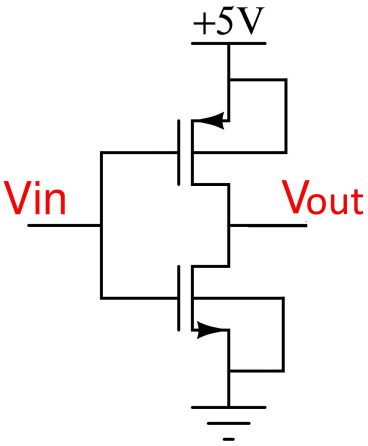
      a Plot voltage transfer characteristics (VTC) of the inverter by applying relevant input voltages and measuring output voltages.

      b Now apply a square pulse of $5V$ ($0V$ off and $5V$ on), 1 Hz to the input of both the inverters and measure the rise and fall times of the output. **What is the ratio of width of the PMOS to NMOS in CD4007?**

   ii Connect a CMOS inverter using PMOS P1 of CD4007 IC and the first NMOS of ALD1106 IC (the same one you used for testing). 10 *marks*

      a Plot voltage transfer characteristics (VTC) of the inverter by applying relevant input voltages and measuring output voltages.

      b Now apply a square pulse of $5V$ ($0V$ off and $5V$ on), 1 Hz to the input of both the inverters and measure the rise and fall times of the output. **What is the ratio of width of PMOS in CD4007 to width of NMOS in ALD1106?**



   iii a Plot both the VTCs on the same plot and report the difference. Explain the reason(s) behind the difference.

      b What are the reasons for similarity or difference in the rise and fall times when compared between the two inverters? 5 *marks*

Assumptions-

- $\mu_n C_{ox}$ and L are the same for all NMOS
- $\mu_p C_{ox}$ and L are the same for all PMOS
- $\mu_n = 2\mu_p$
- Rise time and fall time are directly proportional to the charging and discharging currents respectively.