Experiment 2: Combinational Circuit 2

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## Overview of the experiment:

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| The purpose of this experiment was to design a Vowel Detector using K-Map minimization, coming up with a design using the minimum number of 2-input gates (Bonus), and then implementing the design using VHDL.  Quartus Prime was used to implement the given specifications and my own designs with VHDL. RTL and Gate Level simulations were then carried out using the created Testbench to check for the correctness of the design and its implementation.  The report consists of the following sections:   * **Approach:** An overview of how I approached the experiment and the logic behind my designs. * **Design document and VHDL code:** A brief description of all the design components. * **RTL View:** A screenshot of the RTL View generated using Quartus Prime. * **RTL Simulation:** Screenshots for the RTL and Gate Level Simulations. |

## Approach to the experiment:

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| Given below is the truth table for the vowel detector:   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **x(3)** | **x(2)** | **x(1)** | **x(0)** | **Y** | | 0 | 0 | 0 | 0 | 1 | | 0 | 0 | 0 | 1 | 0 | | 0 | 0 | 1 | 0 | 0 | | 0 | 0 | 1 | 1 | 0 | | 0 | 1 | 0 | 0 | 1 | | 0 | 1 | 0 | 1 | 0 | | 0 | 1 | 1 | 0 | 0 | | 0 | 1 | 1 | 1 | 0 | | 1 | 0 | 0 | 0 | 1 | | 1 | 0 | 0 | 1 | 0 | | 1 | 0 | 1 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | | 1 | 1 | 0 | 0 | 0 | | 1 | 1 | 0 | 1 | 0 | | 1 | 1 | 1 | 0 | 1 | | 1 | 1 | 1 | 1 | 0 | |
| Below is the K-Map for the truth table above and the boolean logic for the output Y:    This logic can be implemented using the following circuit diagram:    The minimum number of 2-input gates with which the circuit can be made is 3 |

## Design document and VHDL code if relevant:

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| Given below is the code for the architecture of the entity **vowel\_det** which is the Vowel Detector circuit we had to implement in Quartus using our own design: |

## RTL View:

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## DUT Input/Output Format:

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  | | --- | --- | | Input  <x3 x2 x1 x0> | Output  <Y> | | 0001 | 0 | | 0100 | 1 | | 1011 | 0 | | 1110 | 1 | |

## RTL Simulation:

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## Gate-level Simulation:

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## Krypton board:

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| Map the logic circuit to the Krypton board and attach the images of the pin assignment and output observed on the board (switches/LEDs). |

## Observations:

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| You must summarize your observations, either in words, using figures and/or tables. |

## References:

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| None |