Experiment 5: Sequential Circuit 1

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## Overview of the experiment:

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| The purpose of this experiment was to design a Sequence Generator with both structural and behavioral modelling using the given logic, coming up with a design to implement the logic, and then implementing the design using VHDL.  Quartus Prime was used to implement the given specifications and my own designs with VHDL. RTL and Gate Level simulations were then carried out using the created Testbench to check for the correctness of the design and its implementation. Scanchain was also used to test the correctness of the design on Krypton hardware.  The report consists of the following sections:   * **Approach:** An overview of how I approached the experiment and the logic behind my designs. * **Design document and VHDL code:** A brief description of all the design components. * **RTL View:** A screenshot of the RTL View generated using Quartus Prime. * **RTL Simulation:** Screenshots for the RTL and Gate Level Simulations. * **Scanchain:** Testing the correctness of my design using Scanchain. |

## Approach to the experiment:

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| We are required to design a Sequence Generator circuit which implements the following design using Structural and Behavioral VHDL description:    We will now draw the State Table for the given sequence:    Using the State Table, we can now write the K-Map minimizations for D2, D1, D0:          This logic can be implemented using the following circuit diagram: |

## Design document and VHDL code if relevant:

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| Given below is the code for the architecture of the entity **sequence\_generator\_structural** which is the Sequence Generator circuit we had to implement in Quartus using structural design:    Given below is the code for the architecture of the entity **sequence\_behavior** which is the Sequence Generator circuit we had to implement in Quartus using behavioral design: |

## RTL View:

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| Structural Design:    Behavioral Design: |

## DUT Input/Output Format:

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  | | --- | --- | | Input  <reset clock> | Output  <y2 y1 y0> | | 11 | 010 | | 00 | 110 | | 01 | 101 | | 00 | 100 | |

## RTL Simulation:

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| Structural Design:    Behavioral Design: |

## Gate-level Simulation:

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| Structural Design:    Behavioral Design: |

## Krypton board:

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| Map the logic circuit to the Krypton board and attach the images of the pin assignment and output observed on the board (switches/LEDs). |

## Observations:

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| After running Scanchain on my Structural Design, I found the following result:    I got “Success” for all the testcases which means that my Structural Design is correct.  Similarly, after running Scanchain on my Behavioral Design, I found the following result:    I got “Success” for all the testcases which means that my Behavioral Design is correct. |

## References:

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| None |