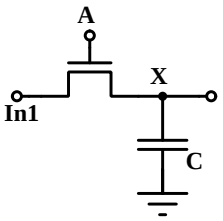
INDIAN INSTITUTE OF TECHNOLOGY BOMBAY
ELECTRICAL ENGINEERING DEPARTMENT

Solution to Mid-Semester Examination
Autumn Semester, 2022

Quantitative answers should be accurate to 0.1%

Q–1 Consider an nMOS transistor charging a capacitor C.



At $t = 0$, Voltage at X is 0 and a logic high voltage $V_H > V_{Tn}$ is applied to terminals A and In1. This results in the capacitor charging through the nMOS transistor.

Use the simple MOS transistor model with ideal saturation.

a) Derive an expression for the voltage at node X as a function of time in terms of transistor parameters and applied voltages.

Soln. 1-a) Let the voltage at X be $V_x(t)$. Since the voltage at In1 is higher that that at X, In1 acts as the drain. Since the drain source voltage and the gate source voltage are the same, $V_{DS} > V_{GS} - V_{Tn}$ and the transistor remains in saturation through the charging process. The current through the transistor is the charging current for the capacitor. Therefore,

$$I_d = \frac{K_n}{2}\left(V_H - V_x - V_{Tn}\right)^2 = C\frac{\mathrm{d}V_x}{\mathrm{d}t}$$

$$\frac{K_n}{2}\frac{\mathrm{d}t}{C} = \frac{\mathrm{d}V_x}{\left(V_H - V_x - V_{Tn}\right)^2}$$

Let $y \equiv V_H - V_x - V_{Tn}$. Then $\mathrm{d}V_x = -\mathrm{d}y$. Integrating both sides from 0 to t,

$$\frac{K_n t}{2C} = -\int_{V_H - V_{Tn}}^{V_H - V_{Tn} - V_x} \frac{\mathrm{d}y}{y^2} = \left[\frac{1}{y}\right]_{V_H - V_{Tn}}^{V_H - V_{Tn} - V_x} = \frac{1}{V_H - V_{Tn} - V_x} - \frac{1}{V_H - V_{Tn}}$$

$$\frac{K_n t}{2C} = \frac{V_x}{\left(V_H - V_{Tn} - V_x\right)\left(V_H - V_{Tn}\right)}$$

So the time take to charge up to a voltage V_x is given by

$$t = \frac{\frac{2C}{K_n}V_x}{\left(V_H - V_{Tn} - V_x\right)\left(V_H - V_{Tn}\right)}$$

$$\text{This gives} \quad \frac{2CV_x}{K_n t} = \left(V_H - V_{Tn} - V_x\right)\left(V_H - V_{Tn}\right)$$

Collecting terms in V_x

$$V_x\left(\frac{2C}{K_n t} + V_H - V_{Tn}\right) = \left(V_H - V_{Tn}\right)^2$$

This gives

$$V_x = \frac{\left(V_H - V_{Tn}\right)^2}{\frac{2C}{K_n t} + V_H - V_{Tn}}$$

This reduces to $V_H - V_{Tn}$ as $t \to \infty$, as expected. – **[3]**

b) You are given that $V_H = 1.7\text{V}$, $V_{Tn} = 0.4\text{V}$ and the voltage at X reaches 0.5V at $t = 100\text{ps}$.

i) What will be the voltage at X at $t = 200\text{ps}$?

Soln. 1-b i) $V_H = 1.7\text{V}$, $V_{Tn} = 0.4\text{V}$, so $V_H - V_{Tn} = 1.3\text{V}$.

$$\text{Since} \quad t = \frac{\frac{2C}{K_n} V_x}{(V_H - V_{Tn} - V_x)(V_H - V_{Tn})}, \qquad \frac{2C}{K_n} = t \frac{(V_H - V_{Tn} - V_x)(V_H - V_{Tn})}{V_x}$$

$$\text{From where,} \quad \frac{2C}{K_n} = \frac{(1.3 - 0.5) \times 1.3}{0.5} \times 100 \times 10^{-12}$$

So $2C/K_n = 2.08 \times 10^{-10}$.

At t = 200 ps,

$$V_x = \frac{1.3^2}{(2.08 \times 10^{-10}/2 \times 10^{-10}) + 1.3} = \frac{1.69}{2.34} = 0.722\text{V}$$

Voltage at 200 ps = 0.722 V – **[1]**

ii) At what time will the voltage at node X reach 1.2V?

Soln. 1-b ii)

$$t = \frac{(2C/K_n)V_x}{(V_H - V_{Tn} - V_x)(V_H - V_{Tn})}, \qquad = \frac{2.08 \times 10^{-10} \times 1.2}{(1.3 - 1.2)(1.3)} = 1.92\text{ns}$$

The capacitor will charge to 1.2 V after 1.92 ns – **[1]**

Notice how slow the charging becomes as we approach 1.3V.

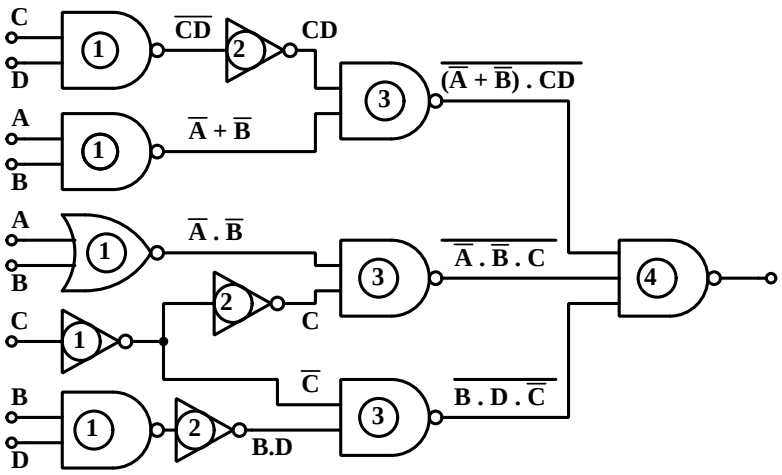
– **[Q1: 3+1+1 = 5 marks]**

Q–2 A circuit receives a 4 bit binary number representing integers in the range $0 \le n \le 15$ at its input. Its output is required to be '1' if the input represents a prime number (2, 3, 5, 7, 11 or 13) and '0' otherwise.

Hint: If the number is ABCD, one can show using a Karnaugh map, that the logic function is: $(\overline{A} + \overline{B}) \cdot CD + \overline{A} \cdot \overline{B} \cdot C + B \cdot \overline{C} \cdot D$.

Implement this function in a 4 phase dynamic logic circuit using only NAND, NOR and inverter gates with no more than 3 inputs for any gate. The four input bits are valid only during phase 1 of a single clock cycle. Complements of these are not provided and should be generated using 4 phase dynamic inverters if required.
Only a logic diagram is to be provided and not a transistor level circuit.
Each logic gate should be labelled with a number written inside its symbol, representing its evaluation phase.
The circuit should produce the output in as few clock phases as possible.

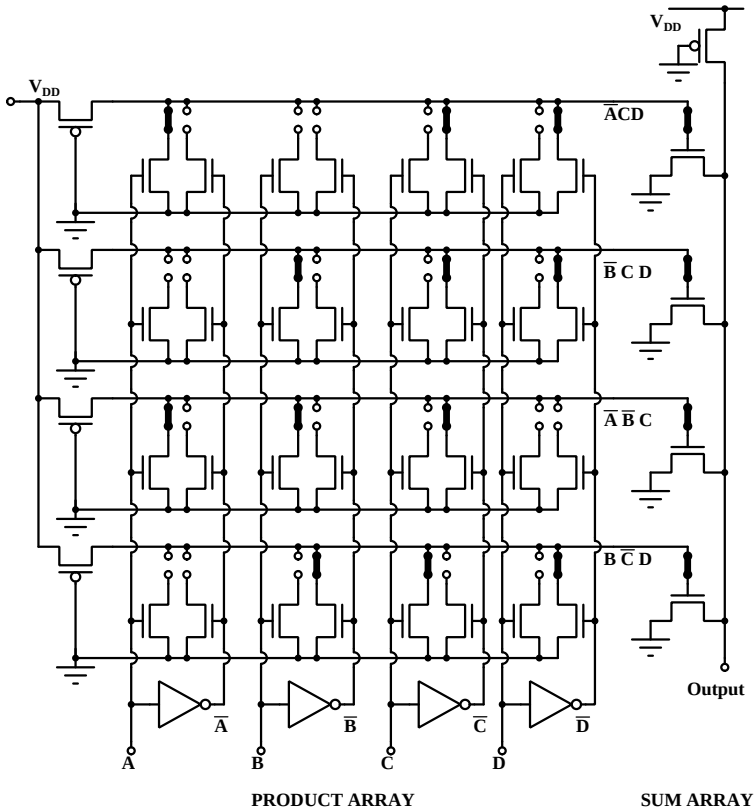
Soln. 2-b) Each 4 phase logic output is valid for 2 phases after the evaluation phase. The following circuit produces the output in phase 1 of next clock (4 clock phases after receiving the input). This solution is not unique and it is possible to have other implementations for the function.



– **[Q2: 4 marks]**

The following question was removed from the actual question paper to reduce the time required for solving. The solution is included here just for reference.

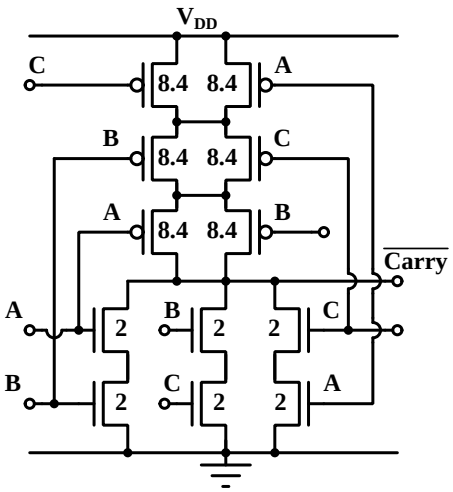
Q: Show how the function (which indicates that the input is a prime number) can be implemented using a programmable logic array with a product array and sum array of the size required for generating the function.
A: We need the product array to generate four product terms from 4 primary inputs. so the product array will have 4 rows and 8 columns (4 for primary inputs and 4 for their complements). The sum array will have 4 rows and just one column to add all the products.



Q–3 In a CMOS process, the value of the mobility correction factor γ is 2.8, while the parasitic delay of the inverter is $p_{inv} = 2.4$.

a) The carry output of a full adder may be expressed as $AB + BC + CA$ where A and B are the bits being added and C is the input carry. Draw a transistor level circuit diagram for a CMOS implementation which generates $\overline{carry}$ using this function.
Using series parallel rules, specify the width of all transistors in the implementation relative to the width of the n channel transistor in a CMOS template inverter.
Find the logical effort for each input A, B and C.
Estimate the parasitic delay of this logic gate relative to the parasitic delay of the template inverter.

Soln. 3-a) The CMOS circuit which generates $\overline{\text{carry}}$ from the symmetric expression is given below:



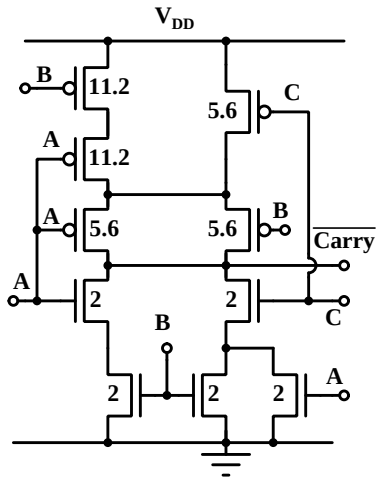
Since there are 2 nMOS transistors in series in each of the three parallel paths to ground, all nMOS transistors should have a width of 2.
There are 3 pMOS transistors in series and by series parallel rules, each should have a width of $3\gamma = 8.4$.
Each input drives 2 nMOS transistors and 2 pMOS transistors. Therefore, the capacitive load is equivalent to $4 + 16.8 = 20.8$ unit transistors. The capacitive load on the input of a template inverter will be $1 + 2.8 = 3.8$ unit transistors. Therefore the logical effort of this stage for all inputs is $20.8/3.8 = 5.474$.
3 nMOS transistors of width 2 each and 2 pMOS transistors with a width of 8.4 each are connected to the output terminal. Therefore the parasitic capacitance corresponds to $6 + 16.8 = 22.8$ unit transistors. In case of an inverter, the parasitic capacitance corresponds to $1 + 2.8 = 3.8$ unit transistors. Therefore the parasitic delay of this gate is $22.8/3.8 = 6$ times that of an inverter. Since $p_{inv} = 2.4$, the parasitic delay of this gate is $6 \times 2.4 = 14.4$ in units of τ. – **[3]**

b) The carry function can also be expressed as $AB + C \cdot (A + B)$. Draw the transistor level implementation for generating $\overline{\text{carry}}$ using this form of the function. Find the relative width of all transistors using series parallel rules and compute the logical effort for each input A, B and C in this implementation. Also find the parasitic delay of the logic gate relative to the parasitic delay of the template inverter.

Soln. 3-b) Using the asymmetric form of the carry function, it is possible to implement it such that the circuit is much faster with respect to the C input. (This is a requirement of adder circuits where carry propagation is on the critical path).

We have two choices for choosing transistor geometries. The nMOS transistors have the same configuration in both cases, but the pMOS transistors have different geometries.

1. The circuit for the first choice shown below.



All paths to ground through nMOS transistors involve two nMOS transistors in series. so the geometry of nMOS transistors should be 2 each. In the path which implements $C.(A+B)$ we keep the single C transistor on top (rather than connecting A and B transistors to the output) to keep the parasitic delay low.

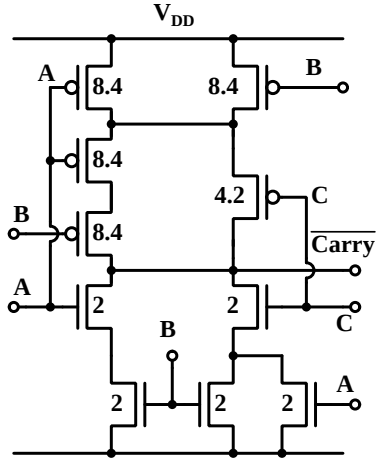
For the pMOS transistors, the sub-circuits implementing $A.B$ and $C.(A+B)$ have to be in series. To keep the total resistance to V_{DD} equivalent to the template inverter, we can keep the effective resistance contributed by each sub-circuit to R/2.

This gives the geometries of A and B transistors in the sub-circuit for $A.B$ as $2\gamma = 5.6$. In the other sub-circuit implementing $C.(A + B)$, width of C transistors should be $2\gamma = 5.6$ and for the other path through series connected A and B transistors, the widths should be $4\gamma = 11.2$. To keep the parasitic delay low, the two transistors forming the $A.B$ sub-circuit should be directly connected to the output.

For this alternative, the A and B inputs are loaded with two nMOS transistors of width 2 and pMOS transistors with widths 5.6 and 11.2. Thus the total capacitive load on these inputs is $2 + 2 + 5.6 + 11.2 = 20.8$ units. This gives the logic effort at inputs A and B to be $20.8/3.8 = 5.47$. The C input is loaded with one nMOS transistor of width 2 and a pMOS transistor of width 5.6. This gives the logical effort at C to be $7.6/3.8 = 2$.

The parasitic delay is contributed by 2 nMOS transistors of width 2 each and 2 pMOS transistor with width of 5.6 each. Thus the total parasitic load on the output is $2 + 2 + 5.6 + 5.6 = 15.2$. The inverter sees a parasitic capacitance of $1 + 2.8 = 3.8$. Therefore the parasitic delay of this gate is:
(15.2/3.8) $p_{inv} = 4p_{inv} = 4 \times 2.4\tau = 9.6\tau$.

2. An alternative choice is shown in the circuit below:



Again, all paths to ground through nMOS transistors involve two nMOS transistors in series. so the geometry of nMOS transistors should be 2 each. In the path which implements $C.(A+B)$ we keep the single C transistor on top (rather than connecting A and B transistors to the output) to keep the parasitic delay low.

For the pMOS transistors, consider the charging path (A, A, B) on the left with 3 transistors in series. To divide the resistance equally along these three transistors, their widths should be $3\gamma = 8.4$ units wide.

Now the B transistor in parallel with the top A transistor should also have the same geometry and so its width should be $3\gamma = 8.4$ units. This means that

the top two transistors implementing $A.B$ have a resistance of R/3. Then, the sub-circuit implementing $C.(A+B)$ can have a resistance of 2R/3. So we can keep the width of C transistor as $1.5\gamma = 4.2$ units. (The width of series A and B transistors in the $C.(A+B)$ sub-circuit have already been decided as 8.4 units and correctly provide a total resistance of 2R/3 in parallel with the C transistor). To keep the parasitic delay low, we connect the smaller transistors directly to the output node.

For this choice of transistor widths, the total capacitive load on A and B inputs is $2+2+8.4+8.4 = 20.8$ units, which gives a logical effort of $20.8/3.8 = 5.47$. For the C input, the total capacitive load is $4.2+2 = 6.2$ units. So the logical effort for C input is $6.2/3.8 = 1.63$.

Total transistor width directly connected to the output is $2+2+8.4+4.2 = 16.6$. Therefore the parasitic delay is $16.6/3.8 p_{inv} = 4.37 p_{inv}$. Thus the parasitic delay is $4.37 \times 2.4\tau = 10.48\tau$.

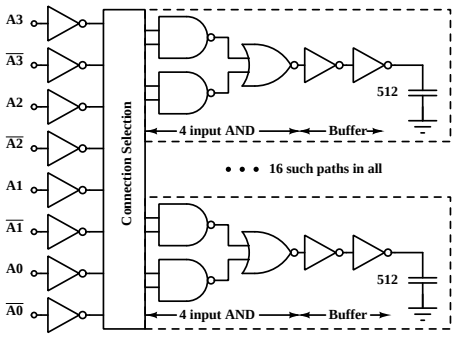
Thus we see that the second choice gives a lower logical effort for C, (1.62 versus 2) but a marginally higher value of parasitic delay. for moderate to high loads, the second choice will be preferable, while for low loads, the first choice may be faster. (Either configuration in the answer will get full credit). – **[3]**

– **[Q3: 3+3 = 6 marks]**

Q–4 A circuit needs to generate 16 select outputs to enable the outputs of one out of 16 registers in a microprocessor. Its input is the 4 bit register address along with their complements. Each of these 8 inputs can drive up to 4 template inverters.

The 8 inputs are first buffered by an inverter each. Appropriate combinations of each bit or its complement are fed to 4-input ANDs to generate the select outputs.

For each select path, the 4 input AND function is implemented using two 2-input NAND gates whose outputs are combined by a 2 input NOR gate to generate the AND function of 4 inputs. There are 16 such select paths and the 4 inputs for each path are formed by appropriate combinations of the 4 input bits or their complements. For example, Select line for register 11 (binary address 1011) will be the AND of $A3, \overline{A2}, A1$ and $A0$.



The full logic path is as shown here on the left.
The 4 input AND is implemented through two 2-input NANDs followed by a 2-input NOR. This is followed by 2 inverters to drive the heavy load at the end of the select line.

Each of the input signals can drive up to 4 template inverters.
The value of γ is 2.8, while the parasitic delay of an inverter is 2.4 in units of τ.

a) what is the branch factor b at the output of the first inverter used at the input?

Soln. 4-a) There are a total of 8 inverter outputs which feed 4 inputs each of the 16 select generator paths – for a total of 64 NAND inputs. Therefore each inverter output will go to $64/8 = 8$ NAND gate inputs. Thus $b = 8$. – **[1]**

b) Compute the optimum stage effort $\hat{f}$ for this circuit if the final output has to drive a load equivalent to 512 template inverters.

Soln. 4-b) Logical effort for all inverters is 1.
The template NAND gate has 2 nMOS transistors in series, each of which should have a width of 2. The pMOS transistors are in parallel, so the pMOS size would

be the same as the pMOS in template inverter, $= \gamma = 2.8$.
Therefore the input capacitance of the template NAND gate is $2 + 2.8 = 4.8$. Since the input capacitance of the template inverter is $1 + 2.8 = 3.8$, the logical effort for the 2 input NAND gate is $4.8/3.8 = 1.2632$.

The template NOR gate has 2 nMOS transistors in parallel, so their widths are 1 each. The p channel transistors are in series, so their widths must be $2\gamma = 5.6$. Hence the logical effort for 2 input NOR gate is: $(1 + 5.6)/(1 + 2.8) = 1.7368$. Multiplying the g values for all stages, we get:

$$G = 1 \times \frac{4.8}{3.8} \times \frac{6.6}{3.8} \times 1 \times 1 = 2.1939$$

The branch factor is 8 for the first inverter and 1 for all the rest. Therefore $B = 8$.

The path electrical effort $H = C_{out}/C_{in} = 512/4 = 128$.

Therefore $F = GBH = 2.1939 \times 8 \times 128 = 2246.56$
Since there are five stages, $\hat{f} = 2246.56^{1/5} = 4.681$. – **[2]**

c) Compute the input capacitance in units of the input capacitance of the template inverter for each stage.

Soln. 4-c) We have $\hat{f} = 4.681$ for all stages. Let us begin with the first inverter stage:

Input Inverter:
$g = 1, b = 8, C_{in} = 4, \hat{f} = bgh = 4.681$
So, $h = \hat{f}/bg = 4.681/8 = 0.585$ $(= C_{out}/C_{in})$.
$C_{in} = 4$, so $C_{out} = hC_{in} = 0.585 \times 4 = 2.340$.

Two input NAND:
$g = 1.2632, b = 1, C_{in} = 2.340, \hat{f} = bgh = 4.681$
So, $h = \hat{f}/bg = 4.681/1.2632 = 3.7055$ $(= C_{out}/C_{in})$.
$C_{in} = 2.340$, so $C_{out} = hC_{in} = 3.7055 \times 2.340 = 8.672$.

Two input NOR:
$g = 1.7368, b = 1, C_{in} = 8.672, \hat{f} = bgh = 4.681$
So, $h = \hat{f}/bg = 4.681/1.7368 = 2.6949$ $(= C_{out}/C_{in})$.
$C_{in} = 8.672$, so $C_{out} = hC_{in} = 2.6940 \times 8.672 = 23.370$.

First buffer inverter:
$g = 1, b = 1, C_{in} = 23.307, \hat{f} = bgh = 4.681$
So, $h = \hat{f}/bg = 4.681/1 = 4.681$ $(= C_{out}/C_{in})$.
$C_{in} = 23.307$, so $C_{out} = hC_{in} = 4.681 \times 23.370 = 109.387$.

Second buffer inverter:
$g = 1, b = 1, C_{in} = 109.387, \hat{f} = bgh = 4.681$
So, $h = \hat{f}/bg = 4.681/1 = 4.681$ $(= C_{out}/C_{in})$.
$C_{in} = 109.387$, so $C_{out} = hC_{in} = 4.681 \times 109.387 = 512$.
This agrees with our final load specification.

– **[3]**

d) Compute the n and p channel transistor geometry size for each stage.

Soln. 4-d) The input capacitance for a template gate with scale factor of 1 is g.
If the actual input capacitance $= C_{in}$, the scale factor is C_{in}/g
Knowing C_{in} for each stage, we can divide by its logical effort g to get the scale factor and then scale all transistor sizes of the template gate by this value.

Input Inverter:
$g = 1, C_{in} = 4$, so scale factor $= 4$.

nMOS size $= 4 \times 1 = 4$, pMOS size $= 4 \times \gamma = 4 \times 2.8 = 11.2$.

Two input NAND:
$g = 1.2632, C_{in} = 2.340$, scale factor $= 2.340/1.2632 = 1.8527$
So nMOS size $= 2 \times 1.8527 = 3.705$
and pMOS size $= 1.8527 \times \gamma = 1.8527 \times 2.8 = 5.188$.

Two input NOR:
$g = 1.7368, C_{in} = 8.672$, scale factor $= 8.672/1.7368 = 4.993$
So nMOS size $= 1 \times 4.993 = 4.993$
and pMOS size $= 4.993 \times 2\gamma = 4.993 \times 5.6 = 27.96$.

First buffer inverter:
$g = 1, C_{in} = 23.37$, scale factor $= 23.37/1 = 23.37$ So nMOS size $= 1 \times 23.37 = 23.37$
and pMOS size $= 23.37 \times \gamma = 23.37 \times 2.8 = 65.44$.

Second buffer inverter:
$g = 1, C_{in} = 109.387$, scale factor $= 109.387/1 = 109.387$ So nMOS size $= 1 \times 109.387 = 109.39$
and pMOS size $= 109.387 \times \gamma = 109.387 \times 2.8 = 306.3$.

Logic Stage	g	C_{in}	Scale Factor	n width	p width
Input Inv.	1	4	4	4	11.2
2input NAND	1.2632	2.340	1.8527	3.705	5.188
2input NOR	1.7368	8.672	4.993	4.993	27.96
Buf Inv. 1	1	23.37	23.37	23.37	65.44
Buf Inv. 2	1	109.39	109.39	109.39	306.3

– **[3]**

e) Find the total delay of the logic path in units of τ.

Soln. 4-e) Delay for every stage is $\hat{f} + p$.
Parasitic delay for 2 input NAND and 2 input NOR is $2p_{inv}$ each.
So the total delay is:
$5\hat{f} + p_{inv} + 2p_{inv} + 2p_{inv} + p_{inv} + p_{inv} = 5 \times 4.68022 + 7 \times 2.4 = 40.203\tau$ – **[1]**

– **[Q4: 1+2+3+3+1 = 10 marks]**
