EE671: Assignment 1

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1 Q-1

From the analysis done in class we know the relationship between Rise Time:

$$\tau_{Rise} \propto L_p/W_p \tag{1}$$

where L_p is the length of the pMOS transistor and W_p is the width.
Similarly for Fall Time,

$$\tau_{Fall} \propto L_n/W_n \tag{2}$$

Given below are the simulation results for Rise and Fall Times for the DUT and Input for $W_n = 0.24\mu m$, $W_p = 0.24\mu m$, $L_n = 0.18\mu m$, $L_p = 0.18\mu m$:

τ^{in}_{Rise}	$16ps$
τ^{in}_{Fall}	$16ps$
τ^{d}_{Rise}	$1200ps$
τ^{d}_{Fall}	$424ps$

Using Eq. 1, we conclude that

$$\tau^1_{Rise} * W^1_p = \tau^2_{Rise} * W^2_p \tag{3}$$

We require a τ_{Rise} of $216ps$. Using this we get $W^2_p = 0.47\mu m$
Similarly, using Eq. 2, we conclude that

$$\tau^1_{Fall} * W^1_n = \tau^2_{Fall} * W^2_n \tag{4}$$

We require a τ_{Fall} of $216ps$. Using this we get $W^2_n = 1.33\mu m$

1.1 Simulation Results

1.1.1 Code Snippet

```
* Unit Inverter
.subckt inv supply Inp Output
.param Wp = 1.33U
.param Wn = 0.47U
.param L = 0.18U
MP1 Output Inp Supply Supply cmosp
+ L=L W=Wp AD = (2*L*Wp) AS = (2*L*Wp) PD = (2*(2*L+Wp))
+ PS = (2*(2*L+Wp))
MN1 Output Inp 0 0 cmosn
+ L=L W=Wn AD = (2*L*Wn) AS = (2*L*Wn) PD = (2*(2*L+Wn))
+ PS = (2*(2*L+Wn))
.ends
vdd supply 0 dc 1.8
* Device under test
x3 supply Ck dutout inv
* Load Capacitor
C3 dutout 0 0.05pF
.include models-180nm
*TRANSIENT ANALYSIS with pulse inputs
VCk Ck 0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8.0nS)
.tran 1pS 35nS 0nS
.control
run
plot 4.0+V(Ck) V(dutout)
meas tran inrise TRIG v(ck) VAL=0.18 RISE=2 TARG v(Ck)
+ VAL=1.62 RISE=2
meas tran infall TRIG v(ck) VAL=1.62 FALL=2 TARG v(Ck)
+ VAL=0.18 FALL=2
meas tran drise TRIG v(dutout) VAL=0.18 RISE=2 TARG v(dutout)
+ VAL=1.62 RISE=2
meas tran dfall TRIG v(dutout) VAL=1.62 FALL=2 TARG v(dutout)
+ VAL=0.18 FALL=2
.endc
.end
```

1.1.2 Simulation

Given below are the simulation results for Rise and Fall Times for the DUT and Input for $W_n = 1.33\mu m$, $W_p = 0.47\mu m$, $L_n = 0.18\mu m$, $L_p = 0.18\mu m$:

τ^{in}_{Rise}	$16ps$
τ^{in}_{Fall}	$16ps$
τ^{d}_{Rise}	$297ps$
τ^{d}_{Fall}	$278ps$

We observe that the simulation results for τ_{Rise} and τ_{Fall} are significantly different from the required $216ps$
Using hit and trial I was able to achieve the following simulation readings for $W_n = 0.665\mu m$, $W_p = 1.91\mu m$, $L_n = 0.18\mu m$, $L_p = 0.18\mu m$:

τ^{in}_{Rise}	$16ps$
τ^{in}_{Fall}	$16ps$
τ^{d}_{Rise}	$215.8ps$
τ^{d}_{Fall}	$216.0ps$

2 Q-2

2.1 Code Snippet

```
* Unit Inverter
.subckt inv supply Inp Output
.param Wp = 1.91U
.param Wn = 0.665U
.param L = 0.18U
MP1 Output Inp Supply Supply cmosp
+ L=L W=Wp AD = (2*L*Wp) AS = (2*L*Wp) PD = (2*(2*L+Wp))
+ PS = (2*(2*L+Wp))
MN1 Output Inp 0 0 cmosn
+ L=L W=Wn AD = (2*L*Wn) AS = (2*L*Wn) PD = (2*(2*L+Wn))
+ PS = (2*(2*L+Wn))
.ends
vdd supply 0 dc 1.8
* Device under test
x3 supply Ck dutout inv
```

```
* Load Capacitor
C3 dutout 0 0.05pF
.include models-180nm
*DC ANALYSIS with pulse inputs
VCk Ck 0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8.0nS)
.dc VCk 0 1.8 0.01
.control
run
plot v(dutout) vs v(Ck)
let derivout = deriv(v(dutout))
meas dc ViL find v(Ck) when derivout = -1
meas dc VoH find v(dutout) when derivout = -1
meas dc ViH find v(Ck) when derivout = -1 rise = last
meas dc VoL find v(dutout) when derivout = -1 rise = last
.endc
.end
```

2.2 Simulation Results

Given below is the plot for static transfer characteristics obtained from the dc analysis of the circuit with $W_n = 1.33\mu m$, $W_p = 0.47\mu m$:

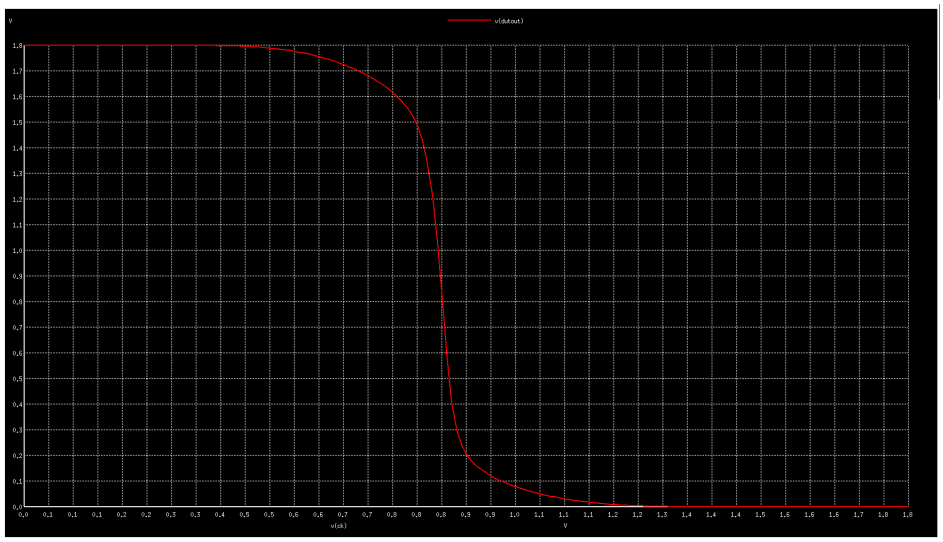


Fig. Static Transfer Characteristics of Inverter

Given below is the plot for static transfer characteristics obtained from the dc analysis of the circuit with $W_n = 0.665\mu m$, $W_p = 1.91\mu m$:

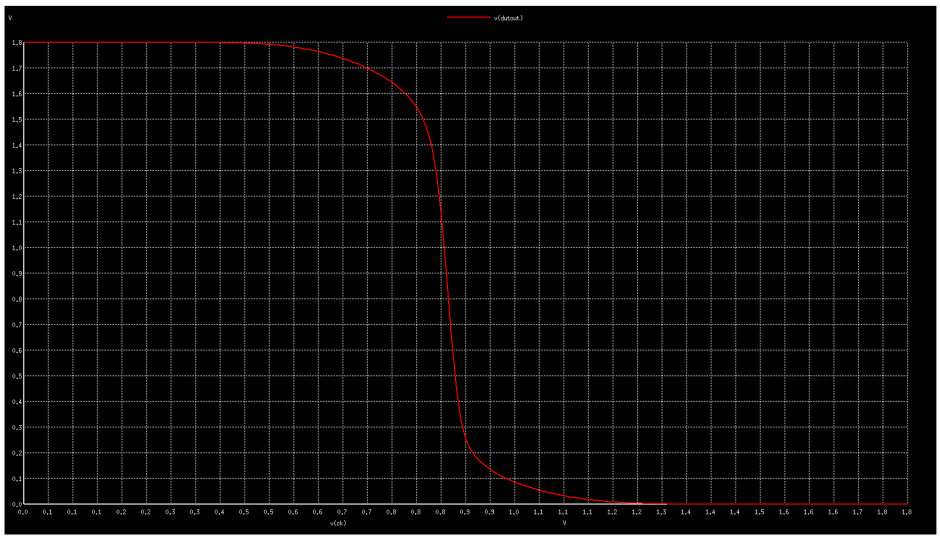


Fig. Static Transfer Characteristics of Inverter

The following calculations have been made for the 2nd Static Transfer Characteristics plot.

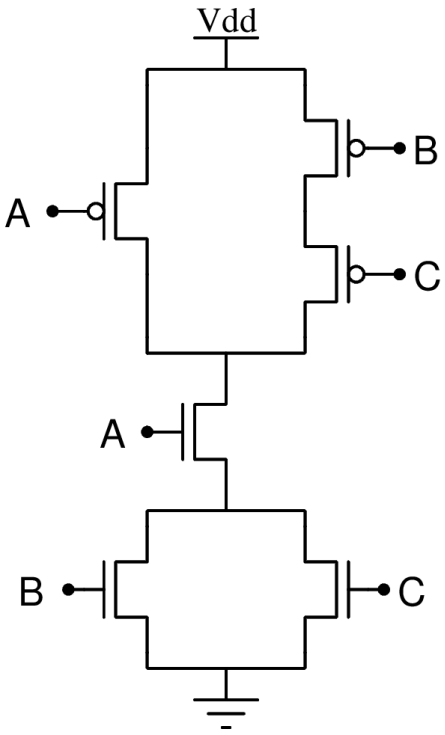
V_{iL}	$0.694V$
V_{oH}	$1.687V$
V_{iH}	$0.957V$
V_{oL}	$0.113V$

Using the above readings, we get the Noise Margins as:

$$\text{High Noise Margin} : V_{oH} - V_{iH} = 0.730V$$
$$\text{Low Noise Margin} : V_{iL} - V_{oL} = 0.581V$$

3 Q-3

3.1 Design



3.2 Code Snippet

```
* Logic Gate
.subckt lg A B C Supply Output
MPA Output A Supply Supply cmosp
+ L=0.18U W=1.91U AD = 0.6876P AS = 0.6876P PD = 4.54U
+ PS = 4.54U
MPB 1 B Supply Supply cmosp
+ L=0.18U W=1.91U AD = 0.6876P AS = 0.6876P PD = 4.54U
+ PS = 4.54U
MPC Output C 1 1 cmosp
+ L=0.18U W=1.91U AD = 0.6876P AS = 0.6876P PD = 4.54U
+ PS = 4.54U
```

```
MNA Output A 2 2 cmosn
+ L=0.18U W=0.665U AD = 0.2394P AS = 0.2394P PD = 2.050U
+ PS = 2.050U
MNB 2 B 0 0 cmosn
+ L=0.18U W=0.665U AD = 0.2394P AS = 0.2394P PD = 2.050U
+ PS = 2.050U
MNC 2 C 0 0 cmosn
+ L=0.18U W=0.665U AD = 0.2394P AS = 0.2394P PD = 2.050U
+ PS = 2.050U
.ends
vdd supply 0 dc 1.8
va A 0 dc 1.8
vb B 0 dc 0
vc C 0 dc 0
* Device under test
x3 A B Ck supply dutout lg
* Load Capacitor
C3 dutout 0 0.05pF
.include models-180nm
*TRANSIENT ANALYSIS with pulse inputs
VCk Ck 0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8.0nS)
.tran 1pS 35nS 0nS
.control
run
plot 4.0+V(Ck) V(dutout)
meas tran inrise TRIG v(ck) VAL=0.18 RISE=2 TARG v(Ck)
+ VAL=1.62 RISE=2
meas tran infall TRIG v(ck) VAL=1.62 FALL=2 TARG v(Ck)
+ VAL=0.18 FALL=2
meas tran drise TRIG v(dutout) VAL=0.18 RISE=2 TARG v(dutout)
+ VAL=1.62 RISE=2
meas tran dfall TRIG v(dutout) VAL=1.62 FALL=2 TARG v(dutout)
+ VAL=0.18 FALL=2
.endc
.end
```

3.3 Simulation Results

Using the series-parallel rule, we find the following values for Rise Time and Fall Time:

Cases	τ_{Rise}	τ_{Fall}
A = Ck; B = 1.8; C = 0	$242ps$	$367ps$
A = 1.8; B = Ck; C = 0	$427ps$	$367ps$
A = 1.8; B = 0; C = Ck	$427ps$	$350ps$

Lets assume, for the inverter, $\tau_{Rise} = \tau_{Fall} = \tau \approx 216ps$
Cases:

- For B = 1.8V and C = 0V, when A = 0V (output will rise), the longest path will contain 1 pMOS transistor and therefore will have a delay of $\tau \approx 216ps$. When A = 1.8V (output will fall), the longest path will contain 2 nMOS transistors and therefore will have a delay of $2\tau \approx 432ps$.

- For A = 1.8V and C = 0V, when B = 0V (output will rise), the longest path will contain 2 pMOS transistors and therefore will have a delay of $2\tau \approx 432ps$. When B = 1.8V (output will fall), the longest path will contain 2 nMOS transistors and therefore will have a delay of $2\tau \approx 432ps$.

- For A = 1.8V and B = 0V, when C = 0V (output will rise), the longest path will contain 2 pMOS transistors and therefore will have a delay of $2\tau \approx 432ps$. When C = 1.8V (output will fall), the longest path will contain 2 nMOS transistors and therefore will have a delay of $2\tau \approx 432ps$.