EE671: Assignment 3

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The delay of a logic stage is defined as the time interval between the midpoint of input and output transients. In this simulation, we'll try to use realistic conditions for input wave shapes and output loading.
We use the following circuit for measuring the delay of the DUT:

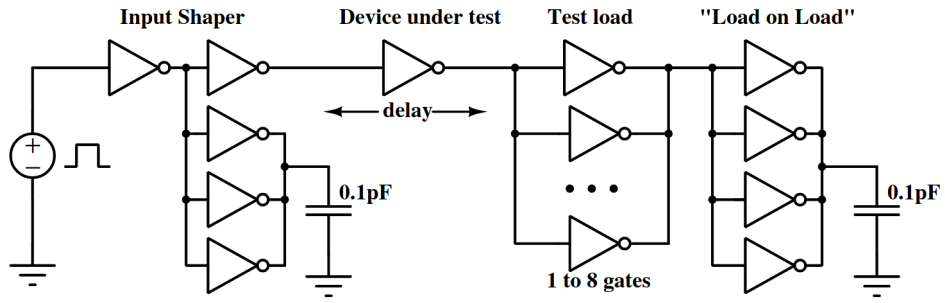


Fig. Circuit for evaluation of τ and p_{inv}

The circuit above is composed of four parts:

- **Input Shaper:** We would like to apply inputs which have the kinds of rise and fall times typically encountered in actual circuits, rather than the steep pulses provided by ideal voltage sources. Therefore we drive the device under test with pulses passed through a two stage inverter buffer. The first stage is a single minimal inverter, driving four minimal inverters which form the second stage. One of the four inverters in the second stage drives the device under test. The other 3 inverters present an additional dummy load to the first stage inverter. These 3 inverters drive a common load of 0.1pF.
- **Device under Test:** This is the minimum inverter whose delay parameters are being evaluated.

- **Test Load:** The DUT will be loaded with 1 to 8 logic gates in parallel, to evaluate the delay as a function of the fan-out. The fanout will be varied from 1 to 8.
- **Load on Load:** The logic gates acting as load should themselves see a realistic capacitive load. Therefore, we use 4 inverters in parallel driving a final output capacitance of 0.1pf as the load on load.

1 Code Snippet

```
Delay of DUT

* Importing required files
.include Inverter.txt
.include models-180nm
* Defining necessary parameters
.param Trep= 5n
.param Trf = {Trep/20.0}
.param Tw = {Trep/2.0 - Trf}
.param hival=1.8
.param loval=0.0
* Generating pulse for Input
Vpulse pgen 0 DC 0 PULSE({loval} {hival} {Tw} {Trf} {Trf} {Tw}
+ {Trep})
* Supply Voltage
vdd supply 0 dc 1.8
* Inverters for loading the input
xin1 supply pgen temp1 inv
xin2 supply temp1 dutin inv
xin3 supply temp1 temp2 inv
xin4 supply temp1 temp2 inv
xin5 supply temp1 temp2 inv
* Cin for loading the input
Cin temp2 0 0.1p
* DUT
xdut supply dutin dutout inv
* Inverters for test load
```

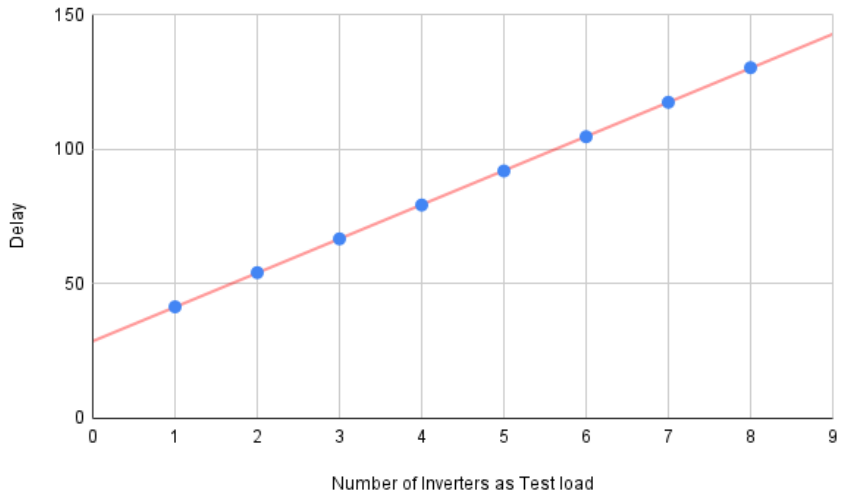
```
xtest1 supply dutout temp3 inv
*xtest2 supply dutout temp3 inv
*xtest3 supply dutout temp3 inv
*xtest4 supply dutout temp3 inv
*xtest5 supply dutout temp3 inv
*xtest6 supply dutout temp3 inv
*xtest7 supply dutout temp3 inv
*xtest8 supply dutout temp3 inv
* Inverters for loading the output
xload1 supply temp3 temp4 inv
xload2 supply temp3 temp4 inv
xload3 supply temp3 temp4 inv
xload4 supply temp3 temp4 inv
* Cout for loading the output
Cout temp4 0 0.1p
* Performing transient analysis
.tran 1pS {3*Trep} 0nS
.control
run
* Plotting voltage waveforms
plot v(pgen)+2 v(dutin) v(dutout)
meas tran invdelay1 TRIG v(dutin) VAL=0.9 RISE=2 TARG v(dutout)
+ VAL=0.9 FALL=2
meas tran invdelay2 TRIG v(dutin) VAL=0.9 FALL=2 TARG v(dutout)
+ VAL=0.9 RISE=2
.endc
.end
```

2 Simulation Results

Given below are the results for the two delays and their average for fanout values varying from 1 to 8:

Fan-out	Delay 1 (in ps)	Delay 2 (in ps)	Average Delay (in ps)
1	41.4245	41.577	41.272
2	54.1325	54.728	53.537
3	66.673	67.495	65.851
4	79.24	80.171	78.309
5	91.882	92.817	90.947
6	104.608	105.473	103.743
7	117.4015	118.148	116.655
8	130.2495	130.841	129.658

Given below is the plot for average delay for different fan-out values varying from 1 to 8:



We know that the delay for the DUT is given by:

$$d = bgh + p_{inv} \tag{1}$$

where b is the branching effort, g is the logical effort and h is the electrical effort.
This delay is in units of τ, which is the delay of a standard inverter driving an identical inverter, excluding the parasitic delays. Therefore the above equation can be more accurately represented as:

$$d = (bgh + p_{inv}) \times \tau \tag{2}$$

On plotting this delay against b, which is the fan-out, we realise that the slope is equal to $gh \times \tau$ and the y-intercept is equal to $p_{inv} \times \tau$. But the logical effort, g for an inverter is equal to 1 and the electrical effort, h is equal to C_{out}/Cin. For our implementation, both C_{out} and C_{in} are equal to $0.1pF$, resulting in $h = 1$. Using this the slope now gives us τ.

γ is just the ratio of the widths of the pMOS and nMOS transistors, which are $1.91\mu m$ and $0.665\mu m$ respectively.

Given below are the observed values for the slope, y-intercept and the calculated values for τ, p_{inv} and γ:

Slope	12.6893ps
Y-Intercept	28.7352ps
τ	12.6893ps
p_{inv}	2.2645
γ	2.8722