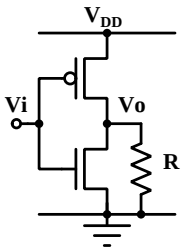
INDIAN INSTITUTE OF TECHNOLOGY BOMBAY
ELECTRICAL ENGINEERING DEPARTMENT

Class Test - 1

Thursday	**EE 671: VLSI Design**	Time: 1140-1255
Aug. 18, 2022	Autumn Semester 2022	Marks: 10

This question paper has 3 questions over 2 pages.
Quantitative answers should be accurate to 0.1%.

Q–1



Consider a CMOS inverter loaded by a resistor R as shown on the left. Use the simple transistor model for both transistors:

$$\begin{aligned} I_{DS} &= 0 && \text{when } V_{GS} \le V_T \\ I_{DS} &= K\left[(V_{GS}-V_T)V_{DS} - \tfrac{1}{2}V_{DS}^2\right] && \text{when } V_{GS} > V_T,\ V_{DS} \le V_{GS}-V_T \\ I_{DS} &= \tfrac{K}{2}\left(V_{GS}-V_T\right)^2 && \text{when } V_{GS} > V_T,\ V_{DS} \ge V_{GS}-V_T \end{aligned}$$

a) Derive an expression for the output voltage V_o as a function of the supply voltage V_{DD}, input voltage V_i, n and p channel turn on voltages V_{Tn} and V_{Tp}, and conductance factors K_n and K_p. ($K_n \equiv \mu_n C_{ox}\ W_n/L_n, K_p \equiv \mu_p C_{ox}\ W_p/L_p$). Assume that the input voltage is such that the n channel transistor is in linear mode while the p channel transistor is saturated.

Soln. 1-a) The current through the pMOS transistor must equal the current through the nMOS transistor plus the current through the resistor. Therefore,

$$\frac{K_p}{2}\left(V_{DD}-V_i-V_{Tp}\right)^2 = K_n\left[\left(V_i-V_{Tn}\right)V_o - \frac{1}{2}V_o^2\right] + \frac{V_o}{R}$$

The term on the left is independent of V_o. Let us represent it as I_{Dp}. Let us represent $V_i - V_{Tn}$ by V_i'. Dividing both sides by K_n, we get

$$\frac{I_{Dp}}{K_n} = V_i' V_o - \frac{1}{2}V_o^2 + \frac{V_o}{RK_n}$$

This leads to the quadratic equation

$$\frac{1}{2}V_o^2 - \left(V_i' + \frac{1}{RK_n}\right)V_0 + \frac{I_{Dp}}{K_n} = 0$$

with solutions

$$V_o = V_i' + \frac{1}{RK_n} \pm \sqrt{\left(V_i' + \frac{1}{RK_n}\right)^2 - \frac{2I_{Dp}}{K_n}}$$

Since the nMOS transistor is in linear regime, the output voltage must be $< V_i'$. Therefore we must choose the negative sign. This gives

$$V_o = V_i' + \frac{1}{RK_n} - \sqrt{\left(V_i' + \frac{1}{RK_n}\right)^2 - \frac{2I_{Dp}}{K_n}}$$

substituting for V_i' and I_{Dp} we get

$$V_o = V_i - V_{Tn} + \frac{1}{RK_n} - \sqrt{\left(V_i - V_{Tn} + \frac{1}{RK_n}\right)^2 - \frac{K_p}{K_n}\ \left(V_{DD}-V_i-V_{Tp}\right)^2}$$

This is the desired expression for V_o. – **[3]**

b) If $V_{DD} = 1.8$V, $V_{Tn} = 0.4$V, $V_{Tp} = 0.45$V, $K_n = K_p = 650\mu$A/V^2 and $R = 100$KΩ, find the minimum input voltage V_i which will ensure that the nMOS transistor is in linear mode of operation.

Soln. 1-b) As the input voltage increase, the output voltage falls. We determine the input voltage at which the output voltage is $V_i - V_{Tn}$ and the transistor is on the edge of saturation. For any higher input voltage, the output voltage (and hence the drain voltage of nMOS) will be lower than $V_i - V_{Tn}$, so it will be in linear regime. Putting $V_o = V_i - V_{Tn}$ in the expression for V_o, we get

$$V_i - V_{Tn} = V_i - V_{Tn} + \frac{1}{RK_n} - \sqrt{\left(V_i - V_{Tn} + \frac{1}{RK_n}\right)^2 - \frac{K_p}{K_n}\ (V_{DD} - V_i - V_{Tp})^2}$$

or

$$0 = \frac{1}{RK_n} - \sqrt{\left(V_i - V_{Tn} + \frac{1}{RK_n}\right)^2 - \frac{K_p}{K_n}\ (V_{DD} - V_i - V_{Tp})^2}$$

which leads to

$$\frac{1}{(RK_n)^2} = \left(V_i - V_{Tn} + \frac{1}{RK_n}\right)^2 - \frac{K_p}{K_n}\ (V_{DD} - V_i - V_{Tp})^2$$

This gives a quadratic equation in V_i, which can be solved to get the input voltage above which the nMOS will be in linear regime.
In the current case, we have $V_{DD} = 1.8$V, $V_{Tn} = 0.4$V, $V_{Tp} = 0.45$V, $K_n = K_p = 650\mu$A/V^2 and $R = 100$KΩ.
$RK_n = 650 \times 10^{-6} \times 10^5 = 65$. Substituting these values, we get

$$\frac{1}{65^2} = \left(V_i - 0.4 + \frac{1}{65}\right)^2 - (1.8 - V_i - 0.45)^2$$

$$\text{So} \quad 2.366864 \times 10^{-4} = (V_i - 0.3846154)^2 - (1.35 - V_i)^2$$

$$\text{Therefore} \quad 2.366864 \times 10^{-4} = V_i^2 + 0.147929 - 0.7692308V_i - V_i^2 - 1.82225 + 2.7V_i$$

Thus the square term in V_i cancels and we are left with a linear equation.

$$1.674808 = 1.930769V_i \quad \text{so} \quad V_i = 0.8674303$$

Thus the nMOS transistor will be in the linear regime for $V_i > 0.8674303$.

To verify this answer, let us compute V_o for this value of V_i. We get:

$$\begin{aligned} V_o &= V_i - V_{Tn} + \frac{1}{RK_n} - \sqrt{\left(V_i - V_{Tn} + \frac{1}{RK_n}\right)^2 - \frac{K_p}{K_n}\ (V_{DD} - V_i - V_{Tp})^2} \\ &= 0.4848149 - \sqrt{0.2331102 - 0.2328735} = 0.4674303. \end{aligned}$$

This is indeed $= V_i - V_{Tn} = V_i - 0.4$.

Further, the pMOS current is

$$I_{Dp} = \frac{650 \times 10^{-6}}{2}(1.8 - 0.45 - 0.8674303)^2 = 75.6839\mu\text{A}$$

Since the nMOS is on the verge of saturation, we can compute I_{Dn} as

$$I_{Dn} = \frac{650 \times 10^{-6}}{2}(0.8674303 - 0.4)^2 = 71.0096\mu\text{A}$$

Current through the resistor is

$$\frac{V_o}{R} = \frac{0.4674303}{10^5} = 4.674303\mu\text{A}$$

Thus we verify that

$$I_{Dp} = I_{Dn} + \frac{V_o}{R}$$

– **[3]**

Q–2 The rise and fall times for a CMOS inverter driving a load capacitor are given by

$$\begin{aligned}\tau_{rise} &= \frac{C(V_i + V_{Tp})}{\frac{K_p}{2}(V_{DD} - V_i - V_{Tp})^2} + \frac{C}{K_p(V_{DD} - V_i - V_{Tp})} \ln \frac{V_{DD} + V_{oH} - 2V_i - 2V_{Tp}}{V_{DD} - V_{oH}} \\ \tau_{fall} &= \frac{C(V_{DD} - V_i + V_{Tn})}{\frac{K_n}{2}(V_i - V_{Tn})^2} + \frac{C}{K_n(V_i - V_{Tn})} \ln \frac{2(V_i - V_{Tn}) - V_{oL}}{V_{oL}}\end{aligned}$$

You are given that $V_{DD} = 1.8\text{V}$, $V_{Tn} = 0.4\text{V}$, $V_{Tp} = 0.45\text{V}$, $\mu_n = 270\text{cm}^2/\text{Vs}$, and $\mu_p = 130\text{cm}^2/\text{Vs}$. The n and p channel transistors have the same channel length and gate oxide capacitance per unit area.
What should be the ratio of widths of n and p channel transistors such that the time taken to charge the output from 0V to $V_{DD} - V_{Tp}$ with the input voltage $= V_{Tn}$ is the same as the time taken to discharge the output from V_{DD} to V_{Tn} with the input voltage $= V_{DD} - V_{Tp}$.

Soln. 2)

$$\frac{K_p\tau_{rise}}{C} = \frac{2(V_i + V_{Tp})}{(V_{DD} - V_i - V_{Tp})^2} + \frac{1}{(V_{DD} - V_i - V_{Tp})} \ln \frac{V_{DD} + V_{oH} - 2V_i - 2V_{Tp}}{V_{DD} - V_{oH}}$$

For τ_{rise} case, we have
$V_i = V_{Tn} = 0.4\text{V}$, $V_{oH} = V_{DD} - V_{Tp} = 1.8 - 0.45 = 1.35\text{V}$,
$V_{DD} - V_i - V_{Tp} = 1.8 - 0.4 - 0.45 = 0.95\text{V}$.
Substituting these values, we get

$$\frac{K_p\tau_{rise}}{C} = \frac{2(0.4 + 0.45)}{0.95^2} + \frac{1}{0.95} \ln \frac{1.8 + 1.35 - 0.8 - 0.9}{1.8 - 1.35}$$

$$\text{So} \quad \frac{K_p\tau_{rise}}{C} = 1.8837 + 1.0526 \times \ln 3.2222 = 3.1153$$

$$\frac{K_n\tau_{fall}}{C} = \frac{2(V_{DD} - V_i + V_{Tn})}{(V_i - V_{Tn})^2} + \frac{1}{(V_i - V_{Tn})} \ln \frac{2(V_i - V_{Tn}) - V_{oL}}{V_{oL}}$$

For τ_{fall} case, we have
$V_i = V_{DD} - V_{Tp} = 1.8 - 0.45 = 1.35\text{V}$, $V_{oL} = V_{Tn} = 0.4\text{V}$,
$V_i - V_{Tn} = 1.35 - 0.4 = 0.95\text{V}$.
Substituting these values, we get

$$\frac{K_n\tau_{fall}}{C} = \frac{2(1.8 - 1.35 + 0.4)}{0.95^2} + \frac{1}{0.95} \ln \frac{2 \times 0.95 - 0.4}{0.4}$$

$$= 1.8837 + 1.0526 \times 1.3218 = 3.2750$$

since $\tau_{rise} = \tau_{fall}$, we get

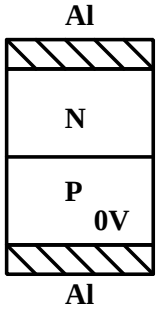
$$\frac{K_n}{K_p} = \frac{\mu_n C_{ox}(W/L)_n}{\mu_p C_{ox}(W/L)_p} = \frac{3.2750}{3.1153} = 1.0513$$

Since $L_n = L_p$, this leads to

$$\frac{W_n}{W_p} = 1.0513 \times \frac{\mu_p}{\mu_n} = 1.0513 \times \frac{130}{270} = 0.5062$$

– **[3]**

Q–3 Consider a silicon pn junction diode with Aluminium as the contact metal.

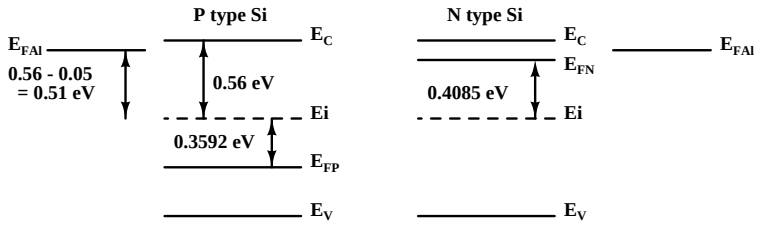


The p side is doped to 1.5×10^{16}atoms/cm^3, while the n side is doped to 10^{17}atoms/cm^3. The electrostatic potential in the bulk of the p side is 0V. The contact metal is Aluminium, whose Fermi level lies 50meV below the conduction band of silicon. The band gap of silicon may be taken as 1.12 eV.

The Fermi level in the P semiconductor is $KT/q\ \ln(Na/n_i)$ below the midgap, while that for the N semiconductor is $KT/q\ \ln(Nd/n_i)$ above the midgap.
Take $KT/q = .026\text{V}, n_i = 1.5 \times 10^{10}/\text{cm}^3$.

Find the electrostatic potential
i) at the Aluminium contact on the p side
ii) in the bulk of n side (outside the depletion region), and
iii) at the Aluminium contact on the n side.

Soln. 3) Fermi level on the P side is $.026 \ln 10^6 = 0.3592$eV below midgap.
Fermi level on the N side is $.026 \ln(10^7/1.5) = 0.4085$eV above midgap.
Fermi level in Aluminium is $1.12/2 - .050 = 0.51$eV above midgap.



i) Fermi level of Aluminium is .3592+0.51 = 0.8692 eV higher than that of P type Si. If the potential in the bulk of P side is take to be 0, the potential at the metal in contact with P silicon will be +0.8692 V.
ii) Fermi level in the bulk of N type Si is 0.4085 eV above midgap. So it is higher than that of bulk in P type by .3592 + 0.4082 = 0.7674 V. Therefore the potential in N type Bulk is +0.7674V.
iii) Fermi level of Aluminium is 50 meV below silicon conduction band. Thus it is $1.12/2 - 0.05 = 0.56 - 0.05 = 0.51$ eV above midgap. This is $0.51 - 0.4082 = 0.1018$ eV above the Fermi level of N type bulk. Therefore the metal contacting N side is 0.1018 V positive with respect to N type bulk. Since the potential of N side bulk is 0.7674 V, the potential of Aluminium contacting N side is $0.7674 + 0.1018 = +0.8692$V. – **[1]**

Paper Ends