- **I/O's devices are used to get input and display the output to the CPU.**
- **I/O's are also known as extended memory systems.**
- **Main memory belongs to frozen data but I/O's can provide the live data from real world.**
- **CPU is faster but I/O's are dead slow so we need interface to resolve the speed issue.**

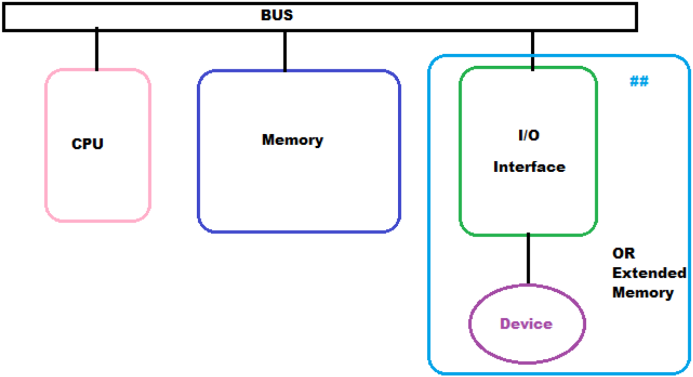

Figure : CPU-Memory-I/O block level representation

- **I/O block:**

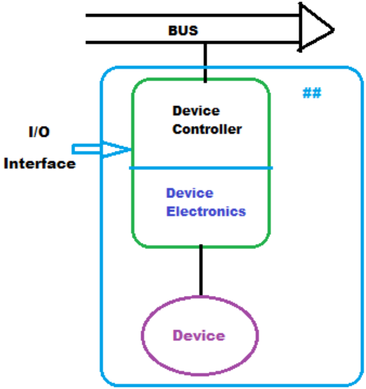

Figure : I/O block

- **I/O's interface comprises of mainly two parts:**
- Device electronics block.
- Device controller block.

- **Device electronics block: Deals with device functionality part like rotatory parts of motor.**

- **Device controller block: Deals with CPU and BUS at the time of data transfer.**
- It manage the data transfer between I/O device and BUS to enhance the system efficiency.

- **At CPU end, corresponding device driver will be running.**
- Device driver will generate the code to device controller block.
- Once data will be placed to CPU, device driver will verify the code, sent earlier.

- **Device Controller:**

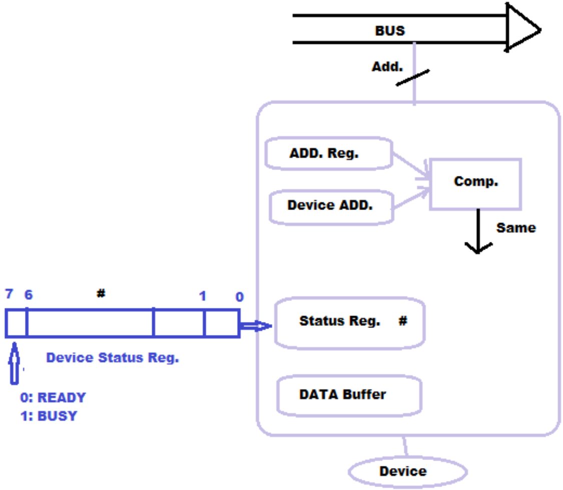

Figure : Device controller block

- **CPU will send the code to identify the concern device.**
- Comp. will compare whether the code is same or not.
- **Mode: CPU**
- CPU will address the status reg. whether the device is ready or not.
- If device is ready it will take the data from buffer.

- **Mode: I/O's**
- CPU check mode: Device is ready or not.
- Programmed mode:If device is ready it will put the data into Data buffer reg.
- Device polling: Whichever device is ready it takes the data from that device.

- **Device Electronics:**

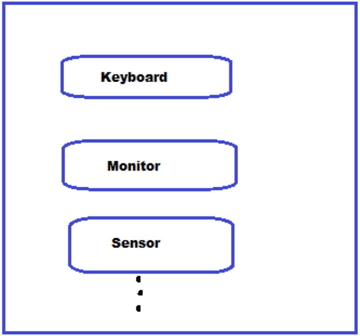

Figure : Device electronics block

- **Address a device:.**
- **Check it's status.**
- **If ready do the data transfer.**

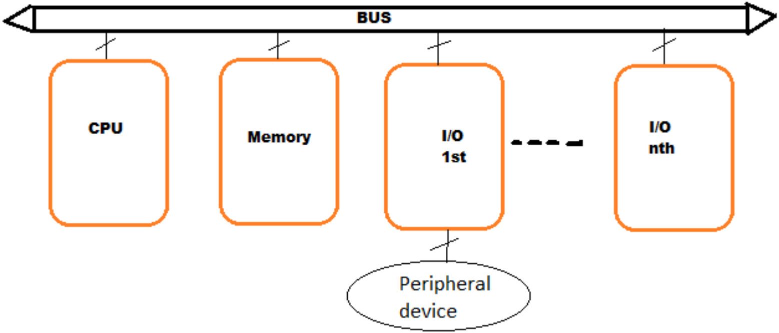

Figure : Example of programmed I/O's

- **(I)I/O Multi-function**
- **Command register: Write**
- CPU send the command to write.
- **Status register:Read**
- CPU send the command to read.
- **Configure phase:**
- CPU send the command what I/O's has to do.
- **Transfer phase:**
- In this phase peripheral chip interface the Bus and peripheral device.

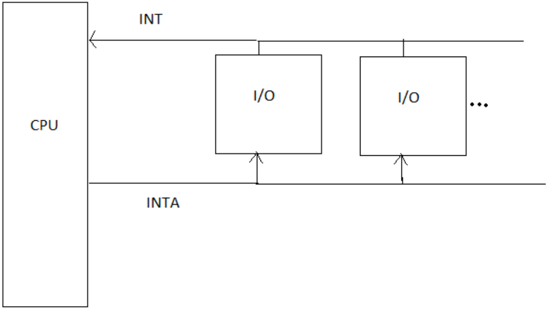

Figure : Example of programmed I/O's INT condition

- **(II) Interrupt driven I/O:**
- **INT: Signal is generated by the I/O device when it is ready.**
- **INT is asynchronous signal, can be generated any time i.e. it is not synchronous with system clock.**
- **INTA:It is an acknowledge signal, will be send by the CPU at the end of instruction cycle.**

- **Mult-interrupt:**
- More than one device requested for interrupt.
- CPU can be confused which interrupt should handle first.
- **Possible Solutions:**
- While acknowledge phase CPU must check each device sequentially.
- Interrupt device must send the identification code (vector) by itself.

- Vector code gives the start address of device routine.
- **Priority based interrupt:**
- Multi-interrupt signal generation at same time.

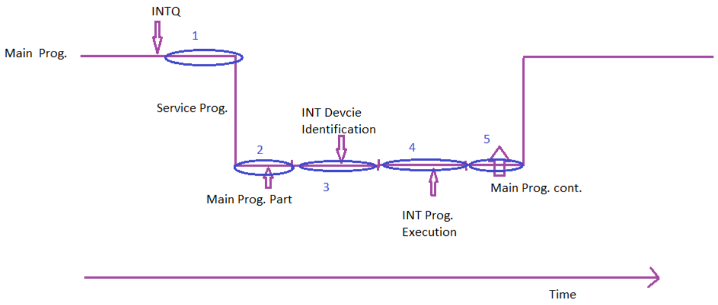

Figure : Timing diagram of INT signal

- **(1):Interrupt latency time.**
- **(2):Saving main program content.**
- **(3):Interrupt device checking.**
- **(4):Interrupt device routine execution.**
- **(5:)Coming back to main program where it was left and start execution further.**