- **Bus is noting but bunch of wires according to CPU and memory blocks requirement.**
- **In another words bus is set of signal lines or highway over which data/address moves.**
- **Bus has drivers to improve the driving capability using current amplifiers.**

- **CPU communicate with the different memory blocks and I/O devices at different speed.**
- **Bus can be unidirectional and bidirectional.**
- **Bus is technology dependent once technology will change the same bus may not be useful to new CPU.**

- **Bus Specifications :**
- **Logical: Sequence of actions**
- Read or Write kind of things not electrical quantities like voltage or current.
- **Electrical: Voltage or Current signal levels**
- Physical quantities must be there in terms of low signal level or high signal level.
- **Mechanical:**
- it is called so because of mechanical portion i.e. human interaction with computer hardware like bus connector.

- **Bus sections:**
- Data transfer: Simple movement of data.
- Priority arbitrator: CPU interrupt signal.
- Initialization : Reset Signal, clock signal, power monitoring signal etc..

- **Processor-Memory bus:**
- The rate of transfer of data/address will be very faster than peripherals.
- Short bus in terms of physical length of wires and fast.

- **I/O bus:**
- Transfer rate of data/address will be slow than processor-memory bus
- Long bus and slow.

- **Back plane bus:**
- On PCB entire set of signal lines to connect the different blocks.

- **Bus latency:**
- Bus availability whenever requested so bus latency must be as low as possible.
- **Bus bandwidth:**
- Maximum transfer of data at a time.
- Buffering and blocks of data increases the bandwidth.
- **Bus latency and bandwidth are compliment to each other.**

- **Synchronous bus**
- Communication between CPU and memory.

- **Asynchronous bus**
- Communication between CPU and I/O's.
- Less speed because of I/O's response time.
- Master-Slave communications interlocked.

- **Handshaking signals:**
- To make proper communication between CPU and other peripherals.
- Master generated signal **mastersync** to place the address.
- Slave generated the signal **slavesync** to place the data.

- **ASSERTED: Signal is placed**
- **NEGATED: Signal is removed**